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INTEGRATION

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Executive Summary

A central part of a microsystem is the control and signal-conditioning electronics where more MEMS devices are functioning as either hybrid or monolithic solutions. The choice of whether or not to integrate the electronics on the same chip as the MEMS elements or to use a hybrid solution is one of the most contentious issues in microsystems technology. The adopted approach will significantly impact product development time, cost, size, performance, reliability and the associated infrastructure (equipment) requirements.

The aim of this roadmap chapter is:

- To clearly highlight the differences between monolithic and hybrid integration and to identify their respective merits
- To identify current and future trends in MST integration
- To highlight any potential roadblocks
- To provide a discussion of the typologies of integration
- To discuss the term “Integration Modules”

The issues significantly overlap other areas of the roadmap as each other area of the manufacturing process will be determined to some extent by the choice of monolithic or hybrid integration and vice versa.

Integration is one of the central strategic decisions in a firm’s product design and development. For many years, it has meant the integration of control and signal-conditioning electronics to a sensor. Now it might include integration of actuation, micro power on a chip, wireless communications, and the like. Examining the current state of the art in hybrid and monolithic solutions can only make the right integration choice.

The latest efforts to integrate not only “Smarts,” but also other functions are often discussed in term of RF wireless communications. Here, RF MEMS hold great promise since the power consumption numbers are so much better than their semiconductor cousins. However, because of size and other issues, more functionality must be put on a chip for RF MEMS to have a value proposition that would allow it to be used in widespread applications such as cell phones. Integration today is centered on sensing, thinking, and actuation; in the future it might include communications, power, navigation and other functions.

Contributors to this have chapter have provided information on MEMS integration device typologies. First, we separated the integration technologies as MEMS first, MEMS in the middle, and MEMS last. Second, we provided the understanding that many hybrid technologies are becoming close to integrated solutions with chip-on-chip and other solution sets. Finally, the contributors understand that MEMS solutions can be provided by many microsystems device typologies such as discrete, hybrid, monolithic with smarts, monolithic with smarts and

communications, monolithic with smarts plus other functions, etc., over the time of their utility. Here we use the term smarts and the figure S to mean integration of control and signal-conditioning electronics to a sensor. Furthermore, we use the terms smarts or S and communications or C to mean the integration of control and signal-conditioning electronics to a sensor as well as wireless communication. Finally, many in our group suggest other functional integration along with the integration of control and signal-conditioning electronics to a sensor or actuator.

Integration is both a strategic and a competence issue for a firm seeking a competence advantage on the basis of microsystems communications as well as the user of a microsystems solution. For the most part, integration has been made possible by the advent of sacrificial surface micromachining. Manufacturing alternatives now exist with monolayer technology for HARM-based solutions to be bonded in a quasi-monolithic approach. MEMS devices have evolved from simple sensors to devices that sense, think, act, and communicate. Thus, it is natural that some will seek a monolithic integrated solution. But is a company's choice to go the integrated or hybrid microsystems route as simple as some often-heard statements? One such statement is "Those that can, do and those that can't, don't? Integration is fundamentally good and in a commercial sense almost Darwinian." Or is it a more of a firm's fundamental decision driven by cost, performance, and other issues?

This decision has far-reaching implications on the manufacturing technology of choice and, therefore, the typology of future products a firm might produce. Firms have succeeded or failed using both design strategies.

The alternative argument to integration is often posed as "Integration is technologically interesting and challenging, but often produces the most complex solution to a commercial problem. It is expensive and often unreliable. It is the solution of last resort to microsystems solutions."

First, it is difficult to produce devices that sense and think, and placing other functions on the chip seems dubious indeed. Where devices such as the Analog Devices' series of accelerometers do sense, think, and communicate, they do not yet communicate in a wireless fashion. Most of the discussion in this chapter will center on the sense, think, and act portions, as well as communications and power issues.

1.0 Introduction

A central part of a microsystem is the control and signal-conditioning electronics or the thinking part of MST devices. The choice of whether to integrate the electronics on the same chip as the microelectromechanical system (MEMS) elements or to use a hybrid solution is one of the most contentious issues in microsystems technology. Some of our contributors think that integration is “Good.” Others feel that the decision to integrate or not is one driven by cost, performance, and other issues. In either case, this decision has far-reaching implication for the choice of manufacturing technology and, therefore, the typology of future products a firm might produce. Firms have succeeded or failed using both design strategies.

This sometimes continuous argument might be put in place by the following two statements that paraphrase the discussion around the issue of integration. The pro argument can be put forth as:

“Those that can do, and those that can’t, don’t? Integration is fundamentally good and in a commercial sense almost Darwinian.”

The alternative argument to integration is often posed as “Integration is technologically interesting and challenging but often produces the most complex solution to a commercial problem. It is expensive and often unreliable. It is the solution of last resort to microsystems solutions”

It is true that placing both the MEMS and the IC solution on one chip approximately doubles the cost of silicon and limits microsystems manufacturing flexibility. It is also true that both cost and performance advantages can be obtained from integration in many applications. Our contributors argue that the choice of either an integrated “Monolithic” or a hybrid microsystems solution is a much more complex and commercially insightful process. This decision is a key element in a firm’s choice of product platform design, a critical issue in the commercialization of any technology. A firm’s choice to provide an “Integrated or Monolithic” solution versus a “Hybrid” solution fundamentally affects a firm’s commercial strategy in the field of microsystems. The adopted approach will significantly impact product development time, cost, size, performance, reliability, and the associated infrastructure (equipment) requirement.

2.0 Trends Driving Integration

The International Roadmap on Microsystems supported by SEMI, MANCEF, IVAM, and over 300 firms has identified trends that seem to point toward integrated solutions. First, the roadmap depicts a trend toward systems solutions rather than discrete devices. Similarly, there's a trend toward more complex devices that not only act as simple structures or sensors or actuators, but also provide customer value by sensing, thinking, acting, communicating, and/or navigating. Finally monolithic packaging solutions are advancing. This trend allows more ease of access to the environment while maintaining semiconductor circuit integrity. This is the harbinger for a new realm of integrated microsystems solutions that can address applications to an increased set of energy domains and environments.

2.1. Integration Typologies

Integration typologies between MEMS micromachining technologies and semiconductor microfabrication technologies have historically been driven by thermal management concerns. They traditionally have fallen into three categories: MEMS first or processes typified by Sandia National Laboratories' IMEMS process; MEMS in the middle of processes typified by Analog Devices' accelerometer process; and MEMS last processes typified by Texas Instruments' processes. Novel materials like silicon germanium and bonded-wafer technologies are challenging these processes.

2.2. Why Not Integrate?

Reasons not to integrate mirror those that suggest when to integrate. Integration limits manufacturing flexibility and many times is not the optimal solution. Many times hybrid solutions satisfy the requirements or are the superior design. Criteria that dissuade integration include:

1. Cost and development time
2. The yield on microsystems manufacturing steps is poorer than CMOS steps, increasing the device costs and decreasing yield in overall design
3. The manufacturing process is much more complex than a hybrid solution
4. It takes time to understand how much smarts to put on a microsystems chip
5. Multi-chip modules, grid arrays, and flip-chip technology make hybrid solutions much more feasible

6. Integration does not fit the technological competence of a firm
7. A firm's wishes to adopt a more flexible manufacturing strategy

2.3. Why Integrate?

One integrates not when one can, but when there are clear benefits. The benefits of integration must overcome yield concerns and must be cheaper or perform much better or both. Some factors that point to an integrated solution include:

1. Cost advantages are realized
2. Integration acts as a partial packaging alternative
3. Reliability is increased
4. There is sufficient volume to rapidly move down the average cost curve
5. The amount of "Smarts" required is not overburdening
6. A reduction of chip leads
7. Other performance characteristics are advanced
8. Integrated solutions fit your strategic product and manufacturing platform.

2.4. What Exactly is Monolithic versus Hybrid Integration?

Monolithic integration employs mass-production batch-processing techniques developed by the IC industry to produce MEMS elements and microelectronics on the same substrate. These may be realized in a fully integrated process flow or by adding MEMS elements before or after a standard IC process. Only the latter has the potential to vertically integrate MEMS elements. Examples of the three approaches are the Analog Devices integrated polysilicon sacrificial surface-micromachining (SSM) process, the Sandia IMEMS polysilicon SSM process, and QinetiQ's metal/nitride SSM process (Figure 1).

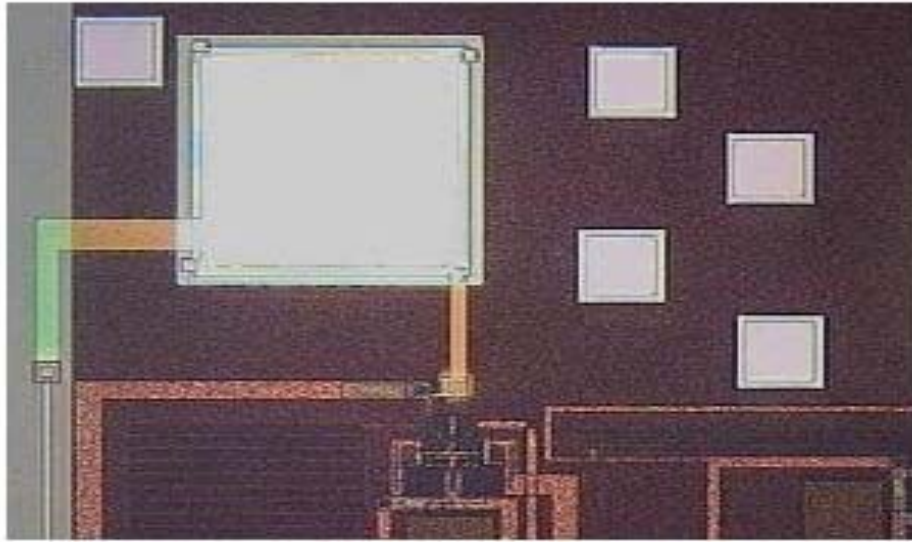


Figure 1. A Fully Integrated Acoustic Microsensor Fabricated by Post-processing on a Standard 0.8- μm CMOS Substrate.

The degree of integration employed is a major factor. As a result, monolithically integrated devices are sub-divided into the following categories in order of complexity:

- (i) *Level 1: Minimal Integration*—essential electronic blocks only (sub-component)
- (ii) *Level 2: Partial integration*—control and sense electronics (component)
- (iii) *Level 3: Full integration*—control, sense, and data-processing electronics (microsystems)

In *hybrid integration*, the key difference to the monolithic approach is that one or more chip(s) contain only MEMS structures (i.e., with remote control and sense electronics). This obviously removes the constraint that the MEMS process needs to be IC compatible and, hence, offers greater flexibility. The precise hybrid approach employed can vary widely. In this roadmap, hybrid integration is broadly sub-divided into two categories:

- (i) *Level 1: Discrete electronics*—e.g., printed-circuit board (pc-board) electronics, surface-mount solutions

- (ii) *Level 2: ASIC electronics*—e.g., multi-chip modules (MCMs) and direct chip-attach (DCA) devices

Finally, other than strategic issues, the following chart (Figure 2) provides a simple view of the benefits of integration and hybrid technologies. This demonstrates that volume considerations play an important role in the decision to choose an integrated strategy.

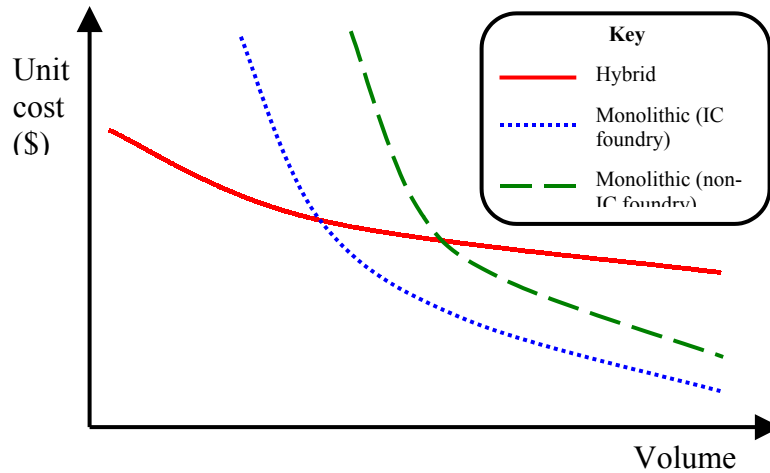


Figure 2. Cost Volume Graphs for MST Devices and their Integration Route (arbitrary scales).

Integration has been an effective strategy for Texas Instrument’s Digital Micro machine Display (DMD) device, Analog Devices’ air-bag accelerometer, and others. Monolithic integration has adapted well to applications where capacitive (high-impedance) transduction is utilized, and where excessively long tracks/bond wires and bond pads degrade performance via parasitic capacitive and resistive loading. Hybrid solutions are performing well in many other energy domains. The leading monolithic market segment is motion sensors where it’s predicted to garner only a 30% market share by 2004. Yet trends are moving toward integration and more and more it is becoming a strategic rather than a technological question for a firm.

3.0 Integration Typologies

Some form of sacrificial surface micromachining has led the charge for monolithic microsystems integration on a chip. Roger Howe and others produced the early versions of sacrificial surface micromachining technologies. Early versions of these SoCs found application in the commercial world as acceleration sensors for airbag deployment—for example, Analog Devices’ ADXL50, and for digital micro-mirror displays like those developed by Texas Instruments. Two advances in manufacturing techniques for micromachined systems-on-a-chip

made it possible to achieve great leaps ahead in system complexity. One was a three-layer polysilicon micromachining process which included a fourth polysilicon electrical interconnect layer. The other was a single-layer (plus second electrical interconnect level) polysilicon surface micromachining process integrated with 1.25- μm CMOS. Examples of systems-on-a-chip built in these processes are pop-up mirrors and multi-axis accelerometers.

Surface micromachining can be combined with IC processes to create a single chip or an integrated micro-electro-mechanical system. The most common mechanical material used for surface micromachining has been polycrystalline silicon; however, other materials derived from electroplating, depositions, polyimides, and silicon germanium have also been used. Monolithic integration of MEMS with driving, controlling, and signal-processing electronics have in many cases improved performance of micromechanical devices, as well as reduced the cost of manufacturing, packaging, and instrumentation for these devices, by combining the micromechanical devices with an electronic subsystem in the same manufacturing and packaging process. Integrating CMOS or biCMOS structures with a sensor and/or actuator element places a larger premium on the die area as opposed to non-integrated solutions. The die area is expanded by many aspects and is directly attributed to bringing these two technologies together, such as buffers between the two technologies and larger masking, relatively thicker MEMS films, and alignment tolerances. This initiates a trade-off between shrinking the critical dominions and optimization interconnection. The integration of surface micromachined structures with microelectronics is most efficiently performed with a minimum disruption to the IC process flow. There is some disagreement on how that is best accomplished.

One of the major problems with integrated MEMS SoCs is the thermal budget for IC processing and integrating that in a compatible manner with surface micromachined devices. Polysilicon micromechanical structures require long, high-temperature anneals to ensure that the stress in the structural materials of the micromechanical structures is completely removed. CMOS technology requires planarity of the substrate to achieve high resolution in the photolithographic process. If the micromechanical processing is performed first, substrate planarity is sacrificed. If the CMOS is built first, it (and its metallization) must withstand the high-temperature anneals of the micromechanical processing. There have been three basic proposals for true monolithic MEMS manufacture: MEMS last, MEMS first, and MEMS in the

middle. Materials and substrate issues are now causing firms commercializing integrated solutions to rethink their approach.

Texas Instruments' Digital Light Projection technology with aluminium is the most famous case of MEMS last technologies. TI utilizes their unique micromachining technology and the micromachined structure *after* the IC is manufactured using plating or deposited films. TI Digital Micro mirror displays now dominate the projector marketplace, but this process was extremely expensive to develop. Currently, TI has an exceptional IP position in this form of sacrificial surface integration (Figure 3).

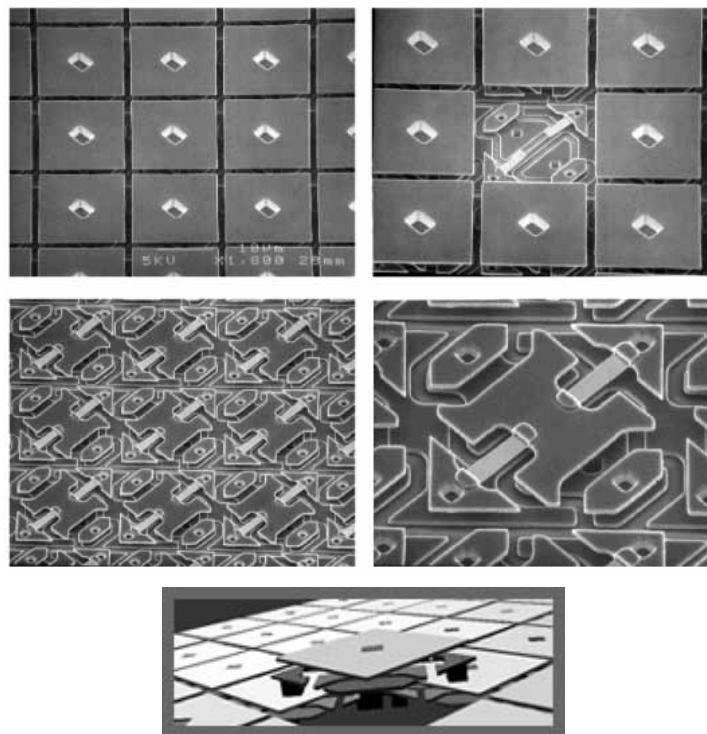


Figure 3. Texas Instruments' DMD Device Manufactured with Digital Light Processing (DLP) Technology.

The microsystems in the middle approach has been made most famous by Analog Devices. The company uses a highly forgiving first phase of the fabrication process, a biMOS process that uses large geometry devices (3- μm gates) and dopants (As) that have low diffusion coefficients. One of the major reasons for this is the thermal budget management. The biMOS process has good performance after the 950°C and 4-hour polysilicon anneal. This form of monolithic integration can be described as inserting the mechanical surface micromachined process in the middle of the biMOS flow *before* contact and metallization occurs. Contacting the mechanical structures, depositing and forming the thin-film resistors, aluminum metallization, and the

passivation complete the process sequence. The remaining steps are to protect the circuit structure with photoresist; etch away the sacrificial layer under the mechanical polysilicon; and then remove the photoresist with a suitable dry etch. This insures that the final steps are not subject to liquids and surface tension that can result in adhering the polysilicon elements to one another or the substrate, when the surface micromachined structures are released.

A unique micromechanics-first approach, which overcomes the planarity issues of building the MEMS before the CMOS, was developed at Sandia National Laboratories. In this approach, micromechanical devices were fabricated in a trench etched on the surface of the wafer. After these devices were complete, the trench was refilled with oxide, planarized using chemical-mechanical polishing, and sealed with a nitride membrane. The wafer with the embedded micromechanical devices was then processed using conventional CMOS processing. Additional steps were added at the end of the CMOS process to expose and release the embedded micromechanical devices. Completed devices are shown in Figure 4. A cross-section of this technology is shown in Figure 5. This technology was named as one of the recipients of the 1996 R&D 100 Award.

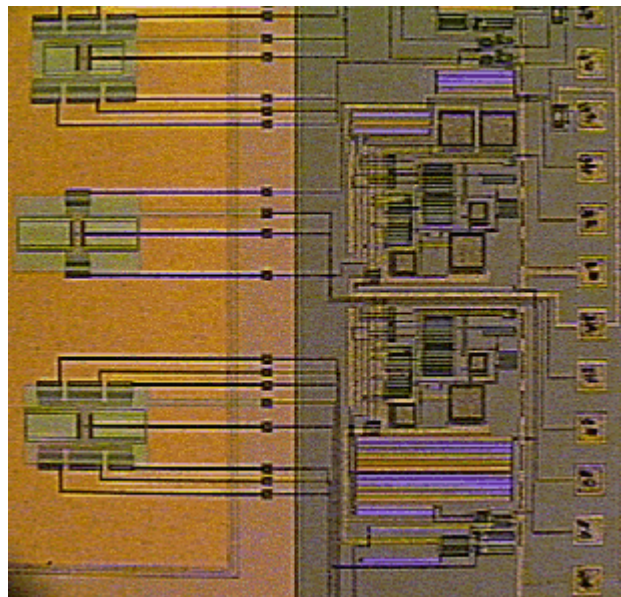


Figure 4. Micromachined Resonators (left) next to their CMOS Drive Electronics (right) Fabricated using the Embedded Micromechanics Integration Process.

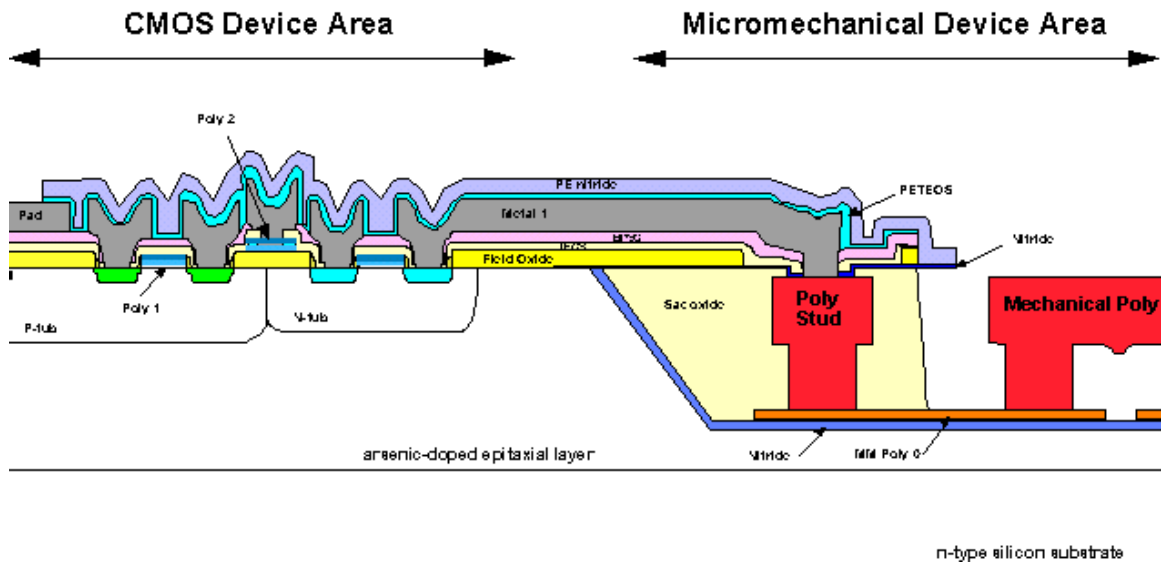


Figure 5. A Schematic Cross-section of the Embedded Micromechanics Approach to CMOS/MEMS Integration.

This technology was utilized by the University of California Berkeley's Sensors and Actuators (BSAC) labs, and Sandia National Laboratories to manufacture a three-axis, force-balanced accelerometer. This overcame the need to manually align and assemble the accelerometer into a three-axis system, improving the resulting alignment tolerances and other aspects. This accelerometer SoC is shown in Figure 6. The Sandia IMEMS three-layer process includes three movable levels of polysilicon in addition to a stationary layer for a total of four layers of polysilicon. Sacrificial oxide layers separate the polysilicon layers from one another. A total of eight mask layers are involved in this process. An additional friction-reducing layer of silicon nitride is placed between the layers that form bearing surfaces.

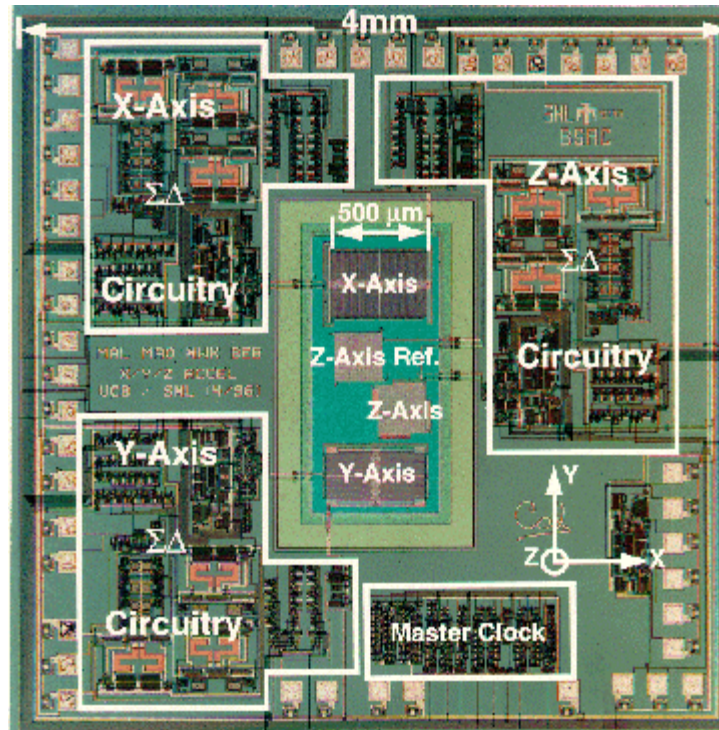


Figure 6. A Micrograph of a Three-axis Accelerometer.

Finally, new materials and close-to-monolithic hybrid solutions are entering the field of monolithic integrated MEMS, challenging established practices on economic grounds. One solution is micromachined devices made from silicon-on-insulator (SOI) that could easily be described as surface micromachined, since they have mechanical structures on the surface. These devices use the buried oxide of the bonded wafer as the sacrificial layer. A similar structure created by epitaxial deposition of silicon over oxide, produces a polysilicon structure. These various devices are described in the Non-IC and IC Fabrication chapters. The reader will find several of these structures in automotive production in the nonintegrated form, and, doubtless in the future, will find them integrated as the economics of larger volumes justify their development as specialized single chip solutions. The use of polycrystalline silicon germanium allows deposition of layers at a much lower temperature, therefore, eliminating much of the thermal management problems, which allow the designer a much greater degree of flexibility in manufacturing design and product flow. This lowering of temperature restriction allows MEMS manufacturing at almost any point along the MEMS up front, MEMS in the middle, and MEMS at the end continuum.

A new form of MEMS last technology is offered through the use of polycrystalline silicon germanium. These efforts are in the development phase at U.C. Berkeley, IMEC in Belgium, and other research facilities. This eliminates some of the thermal-management concerns in an integrated process since the deposition temperatures of Si-Ge is considerably lower than polysilicon and does not appear to interfere with CMOS or biCMOS electronics. This has the additional advantage of eliminating a hydrogen-fluoride (HF)-based release process through the judicious selection of the germanium content in Si-Ge, and then the process can use Si-Ge as both the sacrificial and structural layers. The release process in Si-Ge is based on peroxide rather than HF (Figure 7).

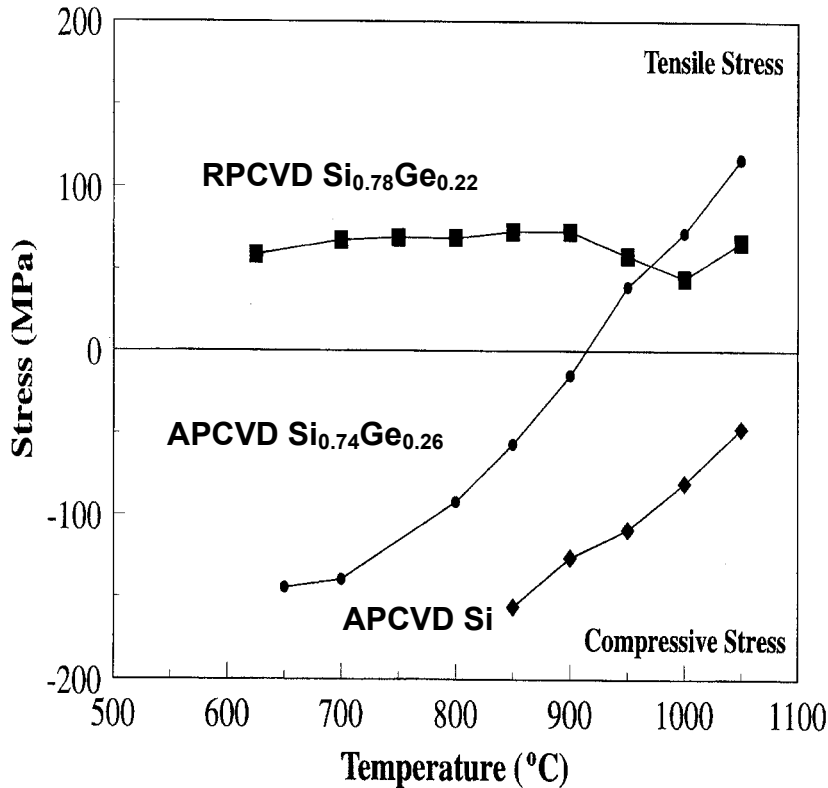


Figure 7. Stress Comparison between Poly SiGe and Silicon over a Wide Temperature Range [Sedky, 1998].

An alternate approach is to incorporate wafer-bonding processes for the MEMS integration. Wafer bonding can be applied in the case of “MEMS First” and further used to combine and serve as packaging functions as well. MEMSIC has developed and brought to market such a unique MEMS-based accelerometer that contains no moving parts using such an approach.

MEMSIC's product combines the sensor and associated electronics onto a single chip manufactured on a standard, sub-micron CMOS process. The accelerometer provides the highest long-term reliability and performance available today at an unprecedented low cost. Hybrid solutions are approaching integrated solutions with chip-on-chip and flip-chip methods by combining processing and packaging aspects to form an integrated microsystem.

4.0 The Pros and Cons

It is true that placing both the MEMS and the IC solution on one chip approximately doubles the cost of silicon and limits microsystems manufacturing flexibility. Adding more MEMS functionality will increase that cost. It is also true that both cost and performance advantages can be obtained from integration in many applications. We argue that a firm's choice to provide an integrated or monolithic or a hybrid microsystems solution is a much more complex and commercially insightful process. This decision is a key element in a firm's choice of product platform design, which is a critical issue in the commercialization of any technology. Whatever the choice, it fundamentally affects the company's commercial strategy in the field of microsystems. The adopted approach will significantly impact product development time, cost, size, performance, reliability, and the associated infrastructure (equipment) requirement.

5.0 Device Types Driving Integration

The trend for integration is to opt for devices that provide "Solutions," rather than use discrete MEMS-based devices. With advancements in microsystems manufacturing technologies, discrete MEMS devices themselves are getting more complex as the structures, not only sense and actuate, but many times are required to sense think, actuate and communicate. We have classified them into four separate segments (see Figure 2): Class 1, devices with no moving parts; Class 2, moving parts and no rubbing or impacting surfaces; Class 3, moving parts and impacting surfaces; Class 4, moving parts, impacting and rubbing surfaces. Class 1 devices include pressure sensors, ink-jet printheads, and strain gauges. Class II devices include comb drives, gyros, resonators, and filters. Class II devices include relays, valves and pumps. Class IV devices include optical switches, shutters, scanners, locks, discriminators, and the like. These vast new devices have created a new type of integration: integrating differing MEMS functions and IC-like intelligence on the chip.

A second trend also suggests an integrated solution, the trend toward systems solutions rather than discrete devices. Similarly, there's a trend toward more complex devices that can not only act as simple structures or sensors or actuators, but also provide customer value by thinking, communicating, and assembling or navigating (see Figure 4). Figure 3 depicts the generation of microsystem device technologies, in which each can be thought of as a design choice between monolithic or hybrid solutions. Here, categorization includes wired communication sensors or actuators that utilize digital-to-analog or analog-to-digital converters (DACs and ADCs), like pressure sensors, which are currently designed as either integrated or hybrid solutions. Second-generation devices include a certain amount of on-board smarts that utilize DACs and ADCs. These include accelerometers currently designed as either integrated or hybrid solutions. Third-generation devices include wireless communications. These multifunctional RF-based MEMS devices are only now being contemplated and prototyped. Fourth-generation devices include wireless communication and on-board power that are just now being contemplated as integrated monolithic solutions; they're now being prototyped as hybrid solutions.

Packaging has also advanced to allow for excellent monolithic or hybrid solutions. Monolithic packaging solutions are advancing. This trend allows more ease of access to the environment while maintaining semiconductor circuit integrity. This is the harbinger for a new realm of integrated microsystems solutions that can address applications to an increased set of energy domains and environments.

6.0 Trends against Integration

Reasons not to integrate mirror those that suggest when to integrate. Integration limits manufacturing flexibility and many times is not the optimal solution. Every added function requires many more processing steps and, therefore, decreases yield. MEMS manufacturing steps are not as robust as their IC microfabrication cousins. Many times, hybrid solutions satisfy the requirements or are the superior functional and cost design.

Criteria, which dissuade integration, include:

1. Cost and development time
2. The yield on microsystems manufacturing steps is poorer than CMOS steps, increasing device costs and decreasing yield in overall design

3. The manufacturing process is much more complex than a hybrid solution
4. It takes time to understand how much smarts to put on a microsystems chip
5. Multichip modules, grid arrays, and flip-chip technology make hybrid solutions much more feasible
6. Integration does not fit the technological competence of a firm
7. A firm wishes to adopt a more flexible manufacturing strategy

7.0 When to Provide an Integrated Monolithic Solution

One integrates not when one can, but when there are clear benefits. The benefits of integration must overcome the yield concerns and must be cheaper or perform much better or both. Some factors that point to an integrated solution is:

1. Cost advantages are realized
2. Integration acts as a partial packaging alternative
3. Reliability is increased
4. There is sufficient volume to rapidly move down the average cost curve
5. The amount of “Smarts” required is not overburdening
6. Reduction of chip leads
7. Other performance characteristics are advanced
8. Integrated solutions fit your strategic product and manufacturing platform.

8.0 What exactly is Monolithic Versus Hybrid Integration?

8.1. Monolithic Integration

Monolithic integration employs the mass-production batch-processing techniques developed by the IC industry to produce MEMS elements and microelectronics on the same substrate. These may be realized in a fully integrated process flow or by adding MEMS elements before or after a standard IC process. Only the latter has the potential to vertically integrate MEMS elements. Examples of the three approaches are Analog Devices’ integrated polysilicon sacrificial surface micromachining (SSM) process, Sandia National Laboratories’ IMEMS polysilicon SSM process, the highly successful Texas Instrument polyimide-based CMOS process, and DERA’s metal/nitride SSM process (see Figures 3 and 4, respectively).

The degree of integration employed is a major factor, and so in this paper, monolithically integrated devices are sub-divided into the following categories in order of complexity:

- (i) *Level 1*: Minimal integration—essential electronic blocks only (sub-component)
- (ii) *Level 2*: Partial integration—control and sense electronics (components)
- (iii) *Level 3*: Full integration—control, sense and data-processing electronics (microsystems)
- (iv) *Level 4*: Wireless communication and full integration—control, sense and data-processing electronics and wireless RF MEMS
- (v) *Level 5*: Wireless communication, other MEMS functions and full integration—control, sense and data-processing electronics and wireless RF MEMS

8.2. Hybrid Integration

The key difference between the hybrid and monolithic approach is that hybrid systems take advantage of the distributed system concept. It utilizes one or more chip(s), which contain only MEMS structures (i.e., with remote control and sense electronics) and combine these through a multitude of means including flip-chips, multi-chip modules, etc., with IC-only chips. This allows MEMS manufacturers to take advantage of costs of scale for IC ASIC chips and allows specification at the MEMS chip level.

A hybrid approach removes the constraint that the MEMS process needs to be IC-compatible and hence, offers greater flexibility. A hybrid manufacturer can choose from a much larger array of materials and processes than a monolithic producer. The packaging options are also much less constrained for hybrid manufacturing. There must be compelling cost and performance benefits for a monolithic approach as well as a large enough market to warrant dedicated die.

The precise hybrid approach employed can vary widely. In this chapter, hybrid integration is broadly sub-divided into the following two categories:

- (i) *Level 1*: Discrete electronics—e.g., printed-circuit board (PCB) electronics, surface-mount solutions
- (ii) *Level 2*: ASIC electronics—e.g., multi-chip modules (MCMs) and direct chip

9.0 Hybrid versus Monolithic Design Choice—Lessons from the IC Industry

Lessons can be learned from the IC industry concerning the product design and manufacturing decision between hybrid and monolithic device choices. Cost and performance are the key drivers for any application. Similarly, broadly speaking, yield goes down with increased chip area and so a higher overall yield may be achieved by splitting a large chip into two or more parts. This is one reason that, although technically possible, mobile phones have not gone to a single-chip solution to date. Where costs are derived may be substantially different in the IC industry, where device yield is the major factor. There is, of course, the very large difference between IC and MEMS chips in packaging. The IC package is sophisticated but the cost impact on the device is negligible. MEMS packaging, assembly, and test (PAT) is also a sophisticated task but garners between 30-80% of the entire cost of the device.

1. Packaging costs play a major role in the decision to make a monolithic design. Much of the development of MST to-date has used IC-like process technologies to produce mechanical elements in silicon-based materials set. It has been natural given this synergy and the fact that large sections of the community have come from a semiconductor manufacturing background for fully integrated monolithic microsystems to be proposed. On the other hand, parts of the community from a more traditional sensors background, without a history in semiconductor manufacturing, have tended to follow a hybrid approach.
2. There's a general trend with the semiconductor manufacturer for fully integrated large volume solutions.
3. Since most semiconductor makers' use forward pricing or competitor minimization strategies, small-volume devices will piggyback other effects and use whatever devices already exist and suggest MCM applications.
4. Smart power has shown that "Smart but not too Smart" is a great axiom for an integrated strategy. This strategy suggests that you limit the amount of smarts each monolithic chip contains. This may be best displayed in microsystems by TI's micro mirror display and the Analog Devices' accelerometer series. Both applications are smart, but are just smart enough. Even in these application areas where integration solutions are prevalent and even dominant, hybrid solutions also are commercially available by firms such as Bosch and Motorola.

10.0 Arguments for Hybrid versus Monolithic

Current arguments for and against each approach broadly fall into the following categories and are discussed in more detail:

1. Cost and development time
2. Transduction mechanism, performance and reliability
3. Process technology
4. Packaging, assembly and test (PAT)

10.1 Cost and Development Time

Whether opting for a monolithically integrated MST solution or level-2 hybrid integration, upfront non-recoverable engineering (NRE) costs and the time associated with developing full or semi-custom ASIC electronics increase rapidly with circuit complexity. These costs are high compared with the use of existing, standard discrete components. IC design and layout are highly specialized if analog functions are to be included—although design reuse and/or the use of standard-cell libraries may reduce the associated NRE cost and development time significantly. Thus the unit cost of an ASIC does not fall below that of hybrid electronics until high volumes are reached. Moreover, if first-pass success is not achieved in an ASIC, then the iteration time is much longer than in discrete electronics. Rapid prototyping and proof-of-concept devices thus tend to use discrete electronics.

Cost may also be influenced by the choice of IC and/or MEMS process technology. In general, costs rise with the number of mask steps and yield falls off. Typically mixed-signal microelectronics is required in a sensor ASIC and so a more expensive biCMOS process is often used to take advantage of bipolar's analog capability. This advantage is less pronounced at smaller (0.6/0.8- μm) CMOS geometries and at low-frequency operation. Process yield also falls off significantly with larger chip area in any process using batch microfabrication techniques. In general, yields are lower in MEMS processes ($\approx 50\text{-}95\%$) than in IC processes ($>99\%$) and costs are higher due to a lower volume of generic product. Thus in a monolithic solution, a significant number of good electronics die may be wasted, increasing unit costs compared with a hybrid solution where only known good-die may be selected from the MEMS and/or electronics wafers prior to further integration. This results in significantly higher overall yield. Similarly, the relative areas of the integrated electronics and the MEMS elements will have a significant impact

on cost. For example, if level-1 monolithic integration is employed, then the chip will typically have relatively large areas of real estate that are not processed during the IC process. The cost of such elements could be many times higher than if the same ICs were fabricated all over the entire wafer in the same process for level-2 hybrid integration.

A major issue relating to development time and cost of monolithic integration is that of the compatibility of the process used to fabricate the MEMS element with the process used for the electronics. This is usually related to controlling the stress in the mechanical layers and coping with surface topography while not compromising the performance of the electronics due to excessive thermal budgets. As a standard, stable MEMS processes at MST foundries are becoming increasingly available with integrated electronics, thus development time and cost is not such an issue, since such a capability does not have to be developed in-house.

Packaging, assembly, and test may be the dominant factors in product cost. Monolithic solutions, on the whole, have simpler packaging and assembly requirements and the process is easier to automate. However, MEMS devices often require expensive, specialized packages (e.g., hermetic, TCE-matched, metal, ceramic, etc.) and monolithic devices may be significantly larger than the equivalent hybrid MEMS-only chip (that could employ a cheap, plastic package for its associated electronics) with an associated rise in package size and, hence, cost. Testing with a monolithic implementation may be more complex as the electronics and MEMS elements often cannot be tested separately prior to system-level testing. However, with appropriate test points, wafer-level testing could be performed. Often, self-test features are built-in to both monolithic and hybrid microsystems. Testing (electrical and non-electrical) prior to packaging in both hybrid and monolithic microsystems may result in cost savings under a specific yield level associated with device-specific PAT costs.

Overall, a unit cost-volume graph may be constructed as previously shown in Figure 2. This has arbitrary units as the precise volumes, and costs will be determined by the specifics of each microsystem. What the graph does clearly indicate is that a hybrid solution will be the lowest cost in all but the highest-volume applications. Also, a monolithic implementation produced by an IC foundry is likely to be lower in cost as it has higher volumes of standard products going through its line, and does not have to include the profit of a third-party IC foundry in its costs.

10.2 Transduction Mechanism, Performance and Reliability

Monolithic integration is currently most suited to capacitive (high-impedance) transduction where excessively long tracks/bond wires and bond pads degrade performance via parasitic capacitive and resistive loading. This is particularly true where the sense capacitance is of the order of a picoFarad or less. However, the large bias and actuation voltages often required may determine that monolithic integration is not possible or may restrict the choice of IC technology to higher-voltage variants (e.g., a typical CMOS process operates with a <5-volt supply). In other techniques, such as piezoresistive transduction, the impedance is reasonably low and so hybrid integration may be used without significant performance penalty. The transduction method may impact whether monolithic integration may be used and/or the MEMS process technology due to materials compatibility issues and thermal budgets. A restriction on MEMS process and hence, design freedom, may result in a non-optimal MEMS process being used that could, in turn, reduce microsystem performance.

Monolithic integration is also well suited to array applications as it avoids the need for complex bonding regimes and vertical integration is possible in some implementations. The latter is also possible in a multi-wafer level-2 hybrid solution for larger-sized elements (i.e., >100- μm pitch). This reduced the number of bonds and the need for soldering/assembly in a monolithic solution that should also lead to improved reliability compared with hybrid solutions. It should also result in improved RF immunity in a monolithic solution. Larger chip size in a non-vertically integrated monolithic solution could result in increased package-induced stress effects that could degrade performance and/or cause failure, and so level-1 or level-2 monolithic integration is likely to lead to the highest-performance solutions.

Performance often drives a monolithic choice. A monolithic approach is often warranted when a MEMS device needs to have high communications speed and a high rate of data processing from a sensed or actuated device. Similarly, the ability to integrate a temperature sensor on the same die as a sensing element makes for more-accurate temperature compensation in many applications. Size and/or power may be key performance parameters in a number of applications, such as biomedical, rather than resolution. Again, monolithic integration should lead to the lowest size and/or power solutions but the difference in level-2 hybrid integration may not be as pronounced as level-1 hybrid integration.

10.3 Process Technology

The advent of sacrificial surface micromachining imitated an interest in monolithic MEMS devices. Sacrificial surface micromachining utilized much of the existing IC fabrication tool set and was not involved in its silicon sculpting. This allowed for an interested engineer or group of engineers to embrace a combined IC MEMS process. Different IC process technologies, dominated by CMOS, bipolar and biCMOS, may limit the choice of materials and MEMS process in a monolithic implementation but provide the synergies of IC fabrication and MEMS fabrication directly. Similarly, thermal budgets, the performance specification, and the transduction technique will affect the choice of MEMS process in a monolithic solution. Examples include gold, ferroelectric materials, anodic bonding, and LIGA typically being incompatible with CMOS electronics. Such considerations do not impact hybrid solutions, providing added flexibility in the MEMS element.

Polysilicon structural layer SSM processes that use oxides and or polyimides as sacrificial layers may be incorporated into a modified biCMOS or CMOS process flow for selected applications. Pre-processing removes the constraints on thermal budgets but will still impact materials choices. However, pre-processed wafers are unlikely to be accepted by a third-party IC foundry. Fabricating MEMS elements after the electronics offers the added potential to vertically integrate the MEMS device on top of the microelectronics but constrains the choice of materials and limits the post-processing temperatures to temperatures $<450^{\circ}\text{C}$ with CMOS wafers. Typical SSM material combinations include metals and PECVD-deposited layers. For example the Sandia IMEMS process allows you to manufacture the MEMS devices first and then cap them and send the resultant wafer to any bipolar or MOS manufacturer to place the IC device on the wafer.

Traditional bulk micromachining may also be used to post-process MEMS elements on CMOS. Similarly, new and promising CMOS-compatible techniques are emerging, including high-aspect-ratio micromachining (HARM) processes based on deep dry etching of bulk silicon, SOI or silicon-on-glass, and UV-based LIGA-like electroforming.

Another issue with monolithic integration is the wafer size used in the process. Most MEMS processes run on 4-in. lines with some on 3-in. and 6-in. lines. Most IC process lines run at 5-in. (bipolar) or 6-in. (CMOS/biCMOS) with some 4-in. and 8-in. lines. The impetus to move to

larger wafer sizes is much stronger in IC lines due to much higher volumes and associated economies of scale. Obsolescence is thus a more significant issue in monolithic solutions.

10.4 Packaging, Assembly and Test (PAT)

Many issues associated with PAT have already been covered in the preceding paragraphs. Unlike IC packaging, MST often requires that the MEMS element is in intimate contact with its environment or is sealed in a hermetic or vacuum environment. The stress induced by the package may also affect microsystem performance. This means that specialized, low-volume packages are often required—more akin to specialized military IC packaging than mainstream IC packaging. It is no coincidence that the first and most successful MST devices to market (pressure and acceleration sensors) have been able to employ more conventional packaging at a lower fraction of the overall microsystem cost ($\approx 30\text{-}40\%$).

Electrical and non-electrical tests may be performed at the wafer level in some cases where device yields are low and/or packaging costs are high. Testability may be lower in monolithic solutions without the addition of test points. Non-electrical automated test equipment (ATE) for microsystems is rare, often requiring custom development, thus self-test functions are desirable. Assembly of hybrid microsystems is a more complex and potentially lower-yielding step than in monolithic microsystems. Some batch-assembly techniques from the IC industry may again be employed, but dicing and handling issues are more complex with released MEMS die than IC die as the effects of moisture (stiction) and other external effects (e.g., air currents) may damage the device irrevocably. Trimming of electrical and mechanical properties may be employed for critical elements within the microsystem before or after packaging and assembly. The final step is electrical and non-electrical testing of the packaged microsystem with many of the same limitations found at the wafer scale.

11.0 Current Status and Future Trends

The current proportion of MST devices employing monolithic integration is very low—approximately 5.6% as can be seen in Figure 8 (top). What is also apparent is that this varies significantly with the market sector with higher proportions of monolithic devices being found in the high-volume motion and pressure-sensing markets.

There's a clear trend towards ASIC electronics and/or value-added post-processed monolithic MST devices being employed in current research and development, although a lower fraction of monolithic devices will find their way into future products as reflected in the 5-year forecast in Figure 8 (bottom). Some products have initially used level-1 hybrid integration and later moved to level 2 as they establish themselves in the marketplace and volumes ramp up. In some cases, where the MEMS processing is compatible with the electronics, the logical extension of this may be to move to a monolithic solution as a high-performance variant and/or mainstream product of the future.

In the longer term (10-15 years), as volumes rise and applications mature, there will be a continuing trend towards monolithic integration, saturating at approximately 10-12%. Again, this figure will be highly dependent on application. Similarly, hybrid products will have a trend towards more complex levels of integration with the use of direct-chip-attach (DCA) techniques, such as flip-chip bonding, and ASICs, increasing. If market forecasts are correct, the relative value of the optical and RF markets will continue to increase also with an increasing fraction of monolithic integration as the fields mature. Several factors will be key in this trend to increasing levels of monolithic integration by reducing the NRE costs and development times. Core to this will be improved CAD tools for faster development cycles with higher first-pass success, and the use of standard-cell libraries of both MST elements and readout/signal-conditioning circuits, enabling design reuse and IP licensing. Similarly, the advent of MST-specific foundries offering a wider range of stable, often CMOS-compatible, processes will reduce infrastructure costs and improve MEMS process yields, making monolithic integration more attractive. This will also result in an increasing trend to working on 6-in. wafers to enable post-processing on third-party IC wafers and possibly towards 8-in. (or larger), if 6-in. (and larger) IC processes become obsolete. A back-end infrastructure with standard packages for MST and improved non-electrical ATE and assembly tools should also reduce the proportion of overall microsystem cost relating to PAT in the future, shifting the balance between monolithic and hybrid integration.

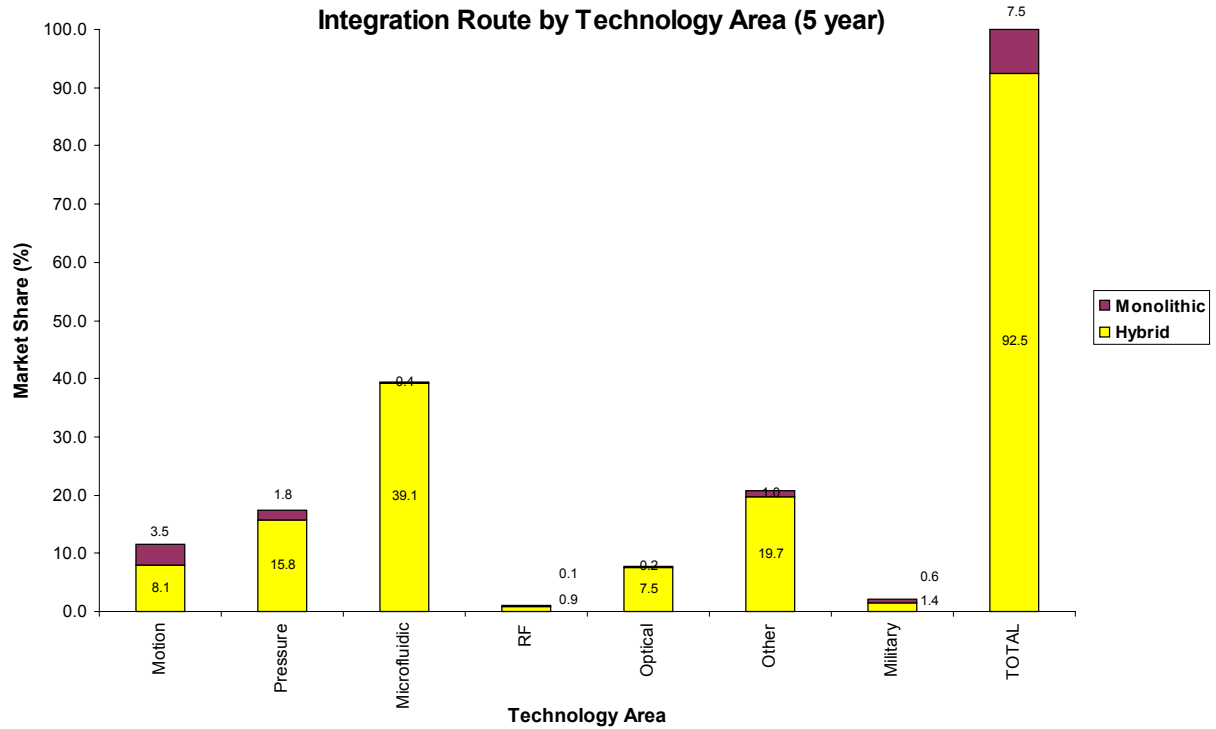
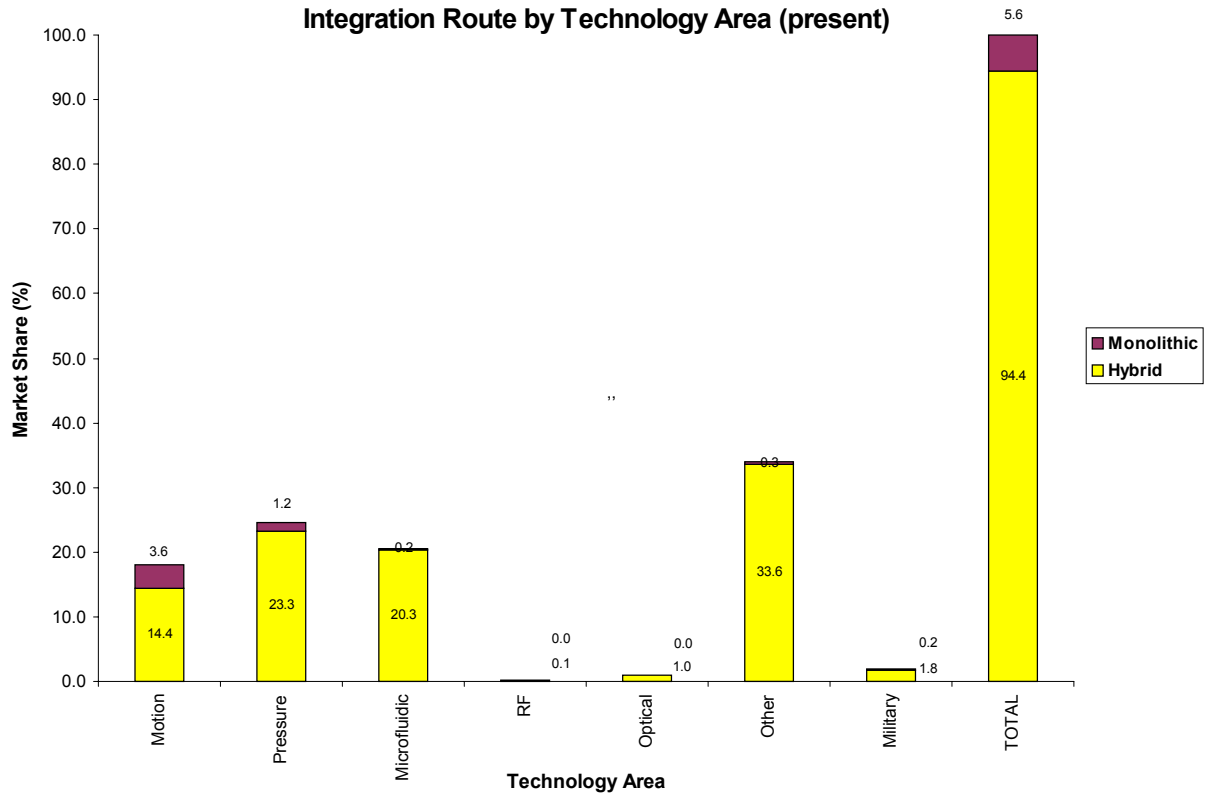


Figure 8. Current (top) and Future (bottom) Market Share by Integration Route and Breakdowns on each Integration Route, based on Technology Area (SPC market survey, 1999).

In the end, the integration route will be determined by the cost of manufacture, competition, what price the market will bear, and the time-to-market. This means that high-volume/low-cost applications, such as automotive sensors; niche, high-value/high-performance applications, such as military; and, in some cases, large-area display (addressable array) products, such as micromirrors; will have higher-than-average levels of monolithic products.

Potential roadblocks to increased levels of monolithic integration include insufficient control of material parameters (e.g., stress and uniformity) in low-temperature deposition equipment; a lack of a back-end infrastructure to supply specialized process steps, such as CMP, to remove surface topography prior to/during MEMS post-processing, and to supply PAT services with appropriate and automated equipment to reduce costs; a lack of CAD tools to allow design and simulation of the MEMS elements with electronics; and a lack of availability of stable, CMOS-compatible, MEMS foundry processes.

12.0 Conclusions

The monolithic approach offers potential size, power, and weight savings as well as improved reliability, reduced temperature variation, reduced parasitics, and improved RF immunity. Costs are potentially low in high-volume applications. On the other hand, the hybrid approach offers low entry and reduced NRE costs, shorter development cycles, lower costs at low-high volumes, and potential yield benefits.

There will be a trend towards a higher proportion of monolithically integrated MST products over the next 10-15 years as the cost-performance ratio decreases. This will be helped by the availability of standard-cell libraries of interface circuits and MEMS elements, together with a wider availability of stable, foundry processes and the use of more advanced CAD tools. There will also be a trend towards larger wafer sizes driven by the entry-level IC technology wafer size. Most of these will employ level-1 or level-2 integration, often in a multi-chip solution. This is likely to saturate around 10-12% of the market with the majority of MST products remaining hybrid. Given current MST market growth predictions, this will still represent a major market segment in terms of value. Specific product areas that will adopt a higher proportion of fully integrated products will be:

- Those with large-volume, maturing markets, such as motion and pressure sensors
- Those that cannot be engineered any other way, such as MST large array display (LAD) products
- Niche high-value, low-medium volume product areas, such as specific military, space and biomedical products where performance and/or size considerations are critical.

Within the hybrid product area, there will similarly be an increasing trend towards level-2 integration with one or more associated ASIC(s) as the cost-performance ratio falls, increasingly employing DCA and MCM solutions. Again, this trend will be particularly apparent in higher-volume, unique-solution and niche product areas. The majority of hybrid products will continue to employ level-1 integration.

Integration has been an effective strategy for TI's Digital Micro machine Display (DMD) device, Analog Devices' airbag accelerometer and others. Monolithic integration has adapted well to applications where capacitive (high-impedance) transduction can be utilized, and where excessively long tracks/bond wires and bond pads degrade performance via parasitic capacitive and resistive loading. Hybrid solutions are performing well in many other energy domains. The SPC market study suggests that integration is still far behind hybrid solutions for most MEMS applications. The leading monolithic market segment being motion sensors where they predict only a 30% market share by 2004. Yet trends are moving toward integration and more and more it is becoming a strategic rather than a technological question for a firm.

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