2011 ITRS

Emerging Research Materials [ERM]

December 14, 2011

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Work in Progress: Not for Distribution

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Work in Progress: Not for Distribution

2011 Key Messages

- **2011 ERM Chapter Updated**
- **P-Ge and n-InGaAs Transitioned to PIDS & FEP**
- **Progress on Directed Self Assembly for Lithography Extension**
- **Progress in Deterministic & Monolayer Doping**
- **Ruthenium Barrier Layers Transitioned to Interconnects**
- **Significant Challenges for all Materials**

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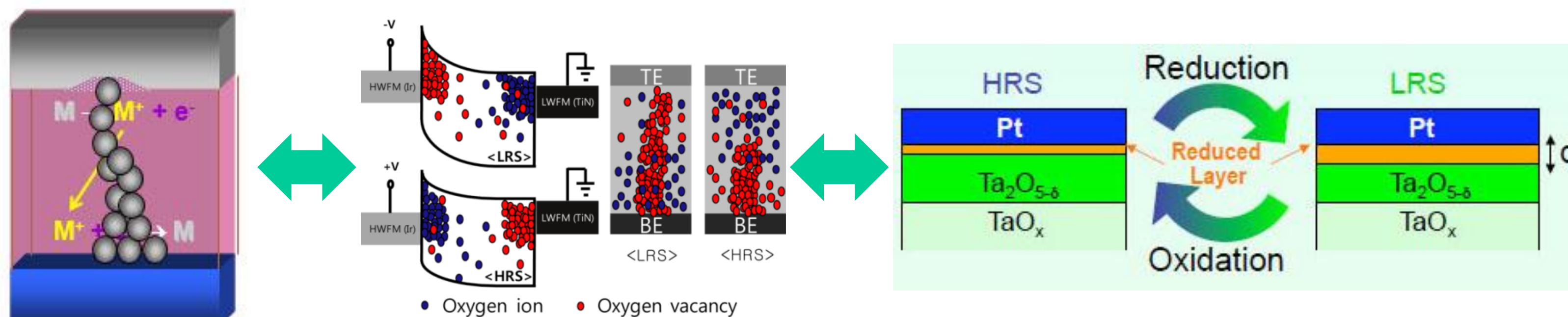
Memory Materials

- Ferroelectric Memory
- Nanoelectromechanical (NEMM)
- Redox RAM
- Mott Memory
- Macromolecular
- Molecular

Memory Materials Workshop

Redox RAM: How can we experimentally verify that the Redox RAM operating mechanism?

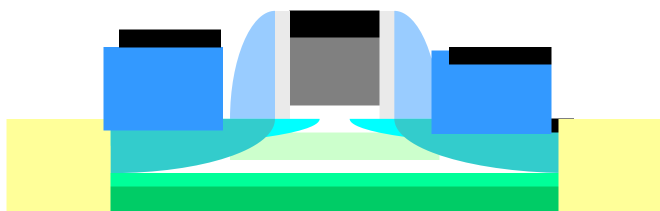


MTJ: What materials or interface research should be performed to enable reduction of write energy by 10X?

Even with the combination of MgO-CoFeB (normally in-plane), interface control enables out of plane MTJ.

Extending CMOS Logic Alternate Channel Materials

MOS



Assess

Materials Performance

Gate materials

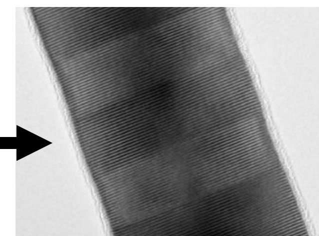
Contacts

Interfaces

Alternate Channel Materials

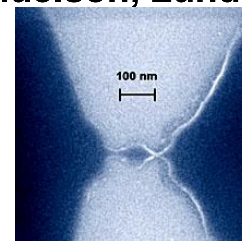
-n-Ge & p-III-V

-Nanowires



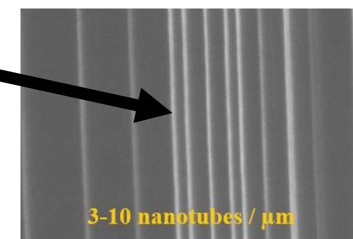
III-V Heterostructures (L. Samuelson, Lund Univ.)

-Graphene



A. Geim, Manchester U.

-Carbon Nanotubes



D. Zhou, USC

-Identify Novel Metrology & Modeling Needs

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Alternate Channel Materials Critical Assessment

Assessment Ratings						
1 = Worse than existing technologies	2 = Same as existing technologies			3 = Better than existing technologies		
Earliest Potential Insertion Date		2013-2018	2013-2018	2018-2023	2018-2023	2018-2023
Chip-Package Interconnect Metrics	Research Targets	ACM Application Opportunities and Ratings				
		p-III-V Materials	Ge [For n-channel devices]	Graphene	Nanowires [Group IV and III-V]	Carbon Nanotubes
Demonstrate co-integration on Si: Ability to achieve high performance	Mobilities: >> Scaled strained Silicon, Quasi ballistic, saturation velocity and current, Understand degradation mechanism	2.3	2.4	2.3	2.3	2.2
Gate dielectric compatibility and control	Unpinned Fermi level, 10% thickness (1s), Dit <1E11 cm-2	1.8	1.9	1.3	1.9	1.3
Low contact resistance and variability	Contact resistivity <1E9	2	1.9	1.3	1.8	1.3
Property control [Eg, Ion: Ioff, assembly/ packaging	10% (1s)	1.9	2.3	1.2	1.8	1.4
Ability to dope	Demonstrate and understand controlled n and/or p channel & S/D doping, e.g. 10% (1s)	1.9	1.8	1.4	2	1.3
Control of formation, location, and direction	CMOS compatible catalyst, as warranted, 10% of half pitch, Vertical and/or horizontal	1.9	2	1.4	1.7	1.6
Defects	Understand formation mechanism, develop low defect density strategy	1.8	1.6	1.8	1.9	1.6

- Carbon nanotubes and graphene were assessed to be less mature than other technologies.

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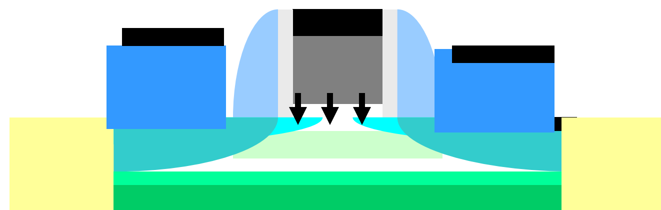
Beyond CMOS Logic Materials & Interfaces

Charge Based

Ferroelectric

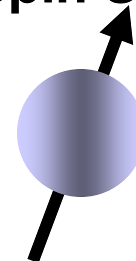
Polarization



Negative Capacitance FET

States Other Than Charge Only

Spin State



•Individual or Collective

Assess

- Ferromagnetic Materials, Dilute Magnetic Semiconductors
- Complex Metal Oxides
- Strongly Correlated Electron State Materials (FE, FM, FE & FM)
- Molecules
- Interfaces

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Lithography

Evolutionary Resist Design

-Positive Resist

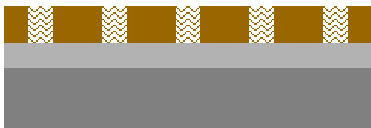
New Applications of Old Resist

Non-Chem Amp (193nm)

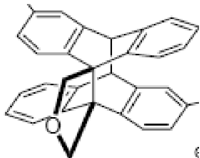
Negative Resist (EUV)

Novel Molecules

for Double Exposure



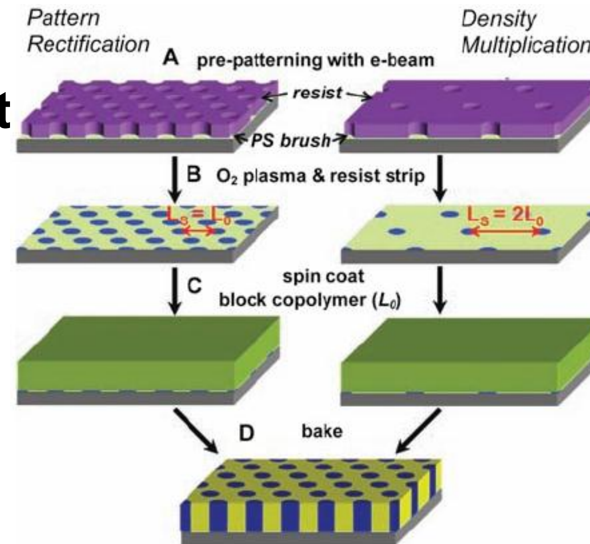
Tethered Anthracene



Bristol, Intel

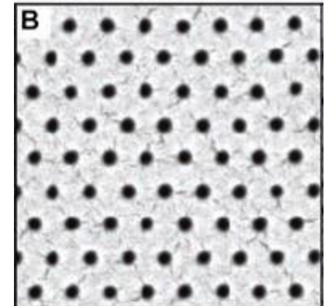
Intermediate State

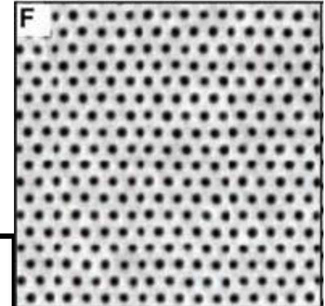
Directed Self Assembly (DSA)

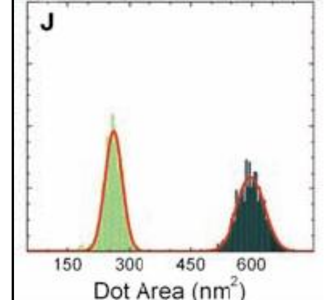


Ruiz, et. al. Science 2008

Density Multiplication L_s=78nm; L_p=39nm







DSA

- Assemble smaller features in higher density
- Defect density reduced <25cm^{-2}
- Critical Assessment completed

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Directed Self Assembly for Litho Extension Critical Assessment

	DSA Assessment Metric Targets			DSA Application Opportunities				Status
Directed Self-Assembly Metrics / Ratings *	1	2	3	LER-LWR Improvement	Contact-Via CD Improvement	Memory Array Litho	Logic Litho Extension	Demonstrated Best-In-Class[1]
L/C Defect Density (10nm defect)[2]	>0.1cm^{-2}	0.01cm^{-2}	<0.01cm^{-2}	2	1.9	1.6	1.6	< 25
CD Control (3σ): C/V/L	>1.7nm	<1.7nm	<0.8nm	2.3	2.4	2.1	2	2-Jan
Low Frequency Line Width Roughness (3σ) [nm]	>1.1nm	1.1 nm	<0.6nm	1.5	1.7	1.5	1.5	1.95
Patterning Throughput: Density multiplication	.5X	1X	2X	2.9	2.8	3	3	>2X
Annealing Time: Track or batch equivalent	>2 min.	~1 min.	<1 min.	2.5	2.9	2.4	2.4	<.5
Minimum Feature Size: L/C	>20nm/ >20nm	16nm/ 18nm	<9nm/ <10nm	3	2.9	2.9	2.9	<9/

- **Partial results of the Critical Assessment**
- **Progress demonstrated in reducing defect density**

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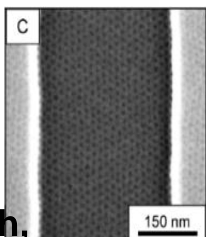
Front End Processing

Deterministic Doping Progress

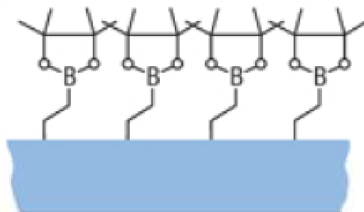
Patterning & doping via DSA



Bosworth, Ober, ACS NANO 2008

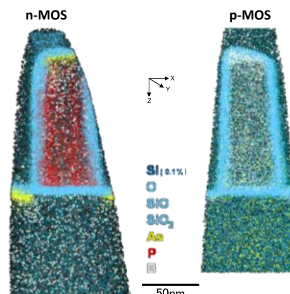
- DSA Produces Order
- Implant Delivers Dopants

Monolayer Doping



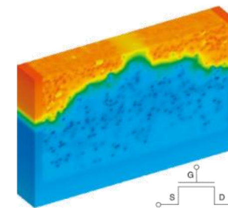
Ho, Javey, Nature Materials 2008

3D atom probe



Inoue, Ultramicroscopy 2009

3D simulation



Roy, Asenov Science 2005

Massive Parallel Dopant Control

Metrology and Modeling Progress

- **Identified potential high volume mfg. techniques**
- **Expected to be Multigate compatible**
- **Monolayer doping has potential for low temperature and low damage**

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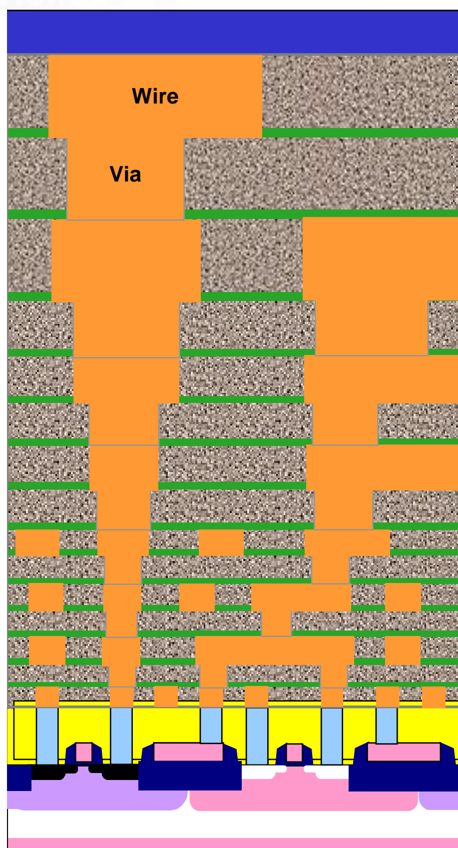
Interconnect Materials

Interconnects



Native Interconnect

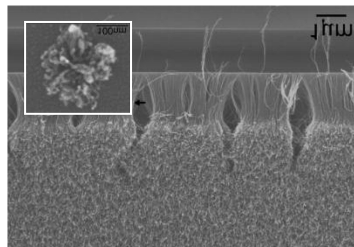
Ultra-thin Barrier Layers

- **Transition Ru Barriers to Interconnect TWG**
- **Novel sub 5nm materials**
- **Self Assembled Monolayers (SAM)**

Ultra low κ ILD

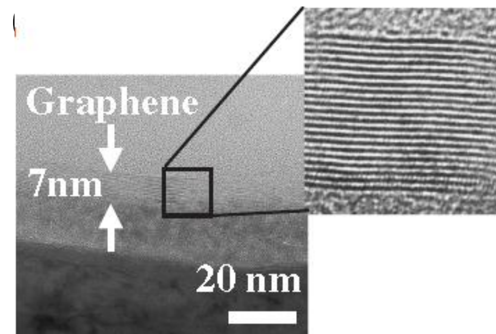
Novel Interconnects & Vias

- Carbon Nanotubes



MIRAI-Selete / TOSHIBA, APEX 3 (2010)

-Graphene



Fujitsu Lab / CREST, APEX 3 (2010)

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3D Interconnects

- Chip Attach Materials With Thermal Hierarchy
  - Electrical Interconnects
  - Nanosolders
  - Polymers
- Stress and Thermal Management Materials
- Self Aligning Material Technologies
  - Beyond surface tension…

Assembly & Package

- 1D Interconnects
  - Nanosolder, CNT & NW
- Polymers with Mechanical, Electrical & Thermal Properties
- Polymers With Zero Moisture Absorption
- Ion Free or Immune Mold Compound
- Management of III-V & Ge Device Stress

Hexagon of Assembly Material Requirements

Examples

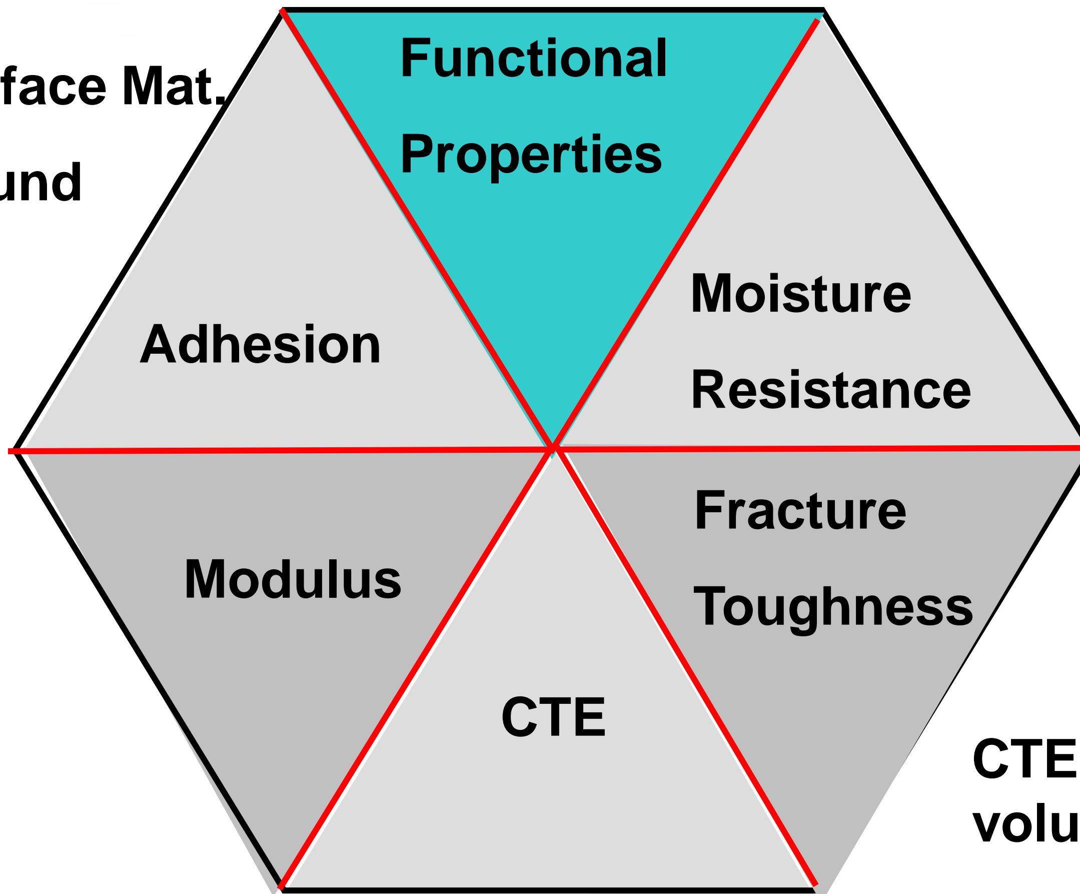
Thermal Interface Mat.

Mold Compound

Underfill

Adhesives

Epoxy



CTE depends on volume fraction

- Highly coupled Material Properties
- Apply novel materials to achieve optimal performance

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ESH Challenges

- Materials needed to overcome significant technical challenges
  - Low energy processes and new materials for low energy integrated circuits
  - Few materials can meet requirements
  - Some materials have known hazards or uncharacterized ESH properties
  - Stimulate ESH research in uncharacterized materials
  - Good risk management methods for materials ESH in Research, Development & Manufacturing
  - Lifecycle Assessment & Management
  - Efficient use of materials

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Summary

- 2011 ERM Chapter
  - Materials Progress Updated
  - Highlighted Critical Challenges
  - Identified New ITWG Requirements for ERM
  - Transitioned Mature Materials to ITWGs
  - Critical Assessments of Alternate Channel Materials and Directed Self Assembly

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Back-up