

Korea Winter Public Conference ORTC 2011 ITRS



2011 Renewal ITRS ORTC Technology Trend Pre-Summary

- 1) **Unchanged for 2010/11 MPU contacted M1**
 - 1) 2-year cycle trend through 2013; then 3-year trend to 2026
 - 2) 60f² SRAM 6t cell Design Factor
 - 3) 175f² Logic Gate 4t Design Factor
 - 4) **Ongoing - evaluate alignment of “nodes” with latest M1 industry status and also High Performance/Low Power timing needs**
- 2) **Unchanged for 2010/11 Tables: MPU Functions/Chip and Chip Size Models**
 - 1) Design TWG Model for Chip Size and Density Model trends – tied to technology cycle timing trends and cell design factors
 - 2) ORTC line item OverHead (OH) area model, includes non-active area
- 3) **Updated for 2010/11 Tables: MPU GLpr, GLph – trends “smoothed” by PIDS modeling; but close to previous targets**
- 4) **Updated for 2010/11 Tables: Vdd Low operating and standby line items from PIDS model track “smoothed” gate length changes**
- 5) **Added in 2011 – Table ORTC-6 Battery Energy Storage (Watt-hours) Line Item from iNEMI Roadmap**



2011 Renewal ITRS ORTC Technology Trend Pre-Summary (cont.)

- 6) Updated in ORTC 2011 Tables - DRAM contacted M1:
 - 1) 1-year pull-in of M1 and bits/chip trends;
 - 2) no Flattening of DRAM M1 as with Flash Poly**
 - 3) 4f2 push out [to 2013];
- 7) Updated in ORTC 2011 Tables - Flash Un-contacted Poly:
 - 1) 2+-year pull-in of Poly; however slower 4-year cycle (0.5x per 8yrs) trend to 2020/10nm; then 3-year trend to 2022/8nm; then Flat Poly after 2022/8nm;
 - 2) and 3bits/cell extended to 2018; 4bits/cell delay to 2022
- 8) Updated in ORTC 2011 Tables - DRAM Bits/Chip and Chip Size Model:
 - 1) 3-year generation “Moore’s Law” bits/chip doubling cycle target (1-2yr delay for smaller chip sizes <30mm² – 2x/2.5yrs)
- 9) Updated in ORTC 2011 Tables - Flash Bits/Chip and Chip Size Model:
 - 1) 3-year generation “Moore’s Law” bits/chip doubling cycle target (after 1-yr acceleration; then flat @ 1-2Tbits; keep chip size <160mm²);
 - 2) New 3D layers Models vs. relaxed half-pitch tradeoffs are now included in the 2011 Renewal for maximum bits per chip

2011 Renewal ITRS ORTC Technology Trend Pre-Summary (cont.)

10) Updated in ORTC 2011 Tables - ORTC Table 5 - Litho # of Mask Counts MPU, DRAM,

- 1) Flash Survey inputs Updated
- 2) Also IC Knowledge (ICK) model contribution to extend mask levels range

11) Unchanged for 2011 - IRC 450mm Position:

- 1) Timing Status
 - 1) Consortia work underway
 - 2) IDM and Foundry Pilot lines: 2013-14;
 - 3) Production: 2015-16
- 2) SEMATECH/ISMI making good progress on 450mm program activities to meet the ITRS Timing
 - 1) Consortium operations are using 450mm early test wafer process, metrology and patterning capability to support Supplier development
 - 2) 193 immersion multiple exposure litho tools are under development to support consortium and manufacturers' schedules
 - 3) 450mm increasing silicon demand is needed from consortium demonstrations to support development
- 3) Europe momentum building - EEMI status reviewed with IRC in Potsdam
- 4) FI TWG will extend 300mm wafer generation in parallel line item header with 450mm;
 - 1) Including Technology upgrade assumptions through end of roadmap
 - 2) Assuming compatibility of 300mm productivity extensions into the 450mm generation;
- 5) Utilizing a new ITRS-based ICK Strategic commercial model , SEMATECH has developed 300mm and 450mm 2009-2024 Range Scenarios for silicon and equipment demand

12) Updated in 2011 - More than Moore white paper online at www.itrs.net

- 1) New "Moore's Law and More" Graphic update included in 2011 ITRS Executive Summary
- 2) MtM Workshop completed in Potsdam, GE, in April and reviewed at Summer ITRS meeting
- 3) New MEMS TWG and Chapter added to 2011 ITRS



2011 Renewal ITRS ORTC Technology Trend Summary (cont.)

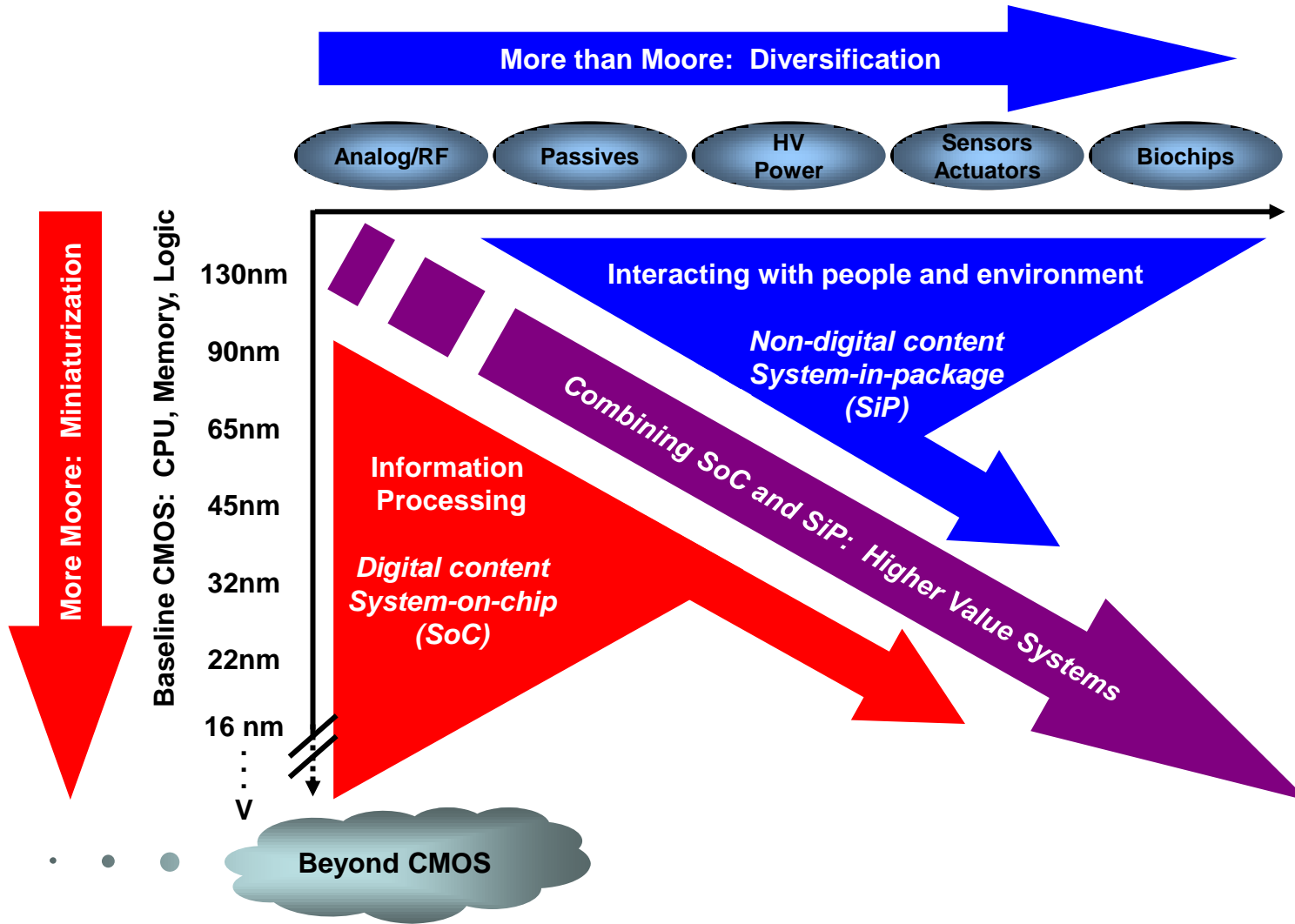
Technology Pacing Cross-TWG Study Group (CTSG) work preparation for 2012 Update:

- **IRC Equivalent Scaling Graphic Update**
 - Included in 2011 Update: Parallel bulk and SOI pathways; and Clarification of gate mobility materials pathway
 - Proposals for pull-in placement of MuGFET [2012 Update work] and III/V Ge Timing [consider in 2013 ITRS work] (one IDM or Foundry company may lead technology production ramp)
- **PIDS and FEP Memory Survey Proposal Updates**
 - Additional acceleration will be monitored
- **FEP and Design and System Drivers Logic Monitor**
 - Monitor MPU and Leading Edge Logic technology trends
- **A&P/Design Power Model**
 - Possible proposals for Power Dissipation "hot spot" model rather than chip area basis
- **PIDS/Design Max On-chip Frequency vs Intrinsic Modeling**
 - Included in 2011 Update: New Max Chip Frequency trends (reset to 3.6Ghz/2010 plus 4% CAGR trend)
 - TBD PIDS Intrinsic Transistor and Ring Oscillator model Changes to 8% [from unchanged 2011 13% trend]
 - PIDS Updates include MASTAR static modeling near-term and TCAD dynamic long-term modeling
 - Also “equivalent scaling” tradeoffs (FDSOI, MuGFET, III-V/Ge) with dimensional scaling
- **YE Defect Density Modeling**
 - New ORTC Defect Density model work moved to 2012 Update due to loss of modeling resources



Figure 4

The Concept of Moore's Law and More



Source: 2011 ITRS - Exec. Summary Fig. 4



Exec. Summary - Figure 1 Definition of Half-Pitch

More Poly Dense Lines added in 2010 ITRS Update

[Note: **The ITRS does not utilize any single-product “node” designation reference**; Flash Poly and DRAM M1 half-pitch are still Lithography drivers; however, other product technology trends may be drivers on individual TWG tables]

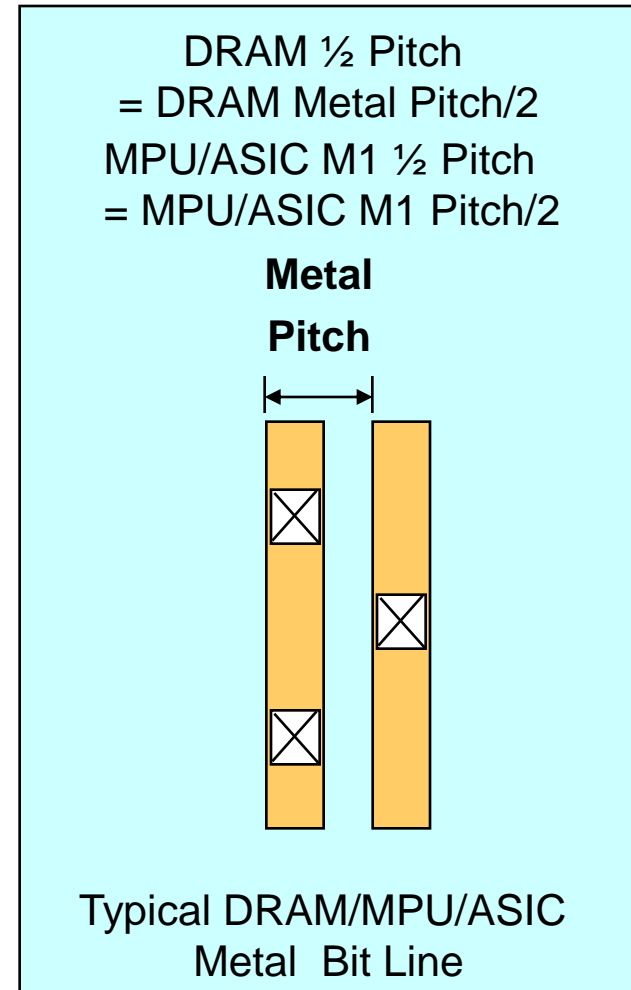
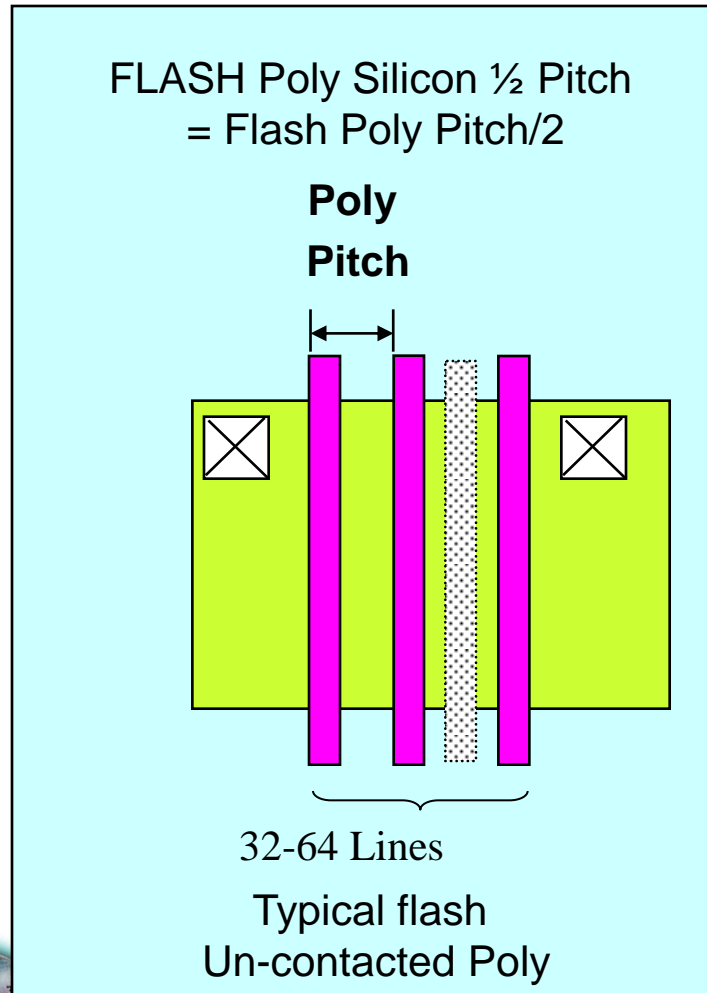
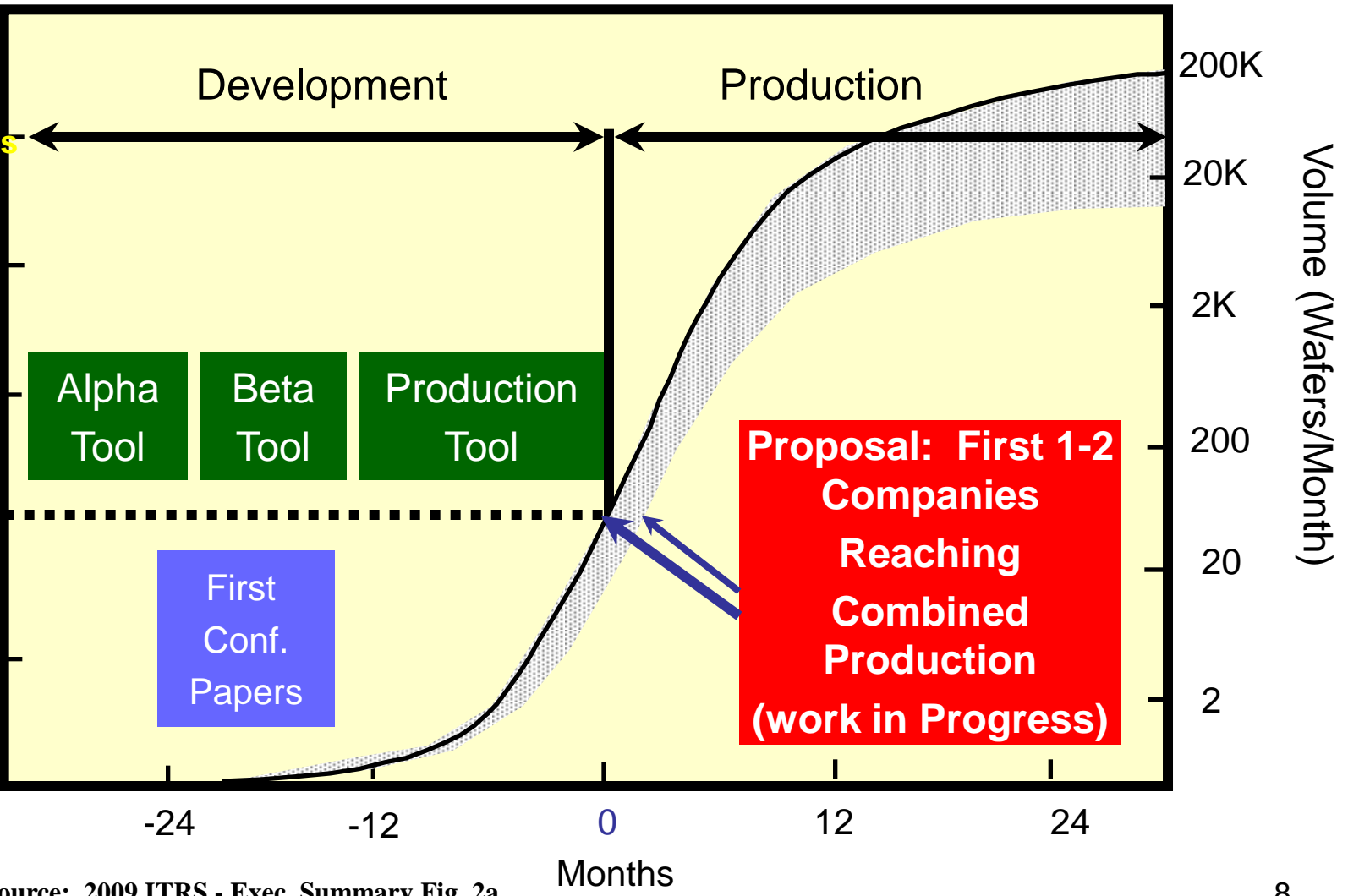


Figure 2a Production Ramp-up Model and Technology/Cycle Timing

- (within an established wafer generation*)
- *see also Figure 2a for ERD/ERM Research and PIDS Transfer timing; and also
- Figure 6 (450mm topic) for Typical Wafer Generation Pilot and Production "Ramp Curves"

Proposal For 2012 Update Note:
 Fewer leading IDM Companies Requires Adaption of Definition To allow one IDM Company Or a Foundry Representing Many Fabless Companies To Lead a Technology Production Ramp Timing

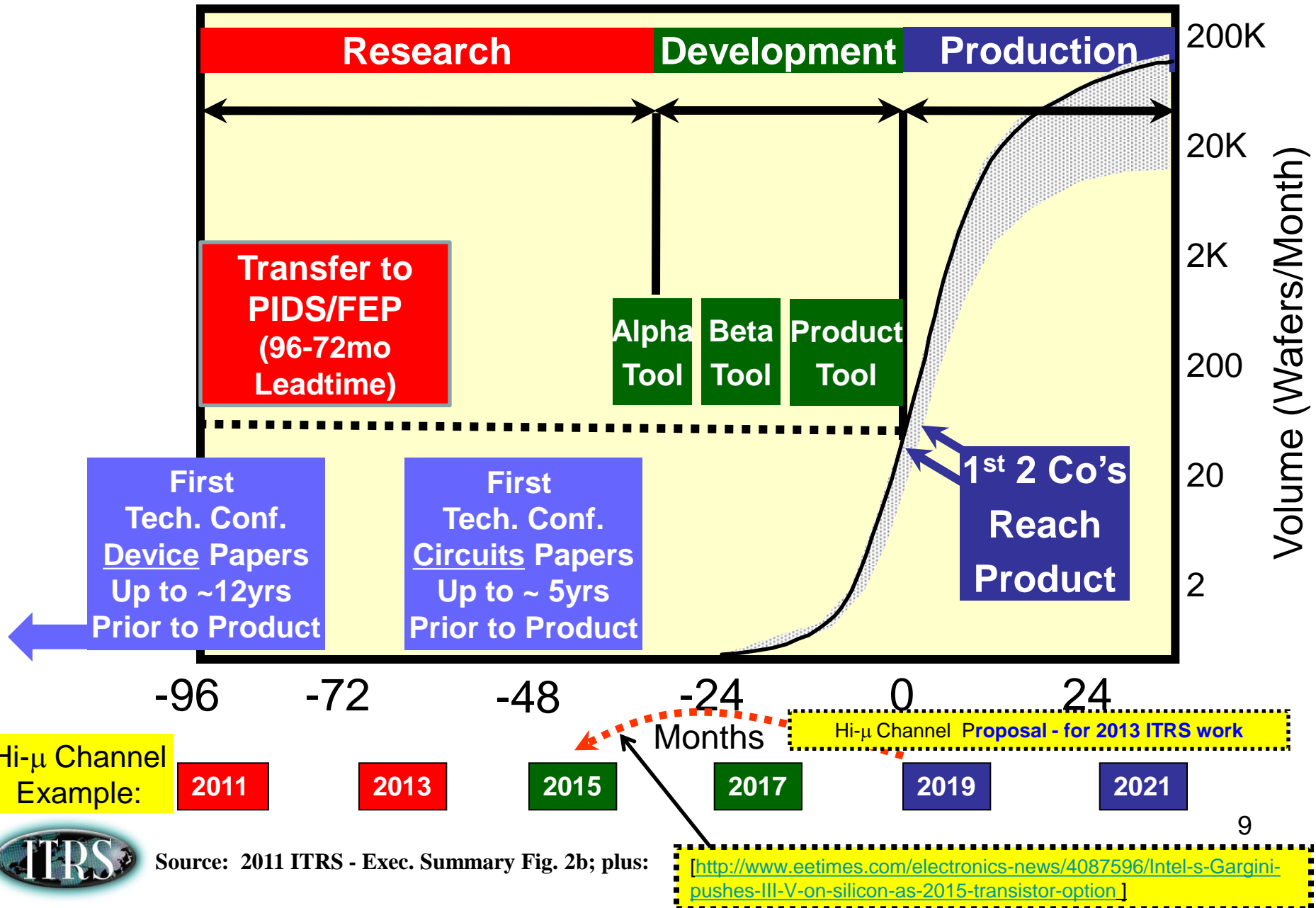


Source: 2009 ITRS - Exec. Summary Fig. 2a



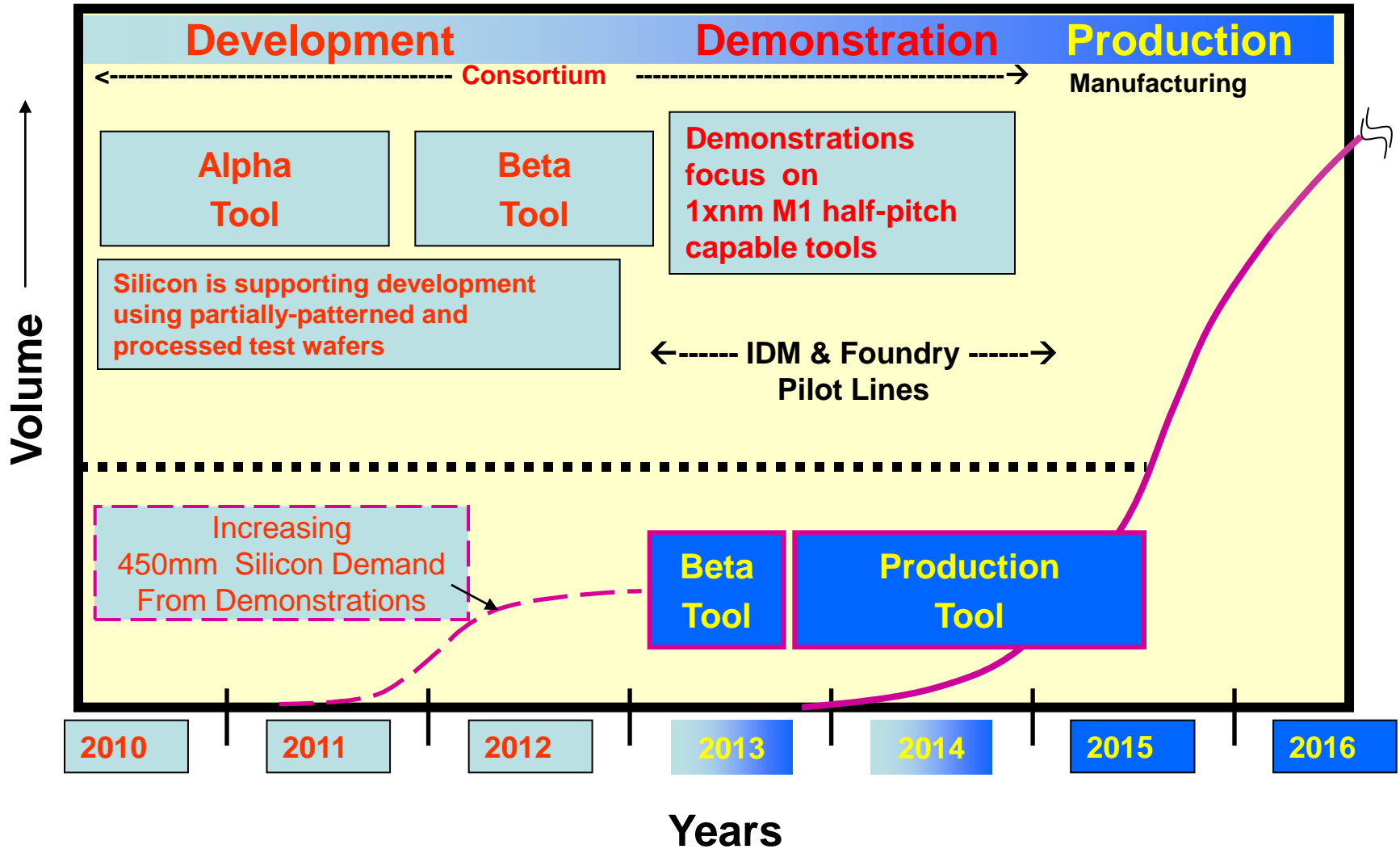
Work in Progress - Do Not Publish

Figure 2b A Typical Technology Production “Ramp” Curve for ERD/ERM Research and PIDS Transfer timing
 - including an example for III/V Hi-Mobility Channel Technology Timing Scenario
 - **Acceleration to 2015 Scenario for the 2012 Update work**



2012 ITRS Update* 450mm Production Ramp-up Model

[2011 ITRS Executive Summary Fig. 6 - A Typical Wafer Generation Pilot Line and Production "Ramp" Curve]



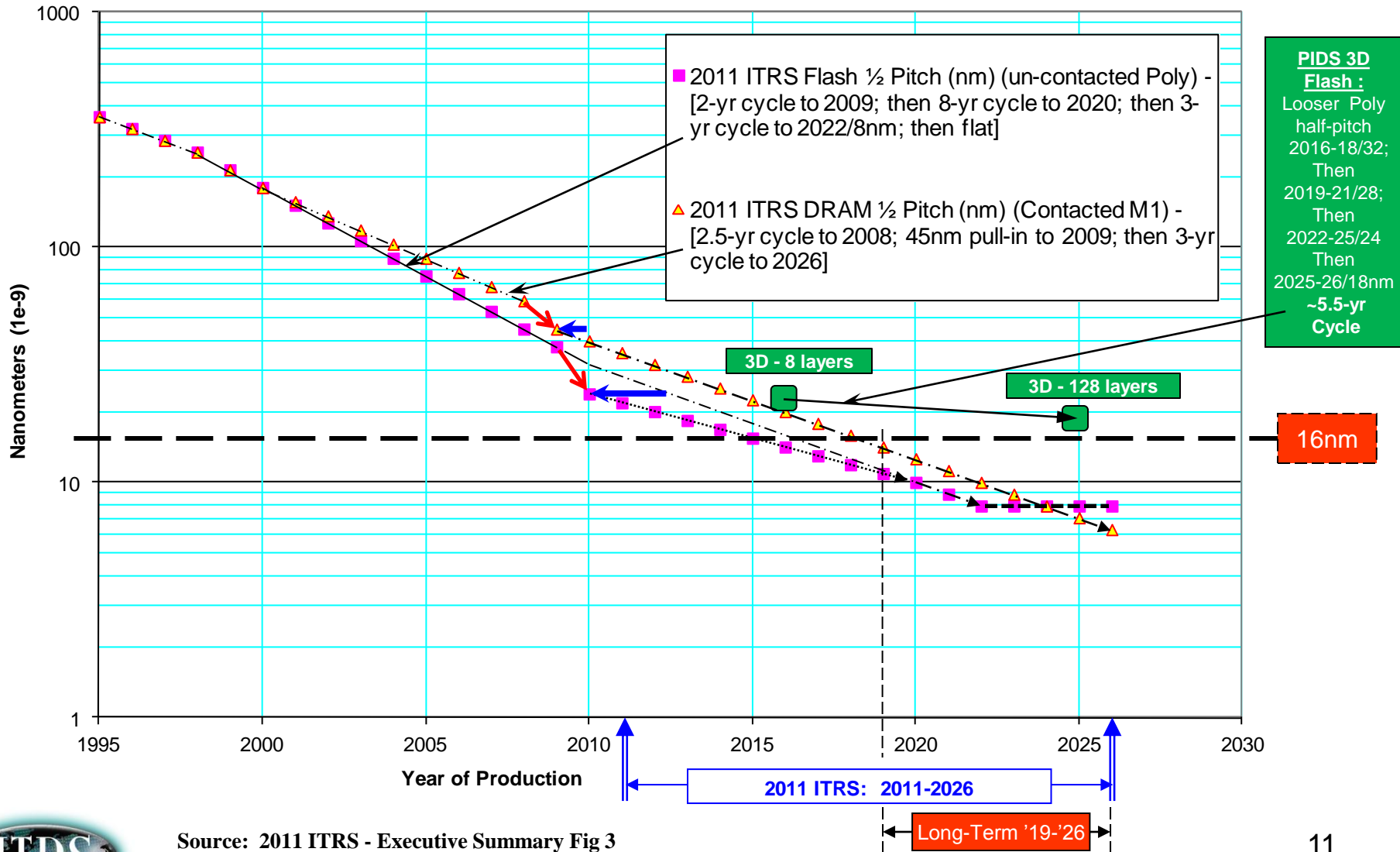
*Note: the IRC recommended updating the ITRS 450mm Timing Graphic for use in the 2011 ITRS Special Topic and 2012 Update Roadmap guidance; based on SEMATECH guidance

Source: 2011 ITRS - Executive Summary Fig. 6



2011 ITRS **Figure 11** – ORTC Table 1 Graphical Trends – Memory Half Pitch [With 2011 Flash 3D Scenario Overlay]

2011 ITRS - Technology Trends

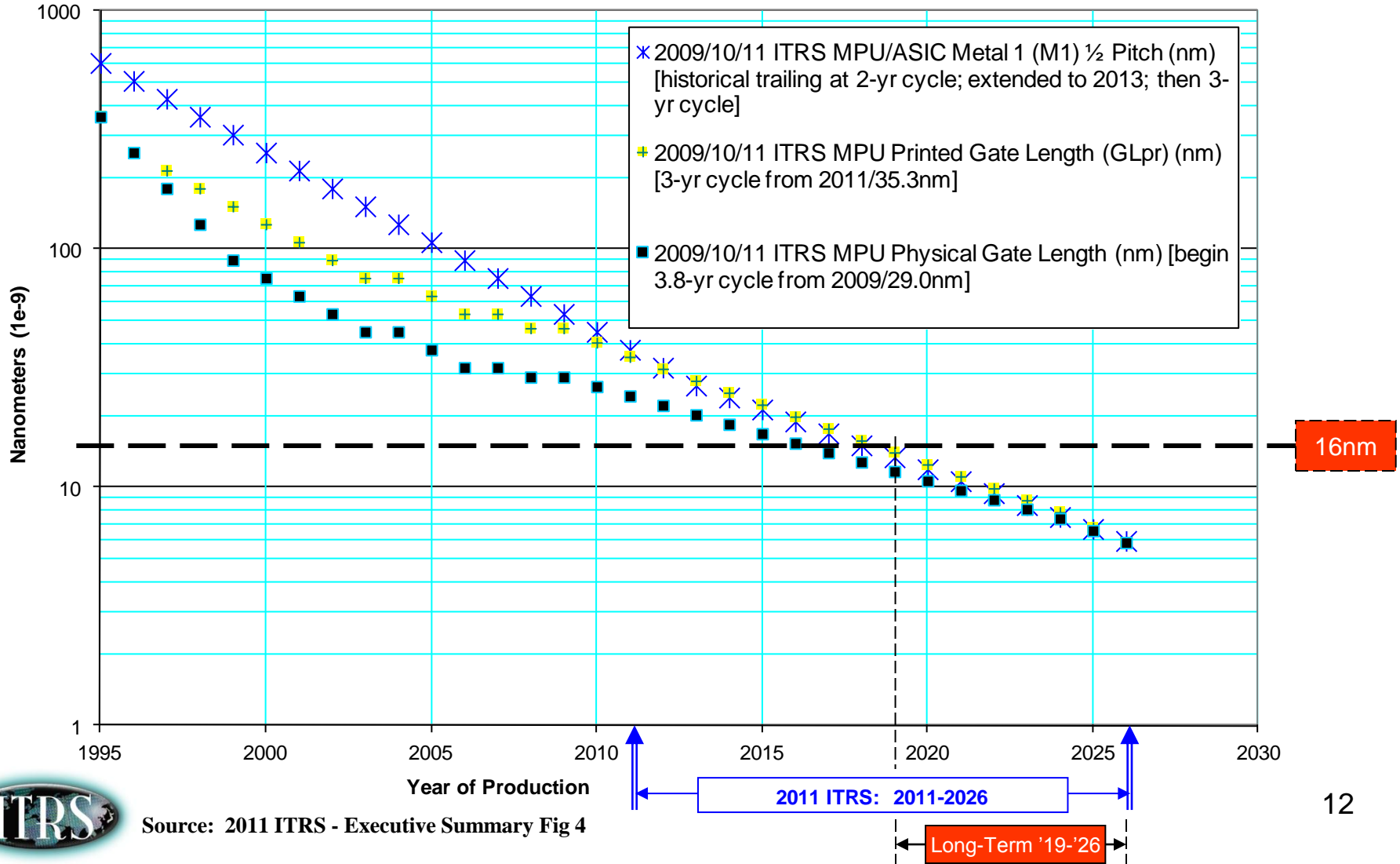


Source: 2011 ITRS - Executive Summary Fig 3



2011 ITRS **Figure 4** – ORTC Table 1 Graphical Trends – Logic (MPU and high-performance ASIC) Half Pitch and Gate Length

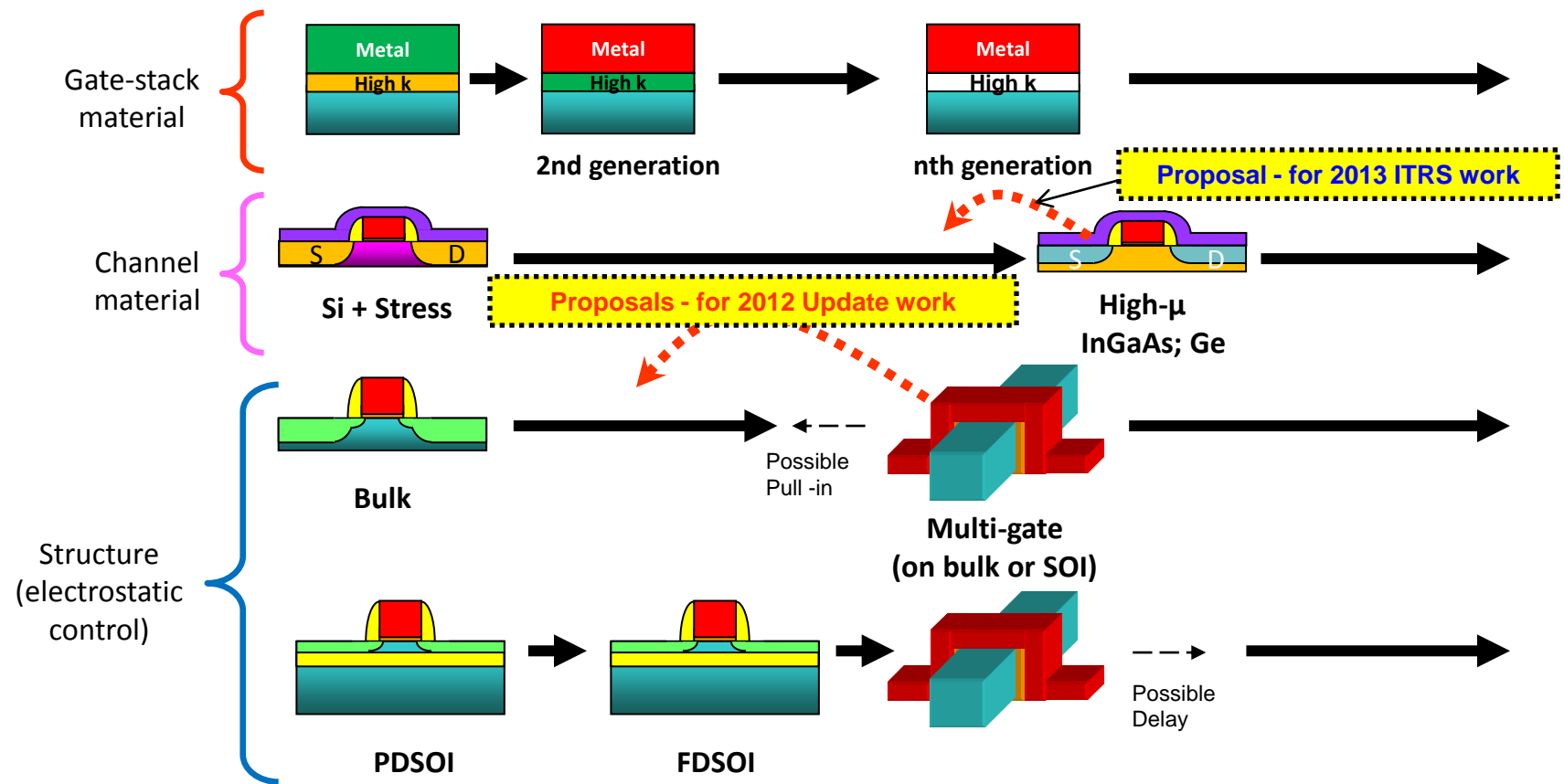
2011 ITRS - Technology Trends



Source: 2011 ITRS - Executive Summary Fig 4

2011 ITRS **Figure 5** “Equivalent Scaling” Roadmap for Logic (MPU and high performance ASIC)

Figure 5 ORTC Table 1 Graphical Trends (including overlay of 2009 industry logic “nodes” and ITRS trends for comparison); also including proposals for MugFET and III/V Ge acceleration **for 2012 ITRS Update work**



2011 ITWG Table Timing:	2007		2010		2013		2016		2019	2021	2024
2011 ITRS Flash Poly :	54nm	45nm	2009 32nm	22nm	2012 32nm		15nm		2018 11nm	2021 11nm	2024 8nm
2011 ITRS DRAM M1 :	68nm		45nm		32nm		22nm		16nm		8nm
MPU/hpASIC “Node”:	“45nm”	“32nm”	“22nm”	“16nm”		“11nm”		“8nm”			
2011 ITRS MPU/hpASIC M1 :	76nm	65nm	54nm	45nm	38nm	32nm	27nm		19nm	13nm	
2011 ITRS hi-perf GLpr :	54nm	47nm	47nm	41nm	35nm	31nm	28nm		20nm	14nm	
2011 ITRS hi-perf GLph :	32nm	29nm	29nm	27nm	24nm	22nm	20nm		15nm	12nm	



2011 ITRS Figure 4 – ORTC Table 1 Graphical Trends – Logic (MPU and high-performance ASIC) Half Pitch and Gate Length

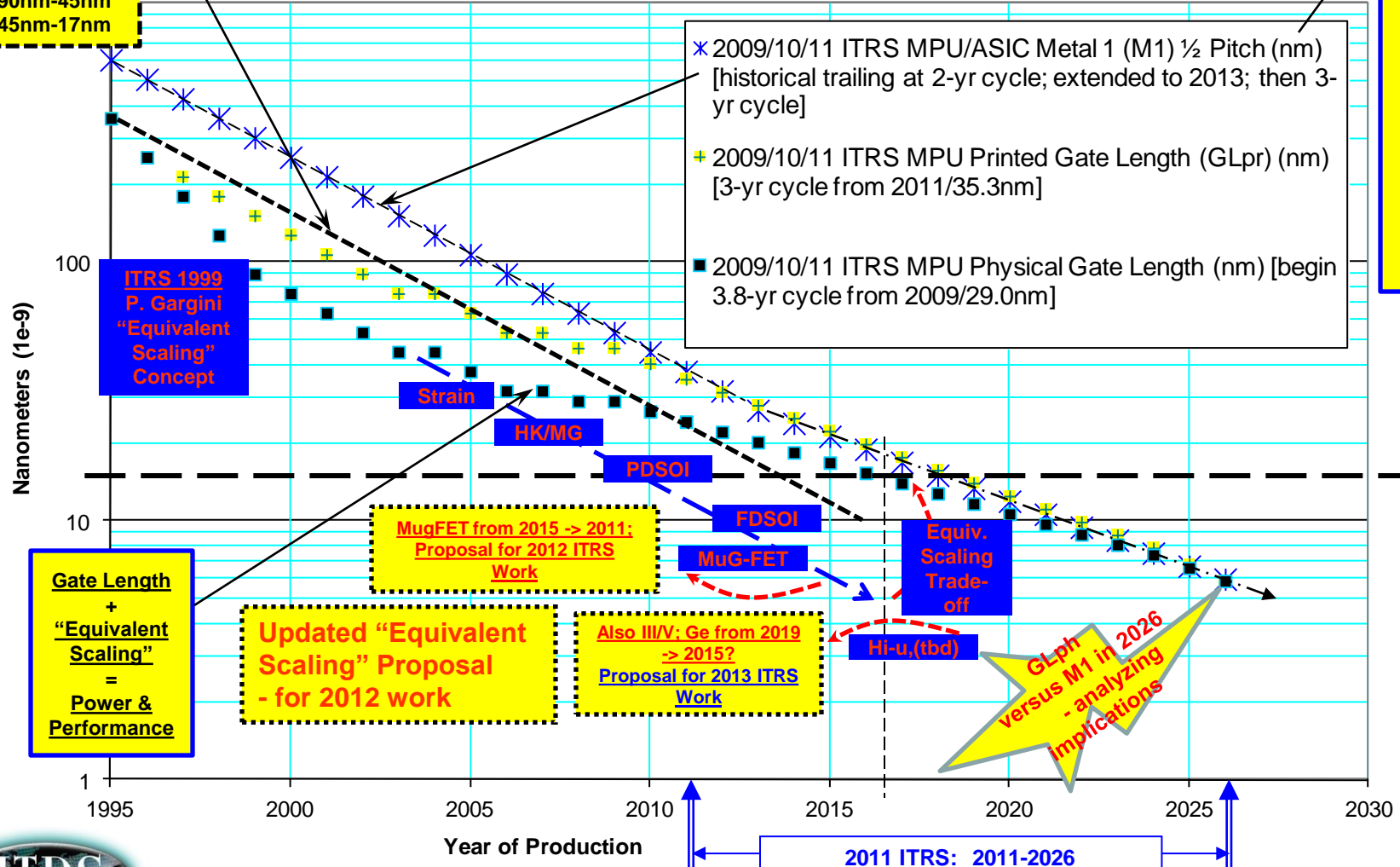
2009/2010 ITRS Unchanged (except extend to new end period): 2011 ITRS: 2011-2026; also includes 2012 Update “Equivalent Scaling” Proposals

2011 ITRS - Technology Trends

1995->2015
“Nodes”
“360-11(10)”

ITRS M1 hp
303-21nm

ITRS GLph
'95-'99-'03-'15
360nm-90nm
90nm-45nm
45nm-17nm

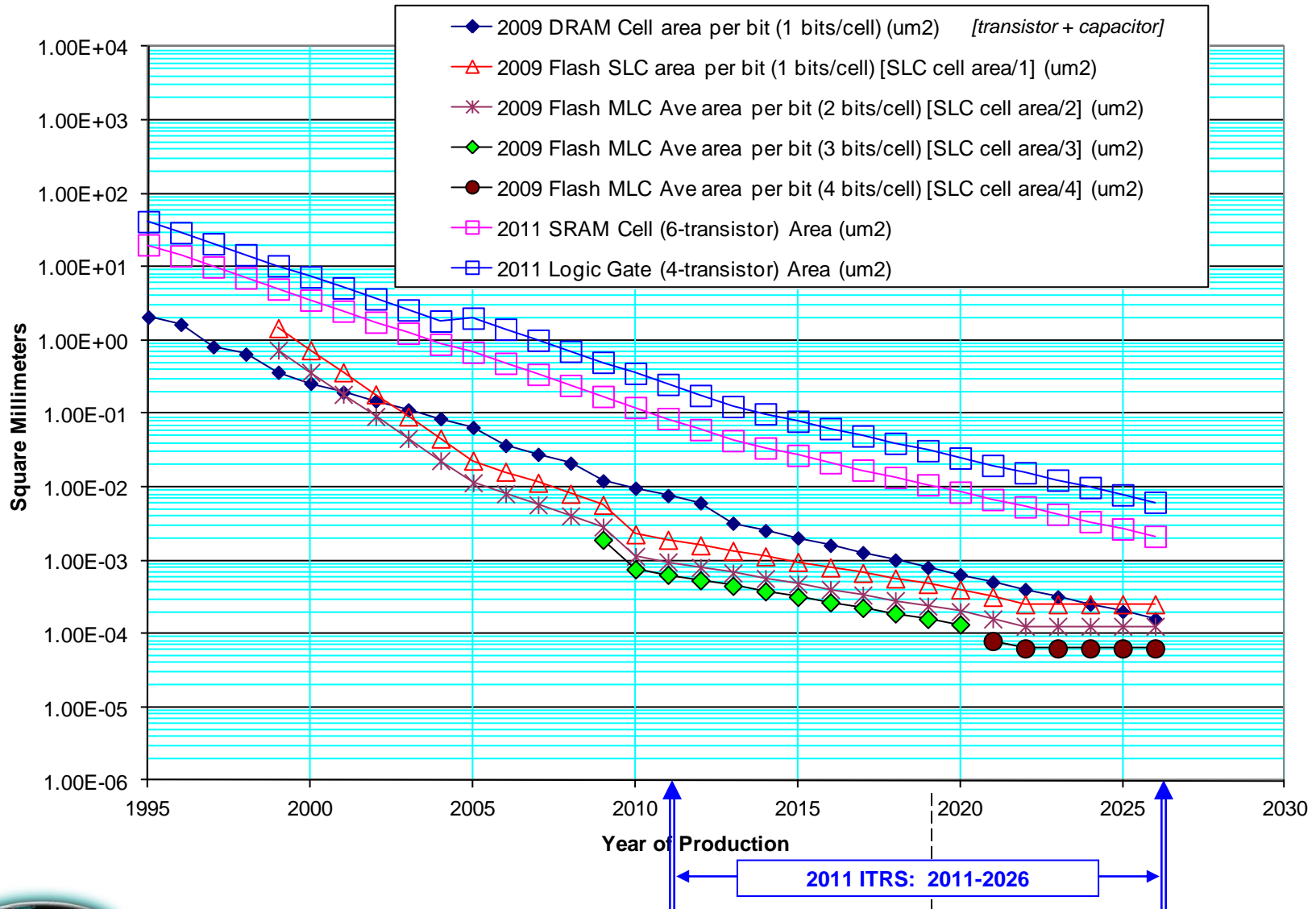


Source: 2011 ITRS - Executive Summary Fig 4



2011 ORTC Figure 6 Product Function Size Trends

2011 ITRS - Function Size



Source: 2011 ITRS - Executive Summary Fig 6



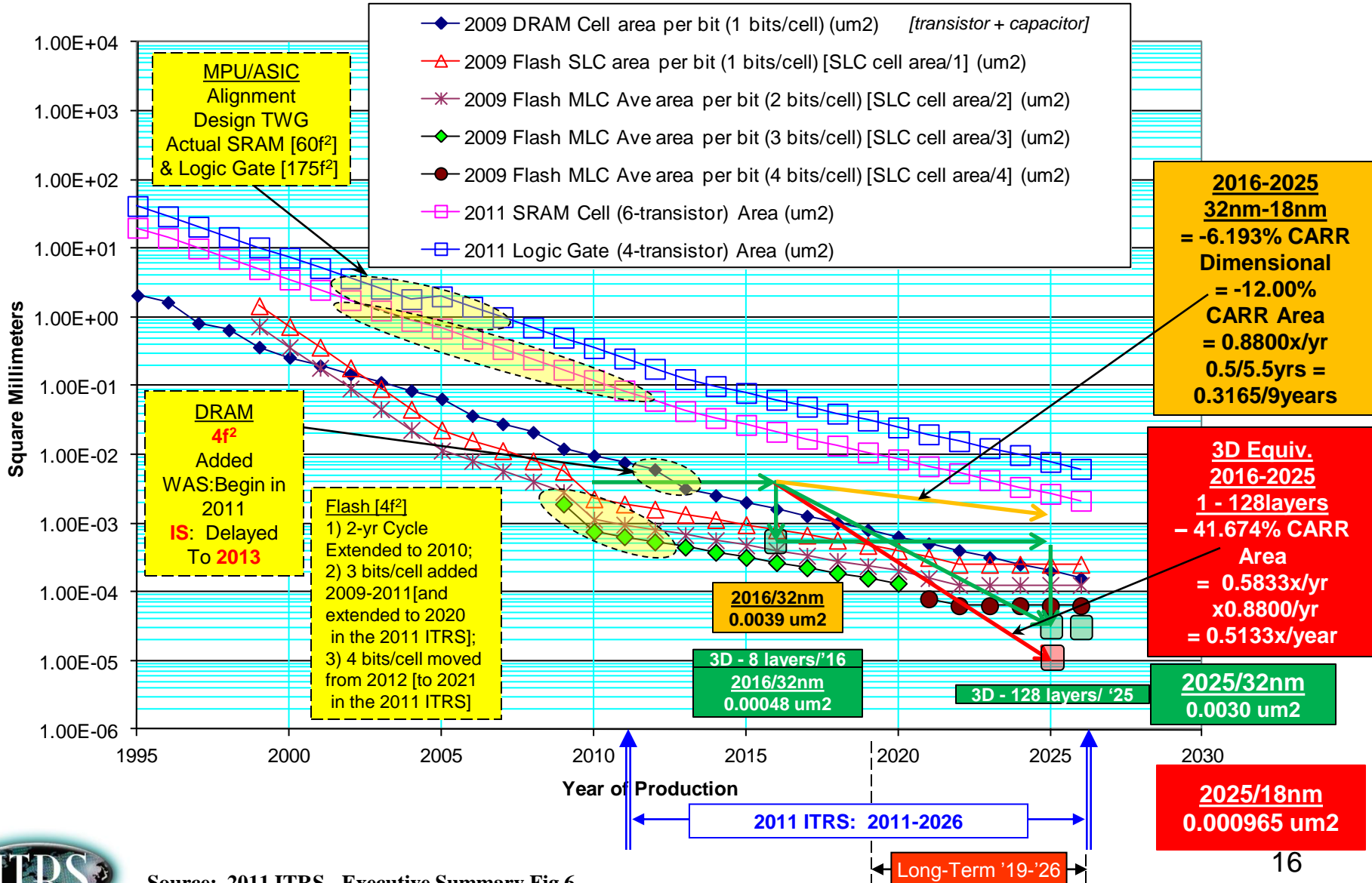
Long-Term '19-'26

2011 ORTC Figure 6 Product* Function Size Trends; plus

PIDS NAND Flash Multi-Layer 3D Model

Plus "Shallow" Dimensional Reduction Rate Trend

2011 ITRS - Function Size



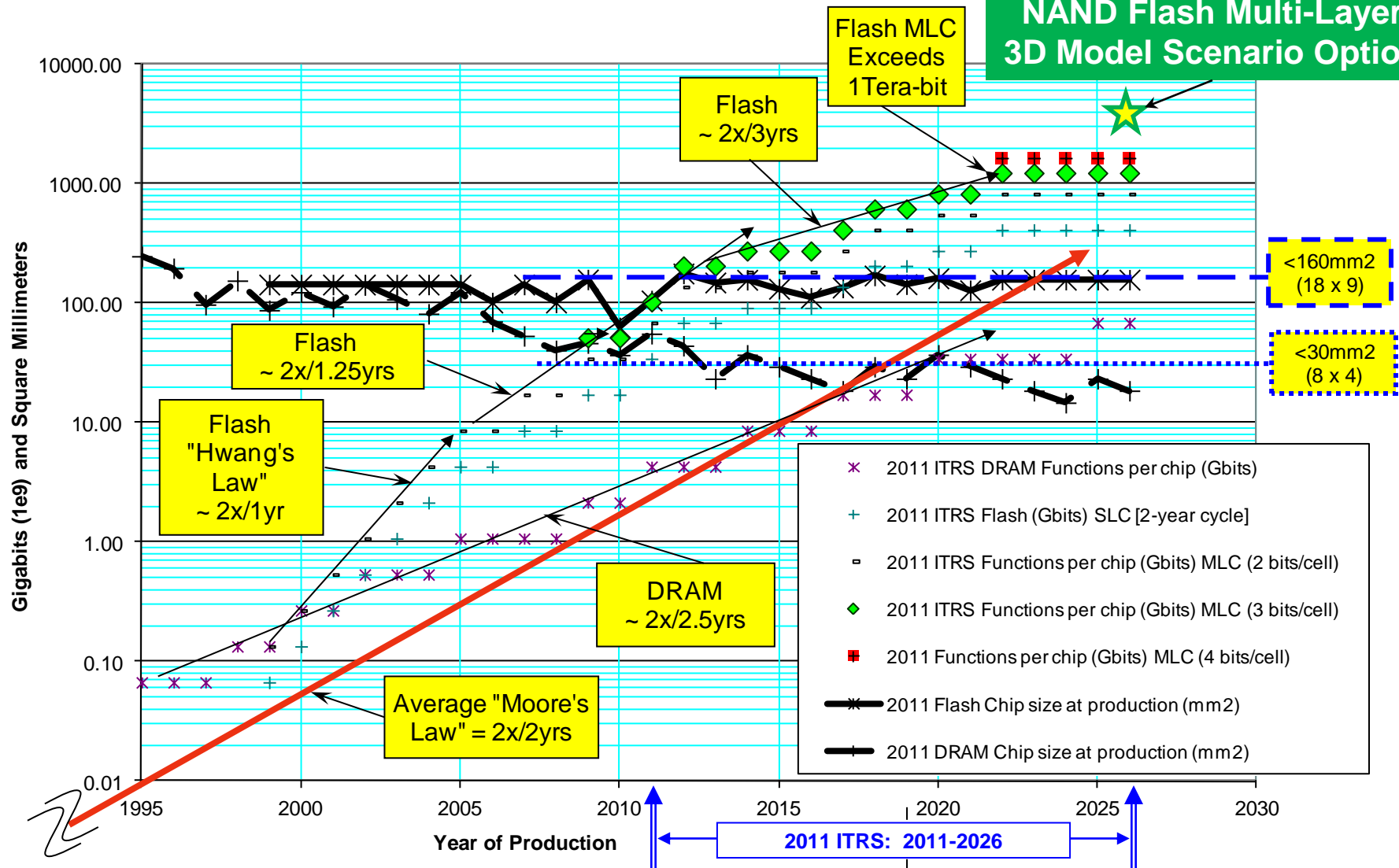
Source: 2011 ITRS - Executive Summary Fig 6



Figure 7 2011 ITRS Product Technology Trends: Memory Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

2009 ITRS - Functions/chip and Chip Size

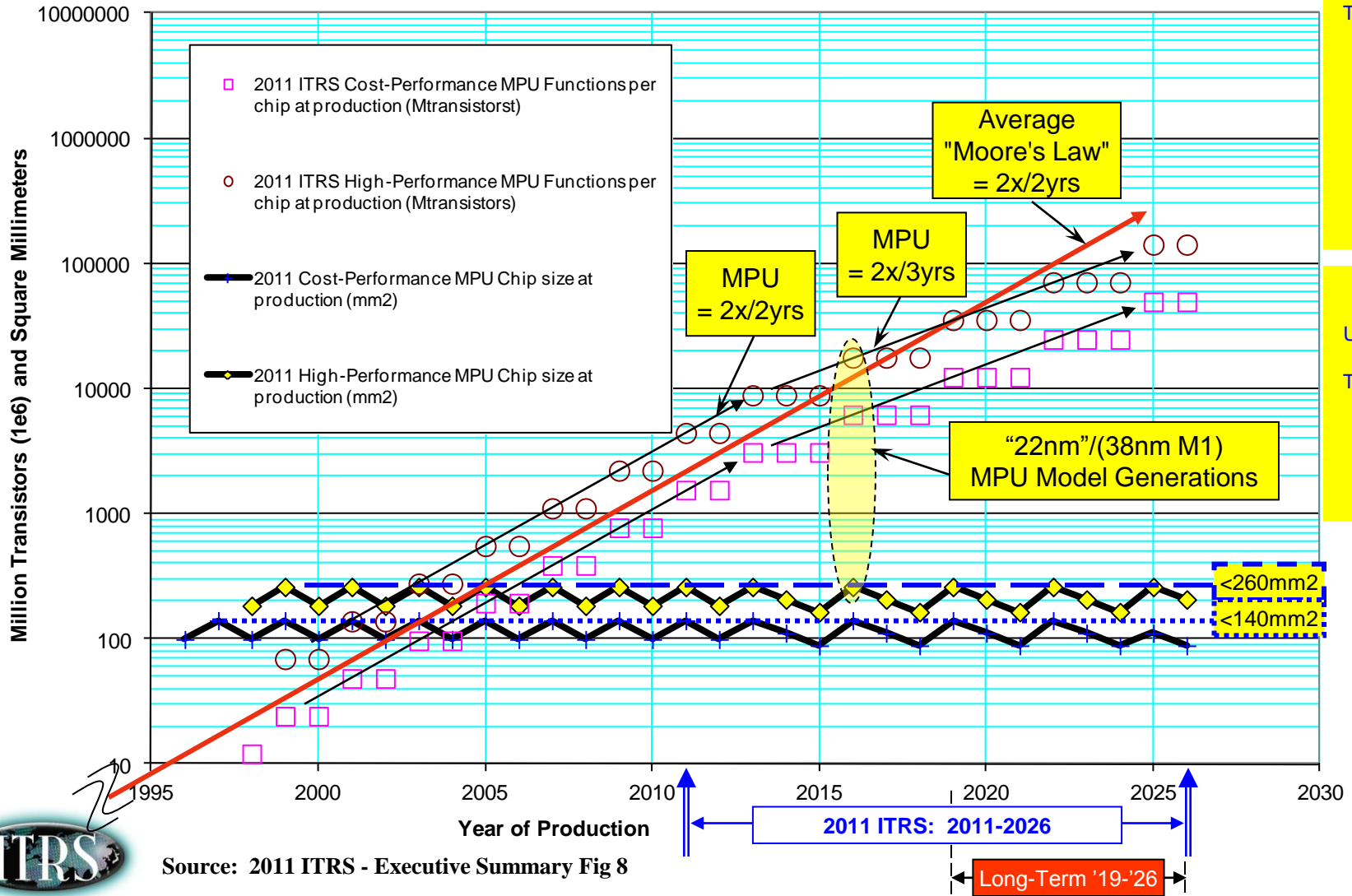
4Tbits Possible with PIDS NAND Flash Multi-Layer 3D Model Scenario Option



Source: 2011 ITRS - Executive Summary Fig 7

Figure 8 2011 ITRS Product Technology Trends: MPU Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends
[unchanged from 2009, except extended to 2026]

2011 ITRS - Functions/chip and Chip Size



MPU/hpASIC
M1 Technology
Cycle and MPU
Transistors/chip
are
**On 3-year
Cycle
after 2013**
vs.
**Average
2-year
Historical
Moore's Law**

**2011
ITRS:**
Unchanged, but
Extend ed
Transistors/chip
& Chip Size
Models
to 2026
**On 3-year
Cycle**

Source: 2011 ITRS - Executive Summary Fig 8



ORTC Table 5 Update: Litho TWG model for Mask Count

- MPU survey-based, mask counts peak 2014/(54 masks peak) EUV expected 2015
- DRAM referenced to MPU, mask counts peak 2012/(41 masks peak) EUV expected 2013
- Flash survey-based, mask counts peak 2012/(43 masks peak) EUV expected 2013
- Sidewall image transfer technology IEDM papers should be evaluated
- Table 5 also includes NEW IC Knowledge (ICK) www.icknowledge.com modeled comparison targeting ITRS 2011 Litho EUV timing; but extended out through 2024 using 2009-10 ITRS (www.itrs.net) assumptions
- **Limited YE Defect Density modeling resources requires delay of update response to 2012 ITRS Update work**

Fig 7a - Litho 2011 Survey vs ICK 2011 ITRS-based* Model

[*extended to 2024 based on 2009-24 ITRS www.itrs.net]

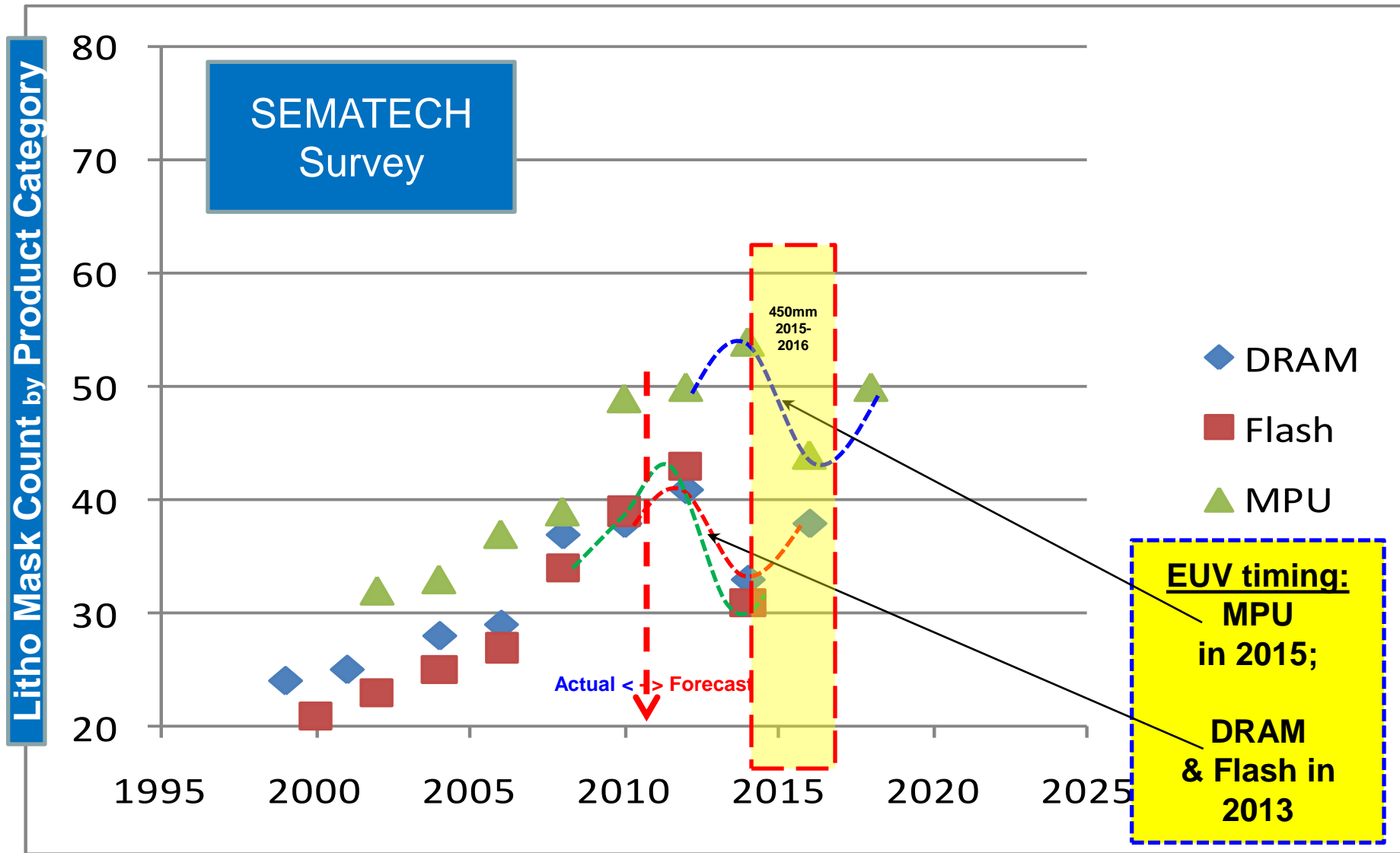
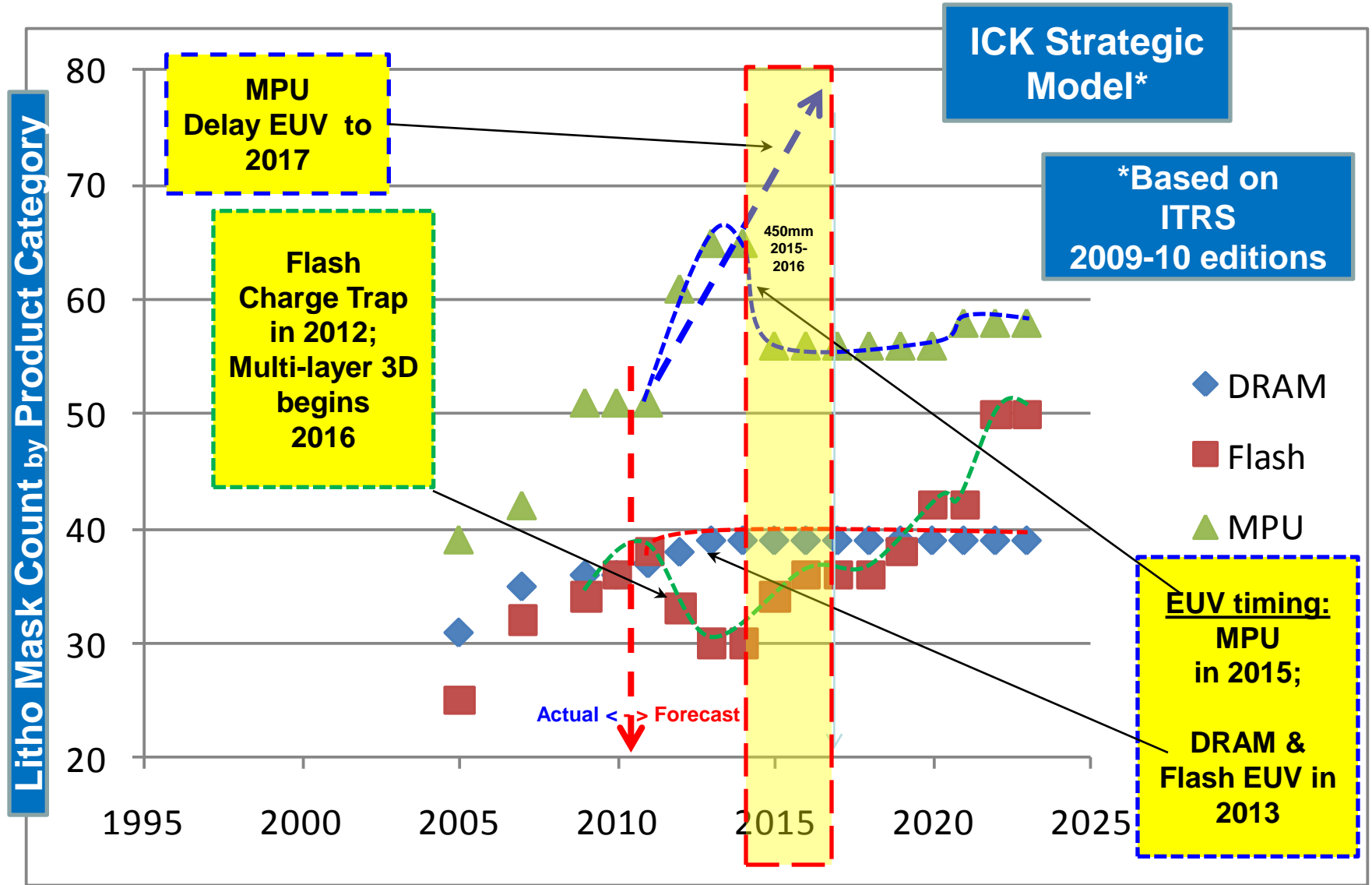


Fig. 7b - Litho 2011 Survey vs ICK 2011 ITRS-based* Model (cont.)

[*extended to 2024 based on 2009-24 ITRS www.itrs.net]



Source: 2011 ITRS - Executive Summary Fig. 7b



Table FreqTopic tbd - 2011 Chip Frequency Model Trend vs.2009/2010 ITRS Frequency

Table ORTC-4 Performance and Packaged Chips Trends

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Chip Frequency (MHz)																		
On-chip local clock [2]	5.454	5.875	6.329	6.817	7.344	7.911	8.522	9.180	9.889	10.652	11.475	12.361	13.315	14.343	15.451	16.640		
On-chip local clock [2]	<u>3.462</u>	<u>3.600</u>	<u>3.744</u>	<u>3.894</u>	<u>4.050</u>	<u>4.211</u>	<u>4.380</u>	<u>4.555</u>	<u>4.737</u>	<u>4.927</u>	<u>5.124</u>	<u>5.329</u>	<u>5.542</u>	<u>5.764</u>	<u>5.994</u>	<u>6.234</u>	<u>6.483</u>	<u>6.743</u>

ORTC Table 4: Design TWG Model for On-Chip Frequency

- Lower model starting point 2010/3.6Ghz
- 4% growth rate through 2026
- *Unchanged 2011 ITRS 13% PIDS target model Intrinsic Transistor Frequency Growth;
- ***However, proposal for 2012 ITRS 8% PIDS target model Intrinsic Transistor Growth (work preparation in 2011)**



Fig 8a - PIDS 2009/11 ITRS CV/I Trends vs. 2012 ITRS MUG-FET 4-year Pull-In and Lower Intrinsic Freq. Trend Proposals

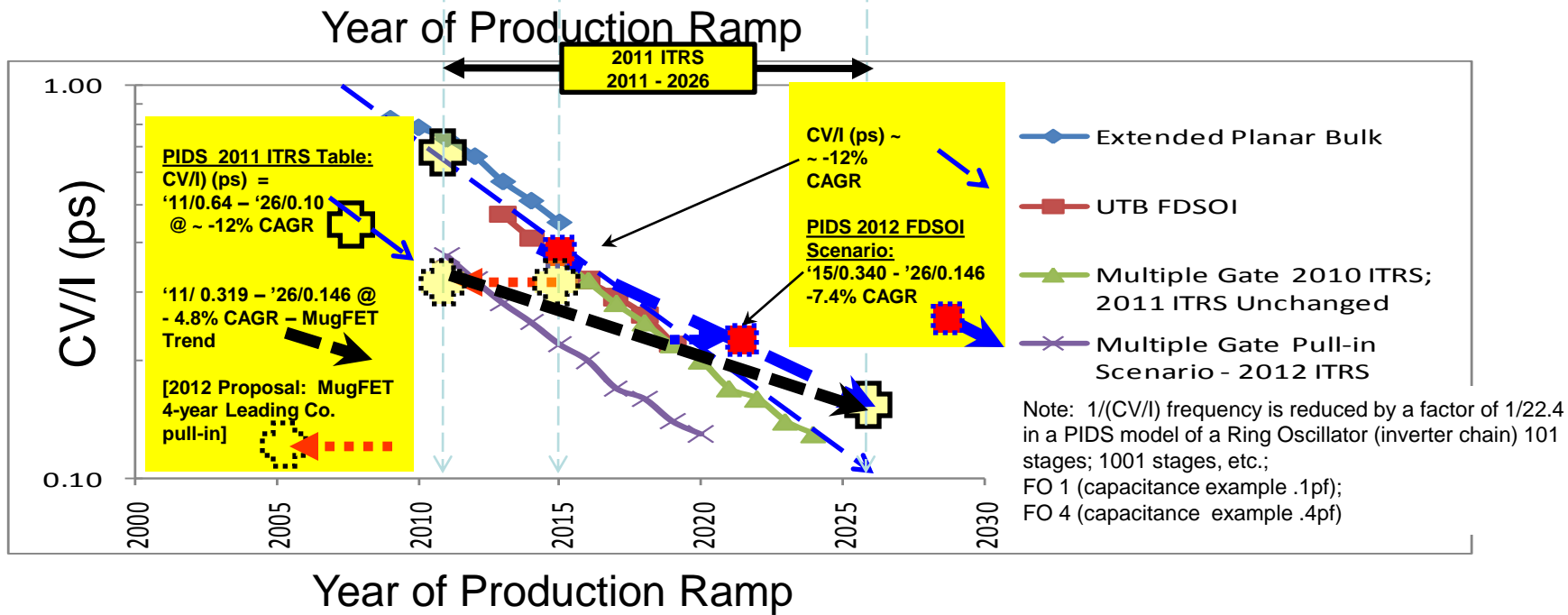
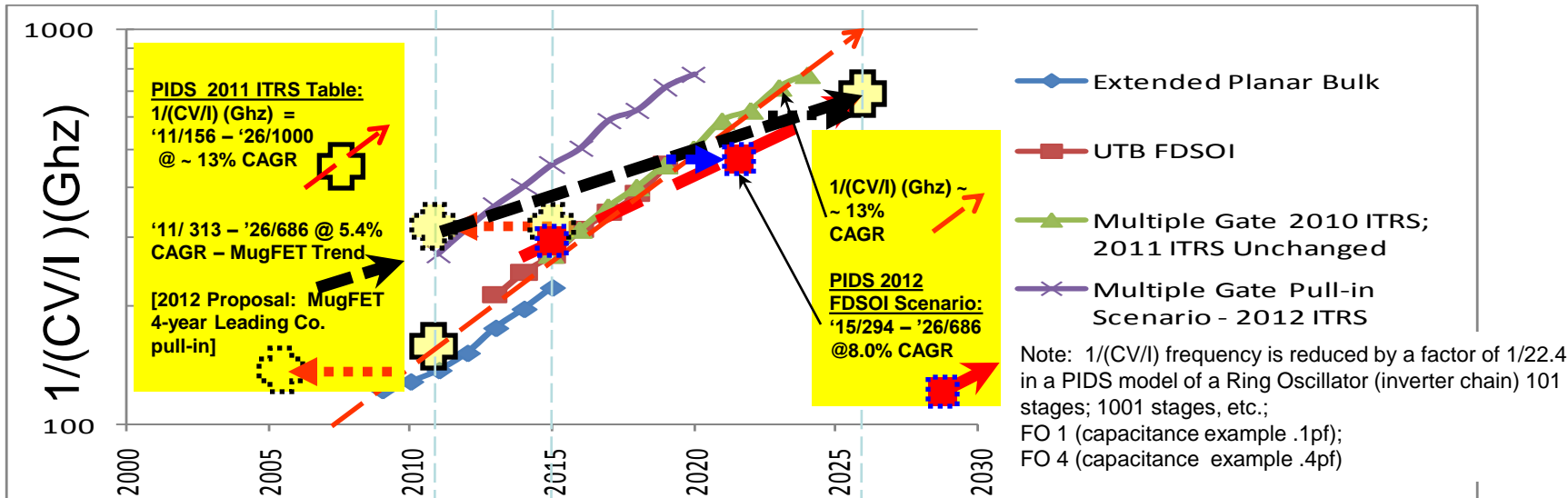
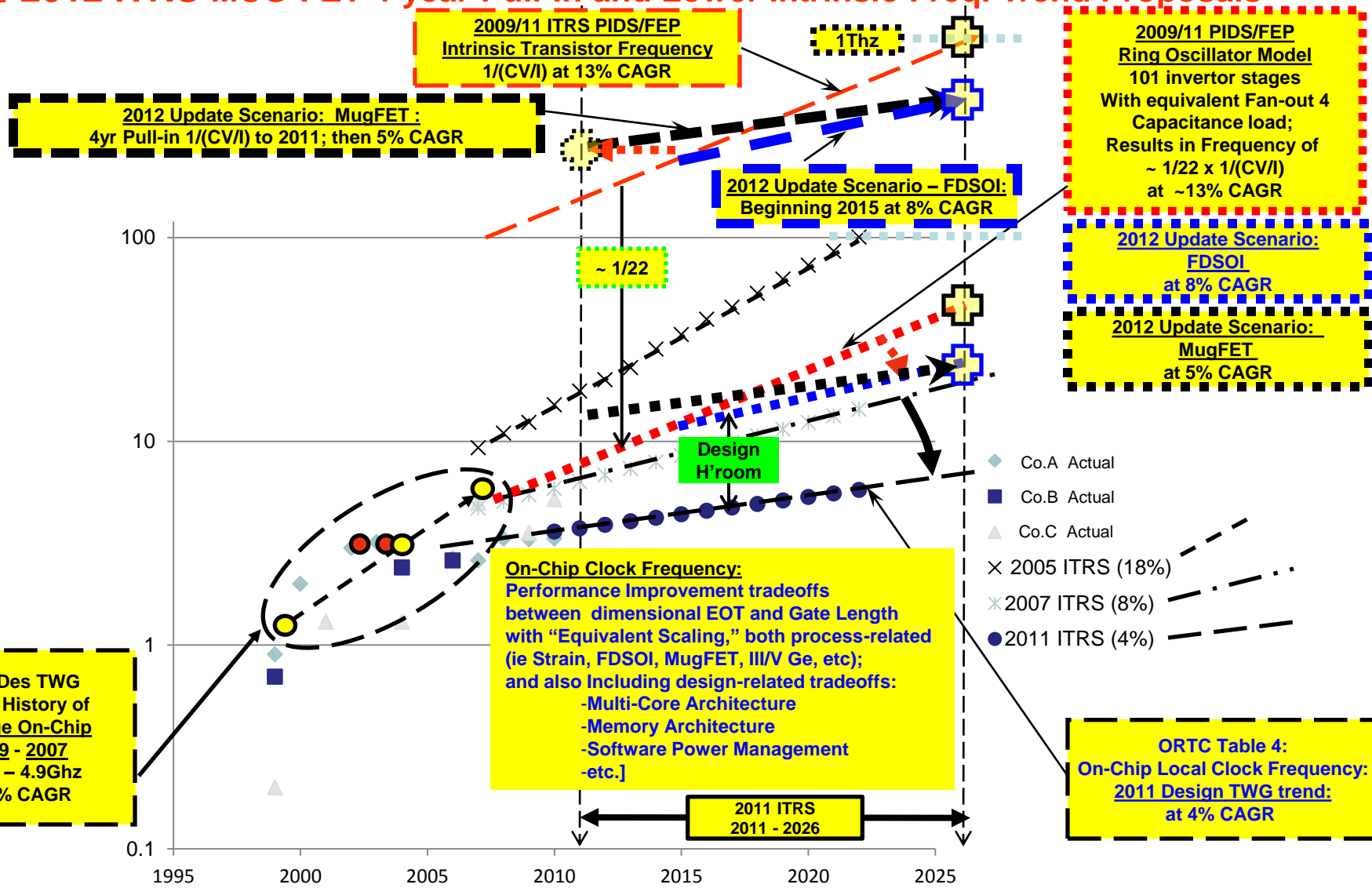


Figure 8a 2012 Update Model Trend versus 2009/2011 ITRS PIDS TWG Transistor Intrinsic Frequency ($1/(CV/I)$) Performance Trends

Source: 2011 ITRS - Executive Summary Fig. 8a



Fig. 8b - ORTC Table 4: On Chip Local Clock Frequency Trend Comparisons to PIDS vs. 2012 ITRS MUG-FET 4-year Pull-In and Lower Intrinsic Freq. Trend Proposals



Source: ITRS Test TWG compilation, ca 4Q 2010; 2011 ITRS PIDS, Design TWGs



Figure 8b Design On-Chip Frequency vs. PIDS Intrinsic Transistor and Ring Oscillator Model Frequency

Source: 2011 ITRS - Executive Summary Fig 8b