

# Test and Test Equipment

December 2009

HsinChu, Taiwan

Roger Barth - Numonyx

ITRS Test TWG



# 2009 Test Chapter Contributors

Debbora Ahlgren  
Rob Aitken  
Ken-ichi Anzou  
Takumi Aoki  
Dave Armstrong  
Roberta Bailey Roberts  
Roger Barth  
John Bearden  
Shawn Blanton  
Ken Butler  
Yi Cai  
Wendy Chen  
Calvin Cheung  
Steve Comen  
Peter Crabbe  
Robert Daasch  
Stefan Eichenberger  
Bill Eklow  
Francois-Fabien Ferhani  
Shawn Fetterolf  
Anne Gattiker  
Rama Gudavalli  
Kazumi Hatayama  
Jeong Ho Cho

Hisao Horibe  
Hiroki Ikeda  
Koji Isodono  
Shuichi Ito  
Takuya Kobayashi  
Gibum Koo  
Akitoshi Kumada  
Greg Labonte  
Rien Looijen  
Michio Maekawa  
Amit Majumdar  
Prasad Mantri  
Peter Maxwell  
Jerry Mcbride  
Anne Meixner  
Peter Muhmentahler  
Takeshi Nagasaka  
Takairo Nagata  
Masaaki Namba  
Phil Nigh  
Akitoshi Nishimura  
Sejang Oh  
Peter O'Neill

Mike Peng Li  
Frank Poehl  
Chris Portelli-Hale  
Bill Price  
Joe Reynick  
Brad Robbins  
Paul Roddy  
Mike Rodgers  
Yasuo Sato  
Taylor Scanlon  
Rene Segers  
Steven Slupsky  
Kozaburo Suzuki  
Ken Taoka  
Wataru Uchida  
Kees Visser  
Erik Volkerink  
Burnie West  
Tom Williams  
Yervant Zorian

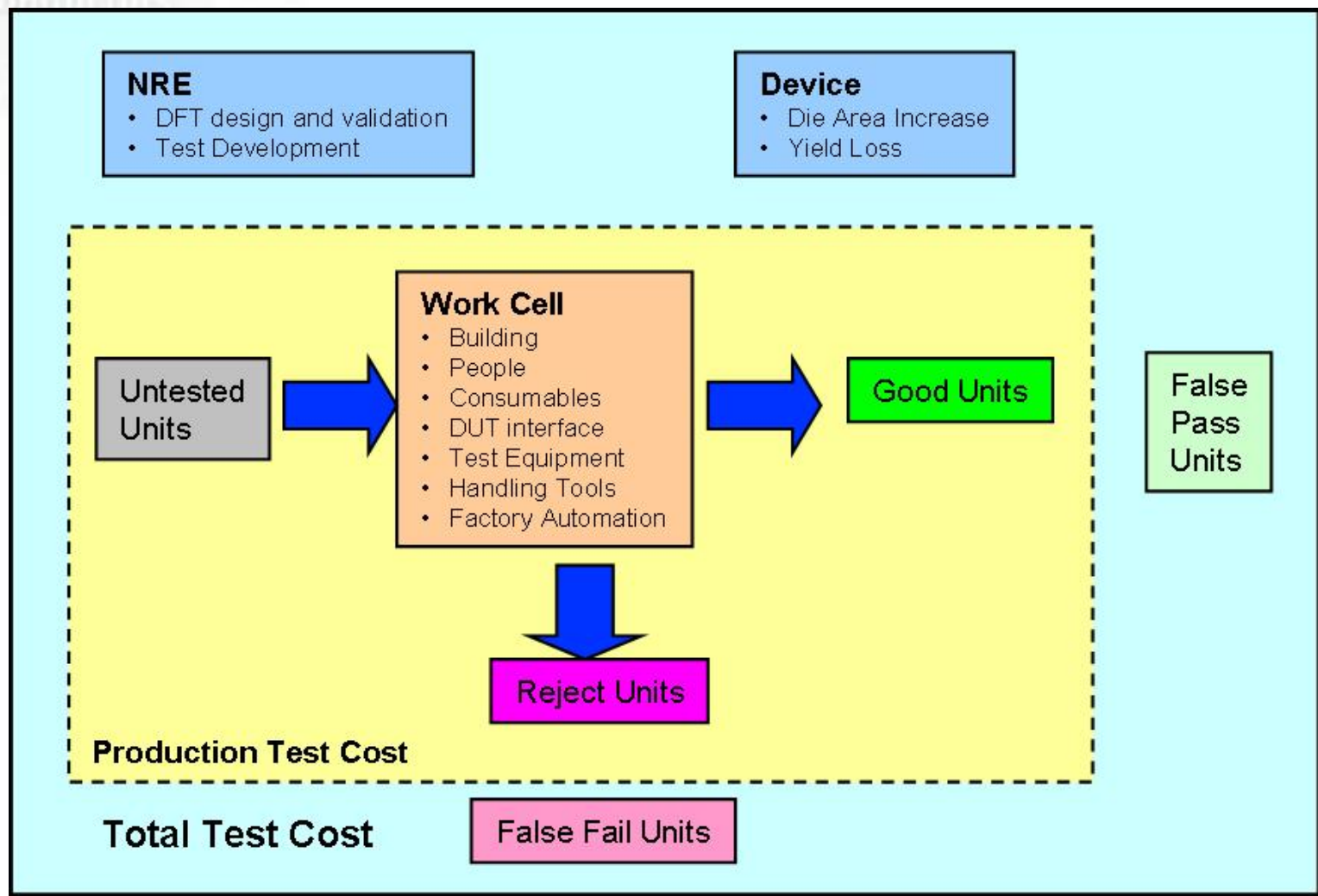


# 2009 Drivers

- Device trends
  - Increasing device interface **bandwidth** (# of signals and data rates)
  - Increasing **device integration** (SoC, SiP, MCP, 3D packaging)
  - Integration of emerging and **non-digital CMOS** technologies
  - **Complex package** electrical and mechanical characteristics
  - Device **characteristics beyond** one sided **stimulus/response** model
  - **3 Dimensional Devices – Multi-die and Multi-layer**
  - Multiple I/O types and power supplies on same device
- Test process complexity
  - Device **customization** during the test process
  - “**Distributed test**” to maintain cost scaling
  - **Feedback** data for tuning manufacturing
  - Dynamic test flows via “**Adaptive Test**”
- Economic scaling of test
  - **Physical limits** of test parallelism
  - Managing (logic) test data and feedback **data volume**
  - Effective limit for speed difference of **HVM ATE versus DUT**
  - Managing **interface hardware** and (test) socket costs
  - Trade-off between the **cost of test** and the **cost of quality**
  - **Multiple Test insertions** due to **System test and BIST**



# Test Cost Components




# Test Cost Survey

- Survey completed in 2009 to determine key factors & metrics

**Test Cost Metrics**

- Cost per unit
- Percent of total Product Cost
- Cost per second
- Cost per megabit (memory)

  
**Metrics Not used**

- Cost per transistor
- Capital expenditures

**Major Test Cost Drivers**

- ATE capital
- Interface hardware
- Test program development
- Test Time and Coverage

**Current Methods of controlling cost**

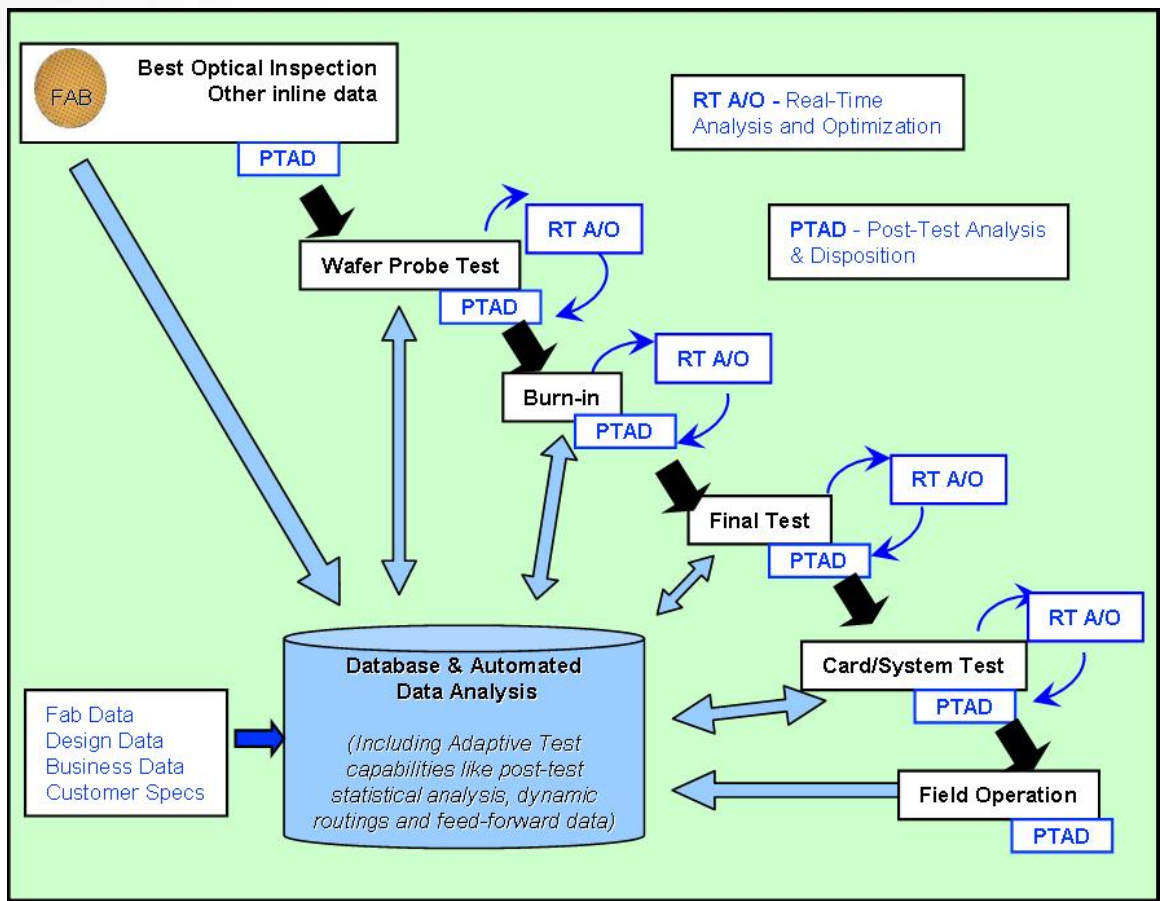
- Test Parallelism
- Reduced Pin interfaces
- Structural Test & Scan
- DFT and BIST
- Concurrent test

**Future Methods of controlling cost**

- Wafer-level at-speed testing
- Advanced embedded instruments
- Adaptive Test
- New contacting technologies
- Build-in Fault Tolerance



# Adaptive Test



- Modify testing based on analysis of previous results
  - Real-time
  - Near-time
  - Off-line
- Benefits
  - Higher Quality
  - Fast Test Time Reduction
  - Lower cost
  - Fast yield learning
- Requires data infrastructure
  - Database
  - Analysis tools ← Confidence
- Implementation is evolving
  - Multiple learning steps
  - Delaying won't ease task



# Prober Characteristics

| Year of Production                    | 2009        | 2010        | 2011        | 2012        | 2013        | 2014        |
|---------------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|
| <b>Device</b>                         |             |             |             |             |             |             |
| Wafer diameter (mm)                   | 300         | 300         | 300         | 300         | 300         | 450         |
| Wafer thickness (um)                  | 80-775      | 80-775      | 80-775      | 80-775      | 80-775      | 50-1000     |
| Maximum I/O pads                      | 4000        | 5300        | 5300        | 5300        | 5300        | 5300        |
| Carrier                               |             |             |             |             |             | TBD         |
| <b>Tester</b>                         |             |             |             |             |             |             |
| Test head weight (Kg)                 | 1000        | 1000        | 1000        | 1000        | 1000        | 1500        |
| Mechanical I/F for Tester (Type)      | Pogo/Chuck  | Pogo/Chuck  | Pogo/Other  | Pogo/Other  | Pogo/Other  | Pogo/Other  |
| <b>Probe Card</b>                     |             |             |             |             |             |             |
| Probe card diameter (mm)              | 2009        |             | 580         | 580         | 580         | 725         |
| Probe card Thickness (mm) PCB         |             |             | 10          | 10          | 10          | 18          |
| <b>Prober</b>                         |             |             |             |             |             |             |
| Chuck X & Y positioning accuracy (um) | 2           | 1           | 1           | 1           | 1           | 1           |
| Probe-to-pad alignment (um) XY +/-    | 2           | 2           | 2           | 2           | 2           | 2           |
| Chuck Z positioning accuracy (um)     | 1           | 0.5         | 0.5         | 0.5         | 0.5         | 0.5         |
| Probe-to-pad alignment (um) Z +/-     | 5           | 5           | 5           | 5           | 5           | 5           |
| Chuck Coplanarity (um) +/-            | 15          | 5           | 5           | 5           | 5           | 5           |
| Maximum Chuck force Logic (Kg)        | 75          | 75          | 75          | 90          | 90          | 90          |
| Maximum Chuck force Memory (Kg)       | 200         | 300         | 300         | 300         | 300         | 500         |
| Set point range (°C)                  | -55 to +150 | -55 to +150 | -55 to +150 | -55 to +150 | -55 to +150 | -55 to +150 |
| Temp. Accuracy (Degree C) +/-         | 1           | 0.5         | 0.5         | 0.5         | 0.5         | 0.5         |
| Total power Logic (Per die)           | 1000        | 1000        | 1000        | 1000        | 1000        | 1000        |
| Power density (Watt/cm <sup>2</sup> ) | 250         | 250         | 250         | 250         | 250         | 250         |
| Chuck Leakage (Parametric, pA)        | 1           | 0.1         | 0.1         | 0.1         | 0.1         | 0.1         |
| Foot Print (m2)                       | 2.1         | 2.1         | 2.1         | 2.1         | 2.1         | 4           |

- Many changes / additions from 2008 tables
  - Probe card dimensions
  - Test head weight
  - Temperature accuracy
  - 450mm wafer support
  - Chuck leakage
  - Planarity
  - Etc.

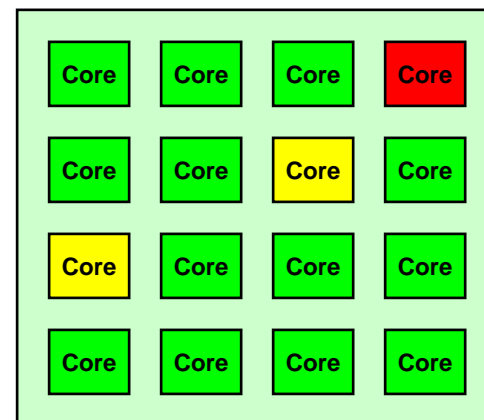
| Year of Production                    | 2007       | 2008       | 2009       | 2010        | 2011        | 2012        |
|---------------------------------------|------------|------------|------------|-------------|-------------|-------------|
| Wafer diameter (mm)                   | 300        | 300        | 300        | 300         | 300         | 300         |
| Wafer thickness (um)                  | 80-775     | 80-775     | 80-775     | 80-775      | 80-775      | 80-775      |
| Maximum I/O pads                      |            |            | 4000       | 5300        | 5300        | 5300        |
| Chuck X & Y positioning accuracy (um) |            |            | 2008       | 1           | 1           | 1           |
| Chuck Z positioning accuracy (um)     |            |            |            | 0.5         | 0.5         | 0.5         |
| Probe-to-pad alignment (um)           |            |            |            | 4.5         | 3.5         | 3.5         |
| Maximum chuck force (kg)              | 100        | 100        | 100        | 100         | 100         | 100         |
| Set point range (°C)                  | -30 to +85 | -30 to +85 | -30 to +85 | -45 to +125 | -45 to +125 | -45 to +125 |
| Total power (Watts)                   | 130        | 130        | 250        | 250         | 250         | 250         |
| Power density (Watt/cm <sup>2</sup> ) | 60         | 60         | 120        | 120         | 120         | 120         |

- Solutions exist until 2014



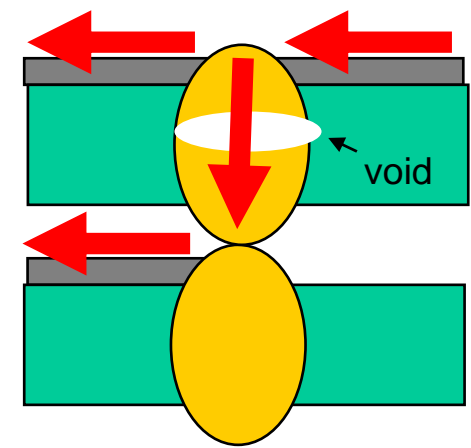
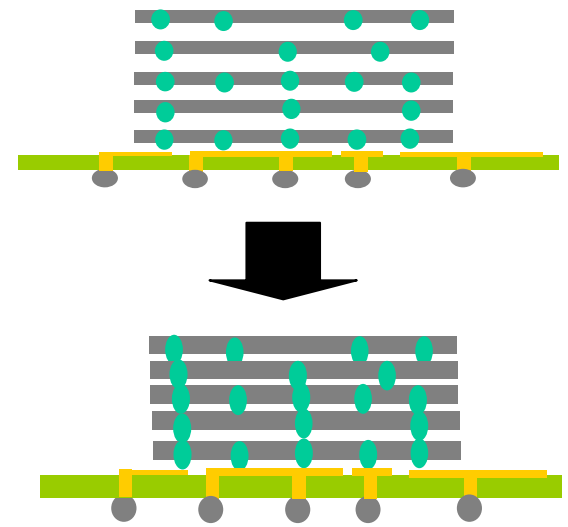
# Fault Tolerant Devices “Bad but Good”

- Many future devices will be Fault Tolerant
  - “Adapt or Repair”
- Homogeneous multi-core device...not all cores need be good
  - Identify with “Smart kernel” or continuous test...
  - ...Ignore the bad core
  - ...Fix (run slower or tailor operations)
- Memory
  - Allow or correct bad bits / blocks
  - Background memory checker
  - Wear leveling
- Image sensors without the “perfect” image
  - What is perfect?



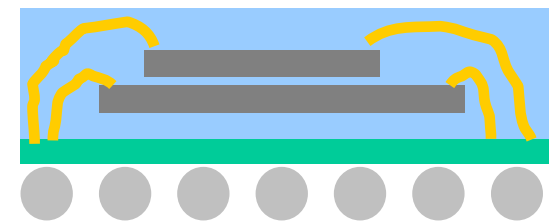
# 3D Devices

- Multiple die system
  - Sub-systems designed to operate and be assembled together
  - Process optimized for contents of each die
    - Logic, DRAM, NVM, Analog
  - Connection by potentially 1000's of TSVs (Thru Silicon Via's)
- Design, Interconnect, Assembly and Test problem
- DFT Requirements
  - Testability of each die
  - Via continuity checks
    - For signal and non-signal vias
    - 3-5 um via cannot be probed! ESD!
  - N+ die test methodology as die added
  - Final "System" test

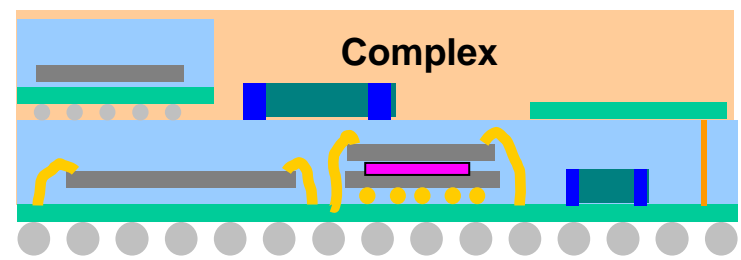
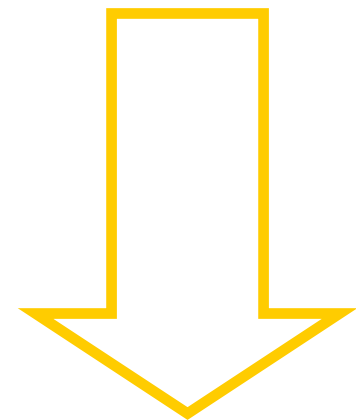


# System in Package (SiP)

- Target is low power devices
- Challenges
  - High yield with low test cost
  - Standardized test strategy for mini-systems
- Potential test solutions
  - Design for die, debug and system test
  - Per die BIST
  - KGD with minimal post test
    - “KGD” defined as Functional and Structural good?



Simple

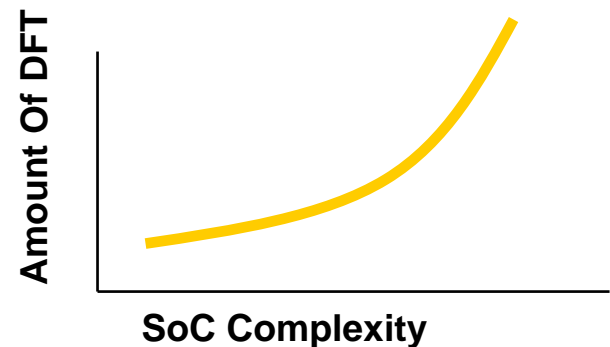
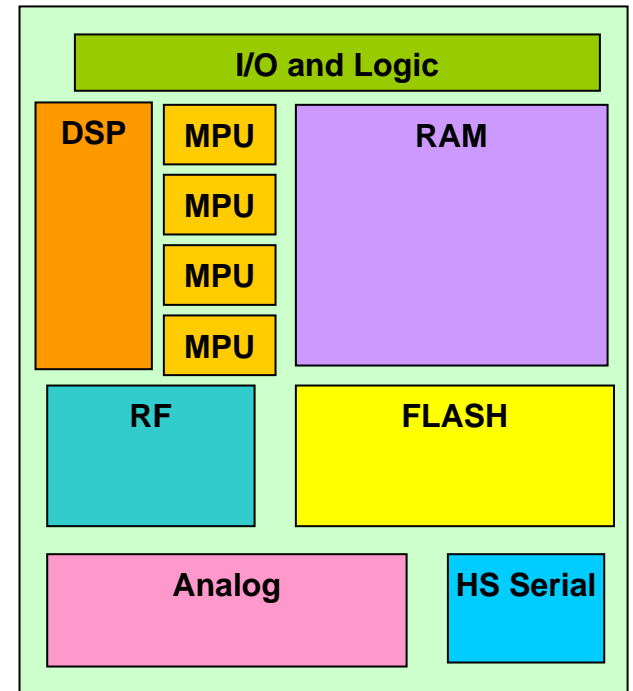


Complex

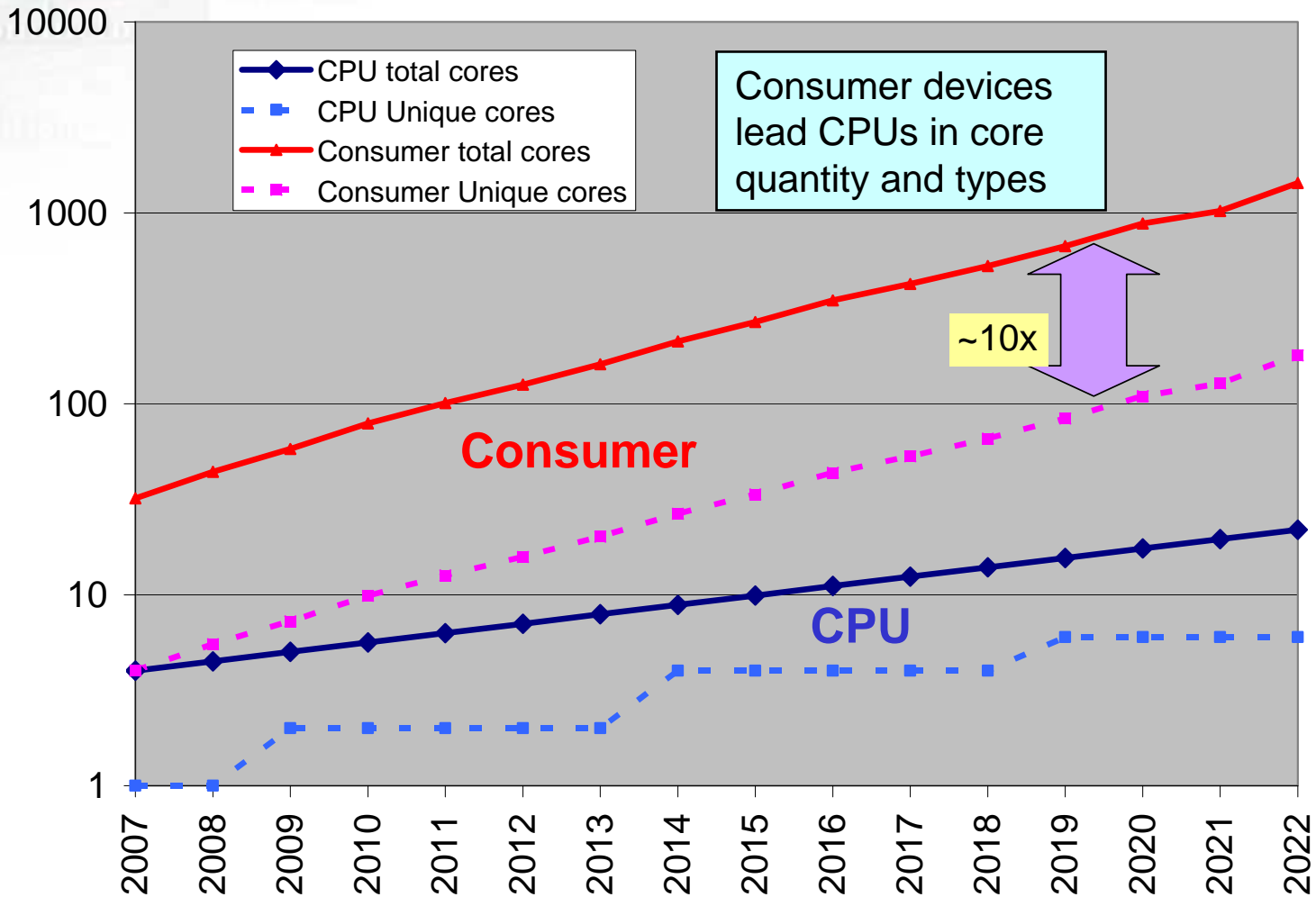


# SoC – Consumer Logic

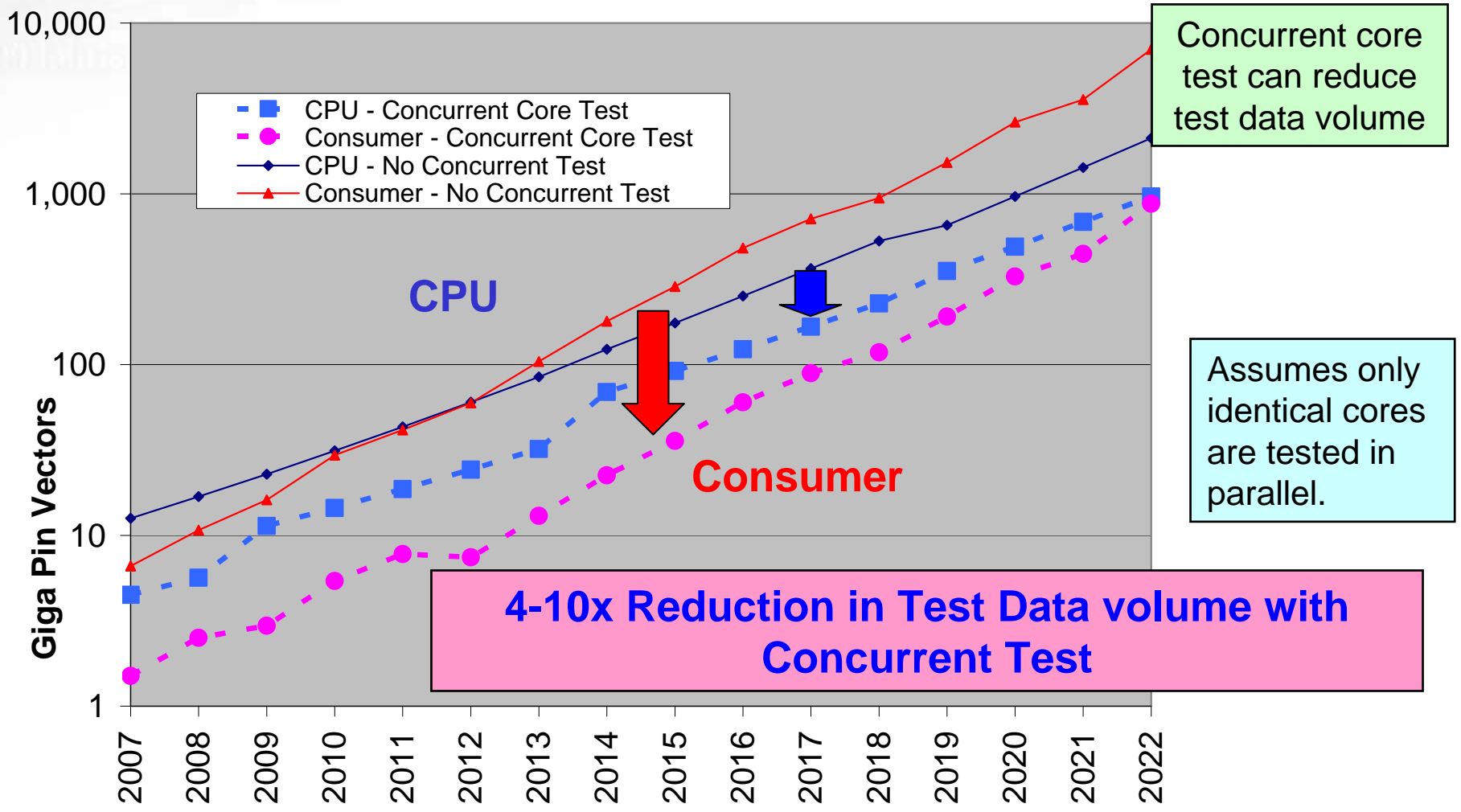
- > **1000** cores by 2020
  - MPU / logic
  - Memory
  - Analog / RF
  - HS serial
- SoC test challenges
  - Management of per core DFT
  - Standardization of core “wrappers”
    - IEEE 1500 core test
    - IEEE P1687 JTAG chip-test
  - High Data Compression (>100)



# Proliferation of Cores



# Test Data Volume



# Test Time Reduction Potential Solutions

| First Year of IC Production                             | 2009     | 2010     | 2011     | 2012     | 2013     | 2014     | 2015     | 2016     | 2017     | 2018     | 2019     | 2020     | 2021     | 2022     | 2023     | 2024     |
|---|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Required Test time reduction</b>                     | 1x       | 2x       | 2x       | 2x       | 2.5x     | 2.5x     | 2.5x     | 3.2x     | 3.2x     | 3.2x     | 4.2x     | 4.2x     | 4.2x     | 5.6x     | 5.6      | 5.6      |
| <b>Multi-site Test</b>                                  | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal |          |          |          |          |          |          |          |          |          |
| <b>Core-Parallel Test</b>                               | Blue     | Blue     | Blue     | Blue     | Blue     |          |          | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal |          |          |          |
| <b>Test Vector Reduction<br/>(includes compression)</b> | Blue     | Blue     | Blue     | Blue     | Blue     |          |          | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal |          |          |          |
| <b>Test per clock</b>                                   | Black    | Black    | Black    | Black    | Black    | Black    | Black    | Blue     | Blue     | Blue     | Blue     |          |          | Diagonal | Diagonal | Diagonal |

*Research Required*   
*Development Underway*   
*Qualification / Pre-Production*   
*Continuous Improvement* 

- Required test time reduction is driven by SoC
- Assumes increasing design complexity and transistor count will not increase test time



# DFT Compression Potential Solutions

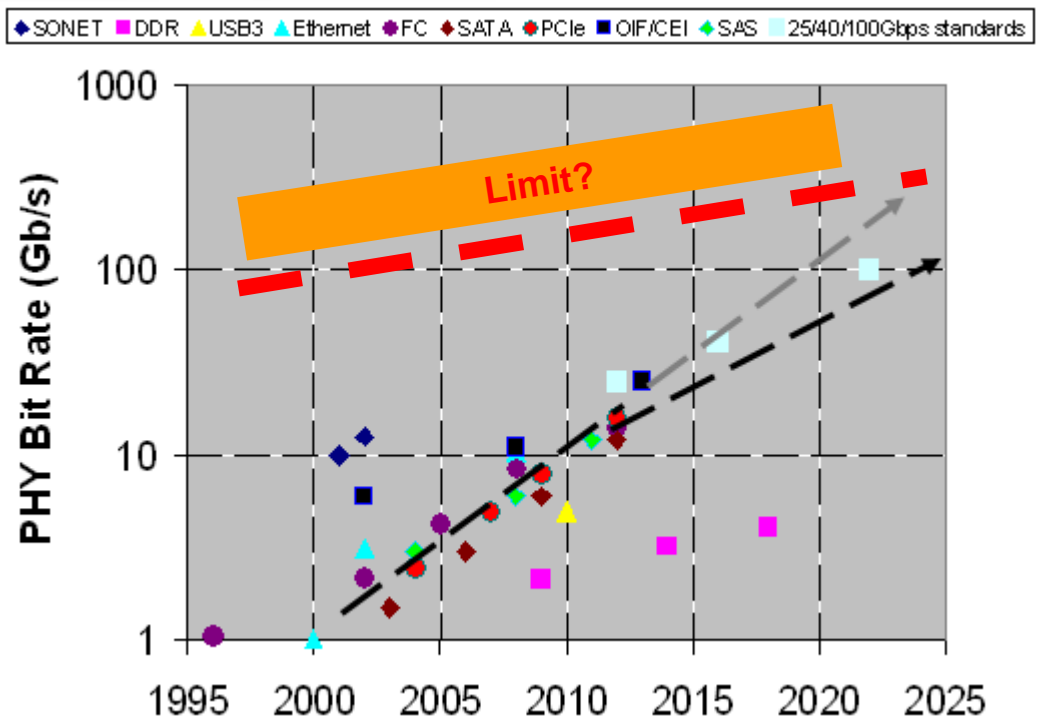
| First Year of IC Production                | 2009     | 2010     | 2011     | 2012     | 2013     | 2014     | 2015     | 2016     | 2017     | 2018     | 2019     | 2020     | 2021     | 2022     | 2023  | 2024   |
|--|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-------|--------|
| Required compression                       | 80       | 200      | 300      | 500      | 750      | 1300     | 2000     | 3300     | 4800     | 7300     | 12000    | 2000     | 35000    | 67000    | 83000 | 104000 |
| 1-Dimensional Test-cube compression (100X) | Diagonal | Diagonal | Diagonal | Diagonal | Diagonal |          |          |          |          |          |          |          |          |          |       |        |
| 2-Dimensional Spatial compression(500X)    | Blue     | Blue     | Blue     |          | Diagonal | Diagonal | Diagonal |          |          |          |          |          |          |          |       |        |
| 3-Dimensional Time compression(1000X)      | Black    | Black    | Blue     | Blue     | Blue     |          | Diagonal | Diagonal | Diagonal | Diagonal |          |          |          |          |       |        |
| Multi-dimensional compression(5000X)       |          |          | Black    | Black    | Black    | Black    | Blue     | Blue     | Blue     |          | Diagonal | Diagonal | Diagonal | Diagonal |       |        |

*Research Required*  
*Development Underway*  
*Qualification / Pre-Production*  
*Continuous Improvement*



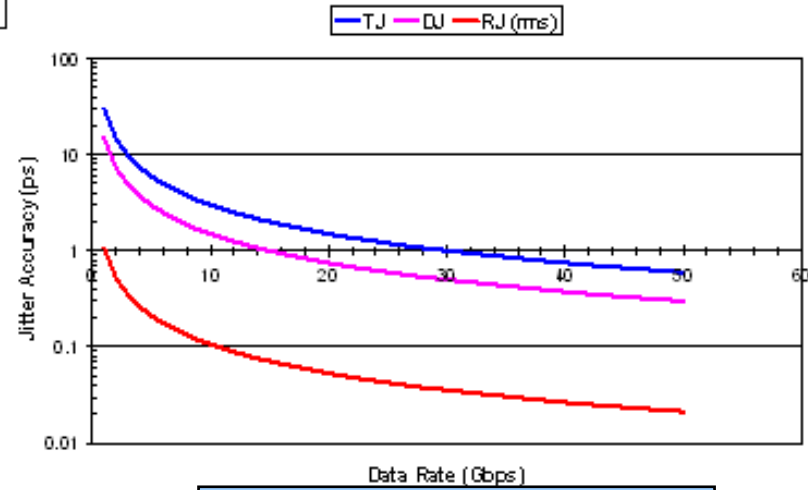
- Development is necessary to get very high levels of data compression
- Demonstrated techniques are just approaching 1000x
- 100k data compression necessary out in time...no clear path yet!

# High Speed Interfaces



- Bit bandwidth increasing...
- Physical limit?
- Test limit?

High-Speed I/O Jitter Test Accuracy



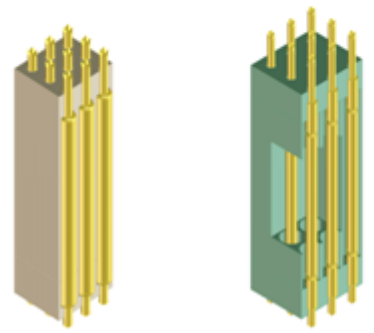
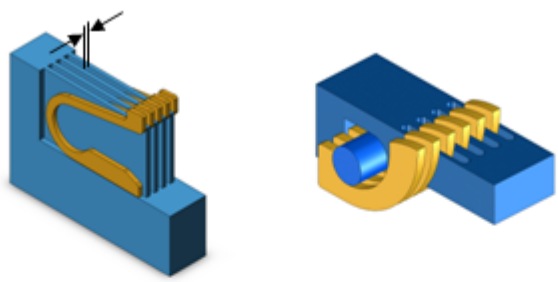
Jitter Test Critical for HS Interfaces

Test Sockets are not able to support controlled impedance contacts at >15 GT/s

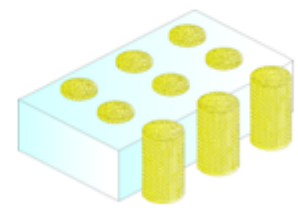


# Contactors

## Blade Contacts



Spring Probe  
Contacts

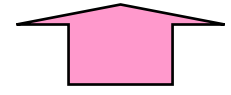


Conductive  
Rubber  
Contact

## BGA Spring Probe Contacts

|        | Pitch |      |      |      |      |
|--------|-------|------|------|------|------|
|        | 0.80  | 0.65 | 0.50 | 0.40 | 0.30 |
| 1.5 nH | 1.0   | 1.0  | 0.8  | 0.8  | 0.9  |
| 1.0 nH | 1.5   | 1.5  | 1.3  | 1.3  | 1.4  |
| 0.8 nH | 2.1   | 2.1  | 1.8  | 1.8  | 1.9  |
| 0.5 nH | 3.3   | 3.2  | 2.8  | 2.8  | 3.0  |
| 0.3 nH | 7.3   | 6.9  | 6.2  | 6.1  | 6.3  |
| 0.1 nH | 21.0  | 20.0 | 20.0 | 19.3 | 19.0 |

Self-Inductance  
(nH)



Bandwidth (GHz)

- Test frequency is limited by test sockets
- New contacting methods are required to support > 10GHz
  - i.e. conductive rubber

# Specialty Devices

- LCD drivers
  - Form factor of 30mm x 1.5mm
  - Long bond pads on 20um centers
- Image sensors
  - Micro lens check with pupil test
  - Backlighting remains an issue
  - Future touch panel enhancement
  - Small die handling
- 3 axis MEMS Accelerometer
  - Consumer drop/rotate applications
  - High gravity operation validation

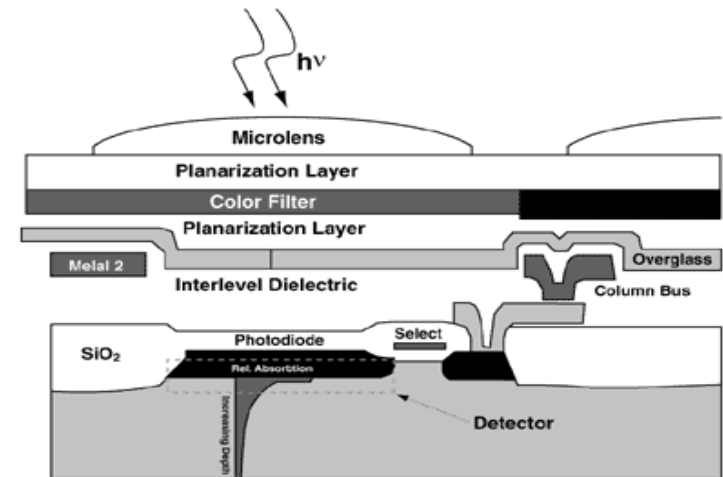
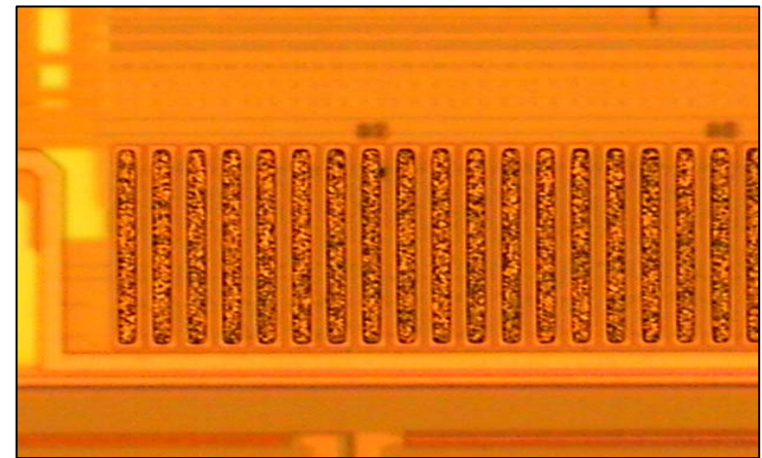


Image sensor structure cross section 18

# 2009 Changes

- DFT
  - Test compression and test time potential solutions identified
  - Major rewrite completed of the Design Chapter DFT section
- Test Cost
  - Test cost survey completed that quantifies industry view
  - Test parallelism dependency by device type modified based on I/O count
- Adaptive Test
  - New chapter section shows necessity for adaptive test to lower cost
- Prober
  - Complete redo of prober table to address parallelism and power
- Probecard
  - LCD display driver probe added as driver
- Handler
  - Added 10-50 Watt handler category
- Test Sockets
  - Socket BW limitations on current sockets
  - New future contacting solutions are required



# 2010 Directions

- DFT partitioning between Design and Test
- Further definition of 3D Silicon Test Requirements
- Review of Key Test Drivers
- Discovery into potential methods for test data volume reduction
- Probing and Contacting for High Speed Devices
- Probing of very thin wafers?

