

PIDS Summary

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Hsinchu, Taiwan

PIDS TWG Members
Speaker: Kwok Ng (U.S. Chair)



PIDS TWG Roster

---U.S---

Ng, Kwok^C
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Brewer, Joe
Chang, Chorng-Ping
Cheung, Charles
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Hutchby, Jim
Lam, Chung
Maszara, Witek
Ning, Tak
Prall, Kirk
Tsai, Wilman
Wong, Philip
Wu, Jeff
Xiang, Qi
Yeap, Geoffrey
Yu, Scott
Zeitzoff, Peter

---Japan---

Oda, Hidekazu^{CC}
Inoue, Hirofumi^{CC}
Akasaka, Yasushi
Eimori, Takahisa
Hiramoto, Toshiro
Hori, Atsushi
Ida, Jiro
Imai, Kiyotaka
Kasai, Naoki
Mifuji, Michihiko
Ogura, Mototsugu
Sawada, Shizuo
Shibahara, Kentaro
Sugii, Toshihiro
Tadaki, Yoshitaka
Tagawa, Yukio
Takagi, Shinnichi
Tanaka, Tetsu
Yoshimi, Makoto

---Europe---

Skotnicki, Thomas^C
Boeuf, Frederic
DeMeyer, Kristin
Jurczak, Malgorzata
Lander, Robert
Poiroux, Thierry
Schulz, Thomas

---Taiwan---

Liu, Rich^{CC}
Ma, Mike^{CC}
Diaz, Carlos
See, Yee-Chaung

---Korea---

Cha, Seon Yong
Jin, Gyoyoung

C=Chair, CC=Co-Chair



Outline

- PIDS Mission and Sub-Groups
- 2009 Edition Update Summary
 - Logic
 - Memory: DRAM
 - Memory: Nonvolatile
 - Reliability
- On-going Activities



- **PIDS** = **P**rocess **I**ntegration, **D**evelopments, and **S**tructures
- Mission:
 - Provide physical and electrical requirements and solutions for sustaining IC scaling
 - Scopes:
 - Performance (speed, density, power, functionality...)
 - Structures
 - Process-integration issues
 - Reliability

PIDS Sub-Groups

- Logic
 - HP = High Performance (μ P...)
 - LOP = Low Operating Power (notebook...)
 - LSTP = Low Standby Power (cellular...)
- Memory
 - DRAM
 - Nonvolatile
- Reliability

2009 Update: Logic

- L_{gate} scaling is slowed down (from survey and reverse engineering):
 - 2008 Edition: HP L_g is slowed down by 3-5 years, with change of slope.
LOP L_g slowed-down by 1-3 years, with change of slope.
 - 2009 Edition: L_g scaling slowed down by 1 year on most devices.
- CV/I metric relaxed from 17% increase per year to 13%.
- Ring-oscillator delay is added, besides CV/I , as a more realistic speed metric.
Both fan-out=1 and fan-out=4 are included.

2009 Update: Logic (cont'ed)

- To simulate CMOS inverter in ring oscillator, I_{sat} of p -channel MOSFET is added.
All other parameters are assumed symmetric to those of n -MOSFETs.
- Subthreshold source-drain leakage currents are held constant independent of L_{gate}/year .
Values for HP, LOP, LSTP are 100 nA/ μm , 5 nA/ μm , 50 pA/ μm respectively.
- The criterion for source/drain parasitic resistance is set for degradation of 33% (1/3) of I_{sat} compared to without any series resistance.

2009 Update: DRAM

- Small cell factor– $4F^2$ introduced in 2011.

<i>Year in Production</i>	2009	2010	2011	2012
<i>DRAM^{1/2}Pitch (nm) [1]</i>	50	44	40	36
<i>DRAMcell size (μm^2) [2]</i>	0.01500	0.01162	0.00640	0.00518
<i>DRAMcell FET structure [6]</i>	RCAT	FinFET	FinFET	FinFET
<i>Cell Size Factor: a [11]</i>	6	6	4	4
<i>Array Area Efficiency [12]</i>	0.56	0.56	0.50	0.50

- FinFET/3D FET is still unknown for 2010 production.
- DRAM product size 1 yr delay from ITRS 2007/2008 (4 Gb in 2011).

2009 Update: Nonvolatile Memory

- NAND flash:
 - Half-pitch pulled-in 1 year from 2007/2008 Editions.
 - Floating-gate to charge-trapping flash transition in 2012, delay 2 years.
 - 3 bit/cell – 4bit/cell transition delays 2 years, to 2012.
 - 3-D charge-trapping flash in 2014, delay 1 year.
- Update non-charge-based NVM requirements:
 - STT (spin torque transfer) MRAM added.
 - PCRAM (phase change RAM) updated to reflect recent product reality.
 - FeRAM scaling pace slows down to reflect product reality.

2009 Update: Reliability

- Major revisions in the reliability requirement specifications.
- Increase emphasis on circuit impact of device reliability issues.
- Bring up the need for paradigm change and the challenges involved.
 - The need for reliability-aware fault-tolerant design.



On-Going Activities

- Adding power metric on device level.
- Explore alternate device simulator to MASTAR.
- Merging LOP and LSTP as 1 low-power technology.
- Expand on potential solutions of III-V or/and Ge as alternate channel materials for Logic HP.
- Surveys on DRAM and NVM being conducted by Japan-PIDS. Results to be presented in Spring meeting 2010.

(End)

