



# 2009 Litho ITRS Update

Lithography iTWG  
2009 Summary



International Technology Roadmap for Semiconductors

# Outline

- Group Functions
  - Various Techniques for Achieving Specifications
  - Lithography Difficult Challenges
    - Difficult Challenges > 22 nm
    - Difficult Challenges < 22 nm (not 193)
  - Lithography Technology Requirements
  - Lithography Potential Solutions
- Table Groups – International
  - Mask / Resist / EUVL / Imprint / Direct Write



Table LITH1 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography for MPU and DRAM

MPU M1 contacted ½ pitch	65 nm	45 nm	32 nm	Optical 22 nm	EUV 22 nm
$k_1$ Range [A]	0.31–0.40	0.28–0.31	0.18-0.28	0.14-0.22	0.58
<b>Design rules</b>	Litho friendly design rules		Double exposure compatible design		Simple High k1 Design
Restrictions (cumulative)	Features on grid	Restricted feature set	Double exposure compatible design	Restricted feature set for Multi Exposure	None
<b>Masks</b> (Optical proximity correction)	Model-based OPC with vector simulation, SRAF, polarization corrections	All previous approaches + variation of OPC intensity by location in circuit.	All previous approaches + Dense OPC. Source Mask Optimization	All previous approaches & + Inverse Lithography	Simple Model based OPC. Similar Patterning Complexities 120nm node
(Gate and M1 layer mask type)	APSM, hiT EPSM, dual dipole	Binary, APSM, CLpsm, hiT EPSM, double exposure with 2x larger pitch			EUV (Binary)
(Contacts/ vias layers mask type)	Binary, EPSM, HiT PSM	EPSM, HiT PSM	HiT EPSM, double exposure with 2x larger pitch		EUV (Binary)
<b>Resist</b>					
Thickness	<225 nm	<160 nm	<120 nm	<66nm	<66nm
Substrate	ARC, hard masks, top coats		ARC, hard masks, top coats, contrast enhancing layers		Hard masks
Etch	Post development resist width reduction				
<b>Tool</b>	Aberration monitoring		Aberration monitoring and adjustment	3-4 X more Brightness	
(Illumination)	Custom illumination, polarization optimization			SMO - Programmable Illumination	
(Dose control)	Dose adjustment across the wafer and along scan		Dose adjustment across wafer, across slit, and along scan		
(Process control (CD and overlay))	Automated process control with downloaded offsets, metrology integrated in lithography cell		Plus - High Order Overlay correctable, Double Patterning Related Interlayer Control		Automated process control with downloaded offsets, metrology integrated in lithography cell

NO PROVEN OPTICAL SOLUTION BELOW THIS LINE

<i>Difficult Challenges &gt; 22 nm</i>	<i>Summary of Issues</i>
Optical masks with features for resolution enhancement and post-optical mask fabrication	<p>Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features</p> <p>Registration, CD, and defect control for masks</p> <p>Eliminating formation of progressive defects and haze during exposure</p> <p>Understanding and achieving the specific signature and specifications for a Double Patterned mask</p> <p>Establishing a stable process so that signatures can be corrected.</p>
Double patterning	<p>Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures</p> <p>Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs</p> <p>Availability of high productivity scanner, track, and process to maintain low cost-of-ownership</p> <p>Photoresists with independent exposure of multiple passes</p> <p>Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.</p>
Cost control and return on investment	<p>Achieving constant/improved ratio of exposure related tool cost to throughput over time</p> <p>ROI for small volume products</p> <p>Resources for developing multiple technologies at the same time</p> <p>Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume</p> <p>450 mm diameter wafer infrastructure</p>
Process control	<p>New and improved alignment and overlay control methods independent of technology option to <math>&lt;5.7</math> nm <math>3\sigma</math> overlay error</p> <p>Controlling LER, CD changes induced by metrology, and defects <math>&lt; 10</math> nm in size</p> <p>Greater accuracy of resist simulation models</p> <p>Accuracy of OPC and OPC verification, especially in presence of polarization effects</p> <p>Lithography friendly design and design for manufacturing (DFM)</p>

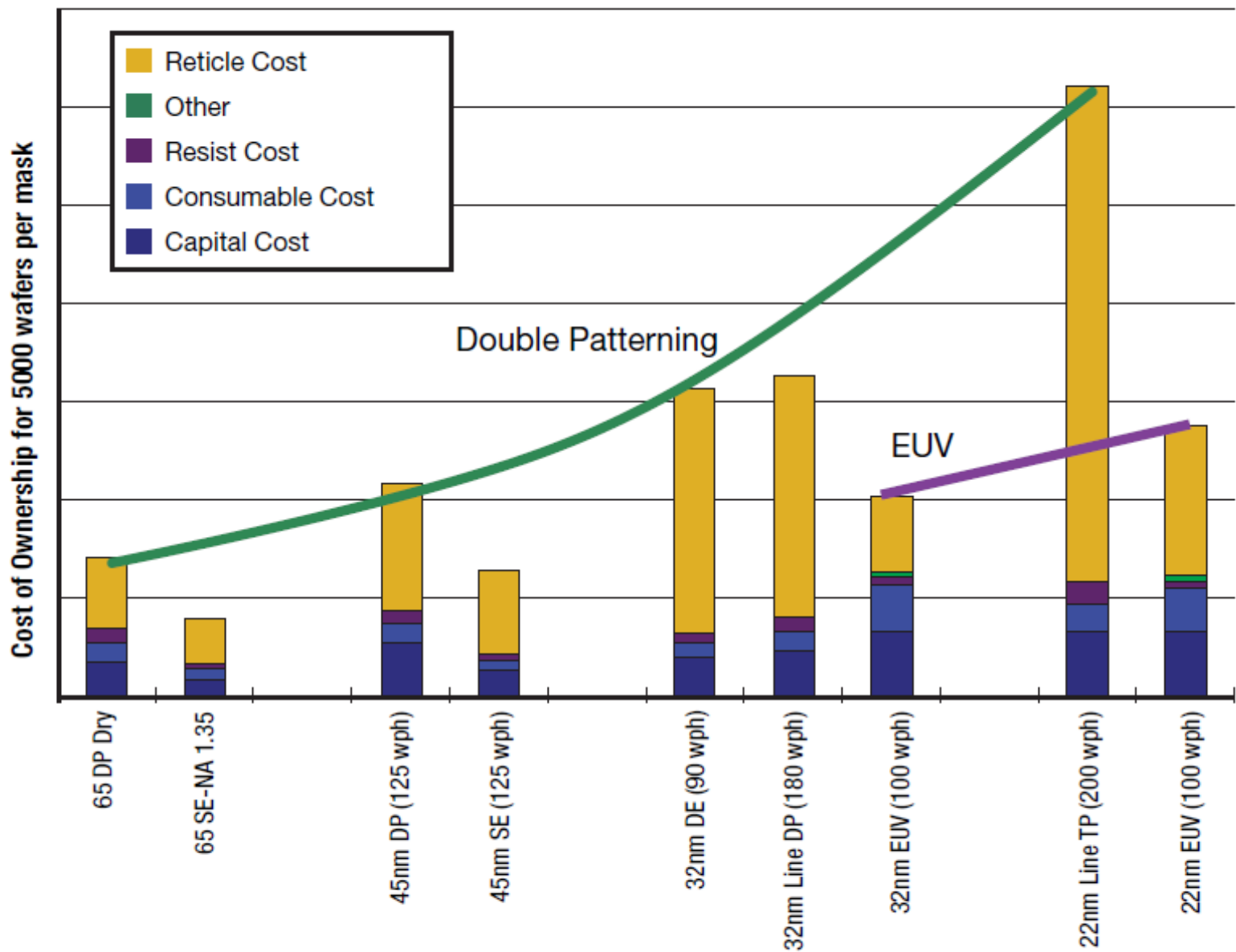


Figure 2. The Relative Cost of Ownership for the Critical Level of a 5000-Wafer Run Device vs. Lithography Process and Node

Table Litho2b Lithography Difficult Challenges

Difficult Challenges = □ 22 nm	
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
	Cost control and return on investment
	Resist with < 1.5 nm 3s LWR, < 10 mJ/cm <sup>2</sup> sensitivity and < 20 nm ½ pitch resolution
	Fabrication of Zero Printing Defect Mask Blanks
	Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection)
	Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs)
	Controlling optics contamination to achieve > five-year lifetime
	Protection of EUV masks from defects without pellicles
	Fabrication of optics with < 0.10 nm rms figure error and < 7% intrinsic flare
Resist materials	Limits of chemically amplified resist sensitivity for < 22 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control add (limits)
	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Low defects in resist materials (size < 10nm)
	Line width roughness < 1.4nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair)
	Mask process control methods and yield enhancement
	Cost control and return on investment
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective post-optical masks
	Cost effective 450mm lithography systems
	Achieving ROI for small volume products

# Future Fab Paper

EUV Lithography	Maskless Lithography	Imprint Lithography
<b>Source Power</b> > 180 W at Intermediate Focus With HVM Reliability Lifetime of Collector Optics and Source Components	<b>E-Beam Patterning System</b> Throughput CD - Stitching Errors Cross Talk Between Beams Wafer Heating During Write Pattern Overlay System Calibrations	<b>Mask</b> 1X Mask Pattern Inspection and Repair 1X Specifications 1X Mask Writing Time (Cost) 1X Defect-Free Process Mask Life
<b>Resist</b> LWR - < 1.5nm 3s Dose - < 10 mJ/cm <sup>2</sup> Resolution < 20nm 1/2 Pitch	<b>Resist</b> LWR - < 1.5nm 3s Dose - Adequate for Throughput Resolution < 20nm 1/2 Pitch	<b>Resist</b> Viscosity - Throughput
<b>Masks</b> Multilayer Defect Densities < 0.003/cm <sup>2</sup> Actinic Blank Inspection - Phase Defects Substrate Inspection - Phase Defect Source EUV Aerial Image Metrology (AIMs) - Defect Review EUV Actinic Pattern Inspection Defect-Free Reticle Handling	<b>Image Verification</b> Patterning Repeating Error - Defect Checking	<b>Imprinting System</b> Throughput Defects Overlay
<div style="display: flex; justify-content: center; gap: 20px;"> <div style="display: flex; align-items: center;"> <div style="width: 20px; height: 15px; background-color: red; margin-right: 5px;"></div> <span>Needs Invention to Reach Manufacturing Numbers</span> </div> <div style="display: flex; align-items: center;"> <div style="width: 20px; height: 15px; background-color: yellow; margin-right: 5px;"></div> <span>Needs 3X Improvement or More</span> </div> <div style="display: flex; align-items: center;"> <div style="width: 20px; height: 15px; background-color: lightgreen; margin-right: 5px;"></div> <span>Needs Less Than 3X Improvement</span> </div> </div>		

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
DRAM ½ pitch (nm) (contacted)	<u>52</u>	<u>45</u>	<u>40</u>	<u>36</u>	<u>32</u>	<u>28</u>	<u>25</u>	<u>23</u>	<u>20</u>	<u>18</u>
<b>DRAM</b>										
DRAM ½ pitch (nm)	52	45	40	36	32	28	25	23	20	18
CD control (3 sigma) (nm) [B]	5	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1	1.9
Contact in resist (nm)	57	50	44	39	35	31	28	25	22	20
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18
Overlay [A] (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1	4.5	4.0	3.6
k1 193 / 1.35NA	0.36	0.31	0.28	0.25	0.22	0.20	0.18	0.16	0.14	0.12
k1 EUVL		0.83	0.74	0.66	0.59	0.52	0.47	0.58	0.52	0.46
<b>Flash</b>										
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16	14	13
CD control (3 sigma) (nm) [B]	4	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
Contact Pitch (nm)	219	190	170	151	135	120	107	95	85	76
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18
Overlay [A] (3 sigma) (nm)	12	10.5	9.4	8.3	7.4	6.6	5.9	5.3	4.7	4.2
k1 193 / 1.35NA	0.26	0.22	0.20	0.18	0.16	0.14	0.12	0.11	0.10	0.09
k1 EUVL		0.61	0.55	0.49	0.43	0.39	0.33	0.41	0.37	0.33
<b>MPU</b>										
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	54	45	38	32	27	24	21	19	17	15
MPU gate in resist (nm)	47	41	35	31	28	25	22	20	18	16
MPU physical gate length (nm) *	29	27	24	22	20	18	17	15	14	13
Gate CD control (3 sigma) (nm) [B] **	3.0	2.8	2.5	2.3	2.1	1.9	1.7	1.6	1.5	1.3
Contact in resist (nm)	66	56	47	39	33	29	26	23	21	19
Contact after etch (nm)	60	51	43	36	30	27	24	21	19	17
Overlay [A] (3 sigma) (nm)	13	11	9.5	8.0	6.7	6.0	5.3	4.7	4.2	3.8
k1 193 / 1.35NA	0.37	0.31	0.26	0.22	0.19	0.17	0.15	0.13	0.12	0.11
k1 EUVL		0.83	0.70	0.59	0.50	0.44	0.39	0.49	0.44	0.39
<b>Chip size (mm<sup>2</sup>)</b>										
Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm <sup>2</sup> )	858	858	858	858	858	858	858	858	858	858
Wafer site flatness at exposure step (nm) [C]	48	42	37	33	29	26	23	20	18	16
Number of mask levels MPU	35	35	35	35	37	37	37	37	39	39
Number of mask levels DRAM	24	26	26	26	26	26	26	26	26	26
Wafer size (diameter, mm)	300	300	300	300	300	450	450	450	450	450

NA required for Flash (single exposure)	1.43	1.70	1.91	2.14						
NA required for logic (single exposure)	1.16	1.38	1.64	1.94	2.31					
NA required for double exposure (Flash)	1.02	1.22	1.36	1.53	1.72	1.93	2.17			
NA required for double exposure (logic)	0.80	0.95	1.12	1.34	1.59	1.78	2.00			

EUV NA minimum 0.25 0.25 0.25 0.25 0.25 0.25 0.25 0.25 0.25 0.25 0.25

# 2009 Litho Requirements

*Table LITH3 Lithography Technology Requirements* Version 2 - 05/08/2009

Year of Production	2009	2010	2011	2012	2013
DRAM ½ pitch (nm) (contacted)	<u>52</u>	<u>45</u>	<u>40</u>	<u>36</u>	<u>32</u>
<b>DRAM</b>					
DRAM ½ pitch (nm)	52	45	40	36	32
CD control (3 sigma) (nm) [B]	5	4.7	4.0	3.7	3.0
Contact in resist (nm)	57	45	40	36	32
Contact after etch (nm)	52	45	40	36	32
Overlay [A] (3 sigma) (nm)	10	9.0	8.0	7.1	6.4
k1 193 / 1.35NA	0.36	0.31	0.28	0.25	0.22
k1 EUVL		0.83	0.74	0.66	0.59
<b>Flash</b>					
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23
CD control (3 sigma) (nm) [B]	4	3.3	2.9	2.6	2.3
Contact in resist (nm)	42	35	31	28	25
Contact after etch (nm)	38	32	28	25	23
Overlay [A] (3 sigma) (nm)	12	10.5	9.4	8.3	7.4
k1 193 / 1.35NA	0.26	0.22	0.20	0.18	0.16

Single Litho Tool Overlay

# Table Sub Teams

- Litho – US, Japan, EU - Tables 1, 2, 3,
- EUVL Masks
  - David Chan – Hayashi-san
- Optical Masks Table 5
  - Hayashi-san (DNP)
- Double Patterning - New
  - Harry Levinson Greg Hughes
- Resist Table 4 Team
  - Ted Fedynshyn, Will Conley
- Imprint Masks
  - Doug Resnick and Lloyd Litt
  - Other member- Hayashi-san
- Maskless
  - John Wiesner and Paul Petric



# Optical Masks Table 5

- Hayashi-san (DNP)
  - Mr. Yasushi Ohkubo of HOYA
  - Mr. Yoji Tonooka of Toppan
  - Mr. Iwao Higashikawa of Toshiba

# Optical Mask - Excel

Mask Team UpDate

1. IP: from max to 3-sigma -> Agreed
2. Defect size coloring : from red to yellow for 43-33nm -> Better to remain red because of high uncertainty for the sensitivity and productivity of the inspection technology. However, if there are some background data of inspection technology candidate, we can re-
3. Other coloring for optical mask table: -> There are no specific requirement to change coloring from

## Mask Table Items

	Items	Spec. Numbers	Comments
	Attenuated PSM transmission mean deviation from target	No change	
Corrected	Attenuated PSM transmission uniformity (% of target transimission, range)	May change to 3 % at 2011	Delete +/-, because of range number
	Attenuated PSM phase mean deviation from (± degree) [U]	No change	Case of not 180 degree requirement
Added	<b>Attenuated PSM phase uniformity ( degree , range) [T]</b>	<b>3 degree</b>	Re-defined as alternating PSM
	Alternating PSM phase mean deviation from nominal phase angle target (± degree) [T]	No change	
	Alternating PSM phase uniformity (degree, range) [U]	No change	number



# EUV Team Members

Scanner Companies	ASML	John Zimmerman
	Canon	Miyake Akira
	Nikon	Tsuneyuki Hagiwara
Consortium	SELETE	Kazuya Ota
	SELETE	Tsuneo Terasawa
	IMEC	Rik Jonckheere
	SEMATECH	David Chan
	SEMATECH	Greg Hughes
	SEMATECH	Abbas Rastagar
Users	Intel	Ted Liang
	Samsung	Seongsue Kim
	Global Foundries	Bruno La Fontaine
	UMC	George Huang
	Toshiba	Hiroyuki Mizuno
	Hynix	Changmoon Lim
University / Nat. Lab	LBL	Patrick Naulleau
Material Suppliers	AGC	Yoshiaki Ikuta
	Hoya	Tsutomu Shoki
Mask Shops	DNP	Naoya Hayashi
	Toppan	Craig West
	AMTC	Karten Bubke



# EUV Table Changes - Excel

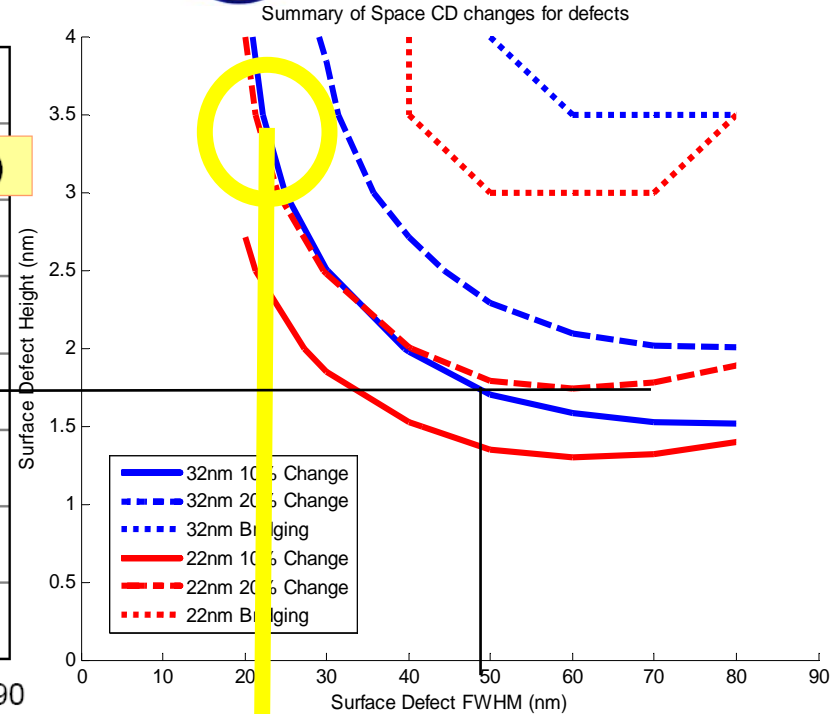
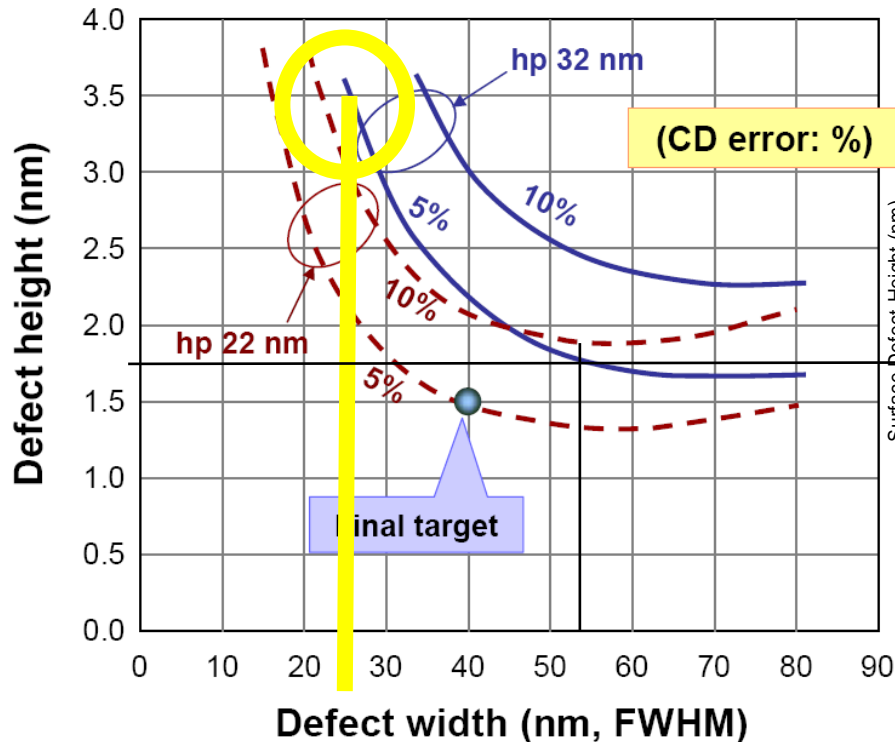
#	Parameters	Conclusions from Taskforce
1	Mask Magnification	No change
2	Nominal Image Size	No change
3	Minimum Primary Size	No change in numbers. Change color white to 99nm, yellow to 70nm, and red below 70nm. Get optical mask team to agree.
4	Image Placement	Change maximum to 3 sigma in definition. No change on numbers. Get optical mask team to agree.
5	CDU - Iso	No change
6	CDU - Dense	No change
7	CDU - Contact	No change
8	Linearity	No change
9	Mean to Target	No change
10	Defect Size	No change in numbers. Change color yellow from 43nm to 32nm and red below 30nm. Get optical mask team to agree.
11	Data Volume	No change
12	Design Grid	Change to 1% DRAM hp*mag
13	Substrate Defect Size	No change in numbers. Change subject heading to <b>Blank Defect Size</b> . Blank defect definition include substrate, ML, and cap layer. Absorber layer is not included.
14	Mean Peak Reflectivity	Change to Constant across time at > 65%. Need to ID champion for next revision.
15	Peak Reflectivity Unif	No change. Need to ID champion for next revision.
16	Centroid Unif	No change. Need to ID champion for next revision.
17	Sidewall Angle	No change
18	Absorber LER	Converting # to LWR. Sqrt(2)* 3% Minimum Primary Mask Feature as equation - Colors Yellow for 3.7 and Red below
19	Substrate Flatness	No change
20	Flatness w/ Compensation	Not add as new parameter. Address in next revision.
21	Surface Roughness	Not add as new parameter. Need to champion to work with Patrick Naulleau for next revision.
22	Defect Density	Not add as new parameter.
23	Absorber Thickness	Not add as new parameter.
24	Illumination Angle	Not add as new parameter. Add as footnote to #14, 15, 16.
25	Local Slope Backside	John Zimmerman will propose numbers for taskforce to consider. Try to make it to this revision.
26	FWHM	John Zimmerman will propose numbers for taskforce to consider. Try to make it to this revision.
27	Bow	John Zimmerman will propose numbers for taskforce to consider. Try to make it to this revision.

<i>Year of Production</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>
<i>DRAM ½ pitch (nm) (contacted)</i>	52	45	40	36	32
<i>Overlay</i>	10.3	9.0	8.0	7.1	6.4
<i>Contact after etch (nm)</i>	60	51	43	36	30
<i>Generic Mask Requirements</i>					
<i>Mask magnification [B]</i>	4	4	4	4	4
<i>Mask nominal image size (nm) [C]</i>	186	162	141	126	112
<i>Mask minimum primary feature size [D]</i>	130	114	99	88	78
<i>Image placement (nm, multipoint) [E]</i>	6.2	5.4	4.8	4.3	3.8
<i>CD uniformity (nm, 3 sigma) [F]</i>					
<i>Isolated lines (MPU gates)</i>	4.4	4.0	3.7	3.3	3.0
<i>Dense lines DRAM (half pitch)</i>	7.5	6.5	5.8	5.2	4.6
<i>Contact/vias</i>	7.2	5.0	4.4	4.0	3.5
<i>Linearity (nm) [G]</i>	7.9	6.8	6.1	5.4	4.8
<i>CD mean to target (nm) [H]</i>	4.1	3.6	3.2	2.9	2.5
<i>Defect size (nm) [I]</i>	41	36	32	29	25
<i>Data volume (GB) [J]</i>	520	655	825	1048	1310
<i>Mask design grid (nm) [K]</i>	2	2	2	1	1
<i>EUVL-specific Mask Requirements</i>					
<i>Substrate defect size (nm) [L]</i>	41	39	37	35	34
<i>Blank defect size (nm) [L2]</i>	41	36	32	29	25
<i>Mean peak reflectivity</i>	>65%	>65%	>65%	>65%	>65%
<i>Peak reflectivity uniformity (% 3 sigma absolute)</i>	0.58%	0.47%	0.42%	0.37%	0.33%
<i>Reflected centroid wavelength uniformity (nm 3 sigma) [M]</i>	0.07	0.06	0.05	0.05	0.05
<i>Absorber sidewall angle tolerance (± degrees) [P]</i>	1	0.75	0.69	0.62	0.5
<i>Absorber LWR (3 sigma nm) [N]</i>	5.5	4.8	4.2	3.7	3.3
<i>Mask substrate flatness (nm peak-to-valley) [O]</i>	59	51	46	41	36

# Blank Defect Size

- E-mail Compromise between ITWG
  - Japan – SELETE Data
  - USA – Berkley Modeling C. Clifford
  - IMEC – Rik Jonckheere

# Comparison to Selete Data



This data matches very well. Selete is measuring the bump in one dark line. Clifford is measuring the space CD. The space CD change is two times larger than the bump in the dark line for a defect centered between the lines and normal incidence.

**Selete's 5% and 10% lines can be compared to my 10% and 20% lines**

[L2] Blank Defect Size —A blank defect is any unintended blank anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear “defect” that is expected to print for the stated generation. This includes phase defects that may come from the substrate or multilayer. A phase defect is a defect that causes a phase change of around 180 deg. (For EUVL this would normally be a 3.5 nm height change.) It should be noted that smaller phase defects will also print but at a larger size limit. (ie a 90 deg defect will print at about 2X the size of the 180 deg defect)



# Double Patterning / Spacer Requirements

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016
DRAM/ MPU/ ASIC (M1) ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23
DRAM CD control (3 sigma) (nm)	5.4	4.7	4.2	3.7	3.3	2.9	2.6	2.3
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	32	27	24	21	19
MPU gate in resist (nm)	47	41	35	31	28	25	22	20
MPU physical gate length (nm)	29	27	24	22	20	18	17	15
Gate CD control (etched) (3 sigma) (nm)	3.0	2.8	2.5	2.3	2.1	1.9	1.7	1.6
Overlay (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1	4.5
Contact in resist (nm)	66	56	47	39	33	29	26	23

## Generic Pitch Splitting - Double Patterning Requirements Driven by MPU metal 1/2 Pitch

Mean CD Difference in DP Lines							0.4	0.4	0.3
Pooled Dual Line CD control (3 sigma) (nm)							2.0	1.8	1.7
Max. mean overlay for MPU LFLE or LELE							0.4	0.3	0.3
Overlay 3s for MPU LFLE or LELE	5.5	4.6	3.8	3.1	2.6	2.3	2.0	1.8	
Printed Dependent Space CD control for MPU LFLE-LELE (nm,3s)	6.4	5.4	4.5	3.8	3.2	2.9	2.5	2.3	

## Generic Spacer Patterning Requirements - Driven By Flash

Nominal printed duty cycle					1:3	1:3	1:3	1:3	1:3
Core Gap (Line) CD Control (3 sigma) (nm)					2.0	1.8	1.6	1.4	1.3
Line - Deposited Sidewall Thickness uniformity (nm)					1.3	1.1	1.0	0.9	0.8
Space Uniformity (Bi-Modal) 3 sigma	4.5	3.8	3.4	3.0	2.7	2.4	2.1	1.9	
Mean CD Differce causing Bi-modal Spacce CD	0.69	0.58	0.52	0.46	0.41	0.37	0.33	0.29	
Overlay for spacer process	11.9	10.0	8.9	8.0	7.1	6.3	5.6	5.0	

## Generic Mask Requirements

Mask magnification [B]	4	4	4	4	4	4	4	4
Mask nominal imag			141	126	112	100	89	79
Mask minimum prin			99	88	78	70	62	55
Mask sub-resolution feature size (nm) opaque [E]	93	81	71	63	56	50	44	40
Image placement (nm, multipoint) [F]	6.2	5.4	4.8	4.3	3.8	3.4	3.0	2.7
CD mean to target (nm) [M]	4.1	3.6	3.2	2.9	2.5	2.3	2.0	1.8

## Pitch Splitting - Double Patterning Specific Mask Rquirements

Image placement (nm, multipoint) for double patterning of dependent layers [V]	4.4	3.8	3.4	3.0	2.7	2.4	2.1	1.9
Difference in CD Mean-to-target for two masks used as a double patterning set (nm) [W]	2.1	1.8	1.6	1.4	1.3	1.1	1.0	0.9

# Double Patterning (LELE)

# Spacer Patterning

# Mask Requirments

# Double Patterning & Spacer

- Greg Hughes
- Harry Levinson (Global Foundries)
- Andrew J. Hazelton (Nikon)
- Christopher Bencher (Applied Materials)
- Mauro Vasconi (Numonyx)

Table LITH5B Double Patterning / Spacer Requirements

Year of Production	2009	2010	2011	2012	2013	2014	2015
DRAM/ MPU/ ASIC (M1) ½ pitch (nm) (contacted)	52	45	40	36	32	28	25
DRAM CD control (3 sigma) (nm)	5.4	4.7	4.2	3.7	3.3	2.9	2.6
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	32	27	24	21
MPU gate in resist (nm)	47	41	35	31	28	25	22
MPU physical gate length (nm)	29	27	24	22	20	18	17
Gate CD control (contacted) (3 sigma) (nm)	3.0	2.8	2.5	2.3	2.1	1.9	1.7
Overlay (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1
Contact resist (nm)	66	56	47	39	33	29	26
<b>Generic Pitch Splitting - Double Patterning Requirements Driven by MPU metal 1/2 Pitch</b>							
Mean CD Difference in DP Lines	0.9	0.8	0.6	0.5	0.5	0.4	0.4
Pooled Dual Line CD control (3 sigma) (nm)	3.3	3.0	2.7	2.4	2.2	2.0	1.8
Max. mean overlay for MPU LFLE or LELE	0.8	0.7	0.6	0.5	0.4	0.4	0.3
Overlay 3s for MPU LFLE or LELE	5.5	4.6	3.8	3.1	2.6	2.3	2.0
Printed Dependent Space CD control for MPU LFLE-LELE (nm,3s)	6.4	5.4	4.5	3.8	3.2	2.9	2.5
<b>Generic Spacer Patterning Requirements - Driven By Flash</b>							
Nominal printed duty cycle	1:3	1:3	1:3	1:3	1:3	1:3	1:3
Core Gap (Line) CD Control (3 sigma) (nm)	3.0	2.5	2.3	2.0	1.8	1.6	1.4
Line - Deposited Sidewall Thickness uniformity (3 sigma) (nm)	1.9	1.6	1.4	1.3	1.1	1.0	0.9
Space Uniformity (Bi-Modal) 3 sigma	4.5	3.8	3.4	3.0	2.7	2.4	2.1
Mean CD Difference causing Bi-modal Spacce CD	0.69	0.58	0.52	0.46	0.41	0.37	0.33
Overlay for spacer process	11.9	10.0	8.9	8.0	7.1	6.3	5.6

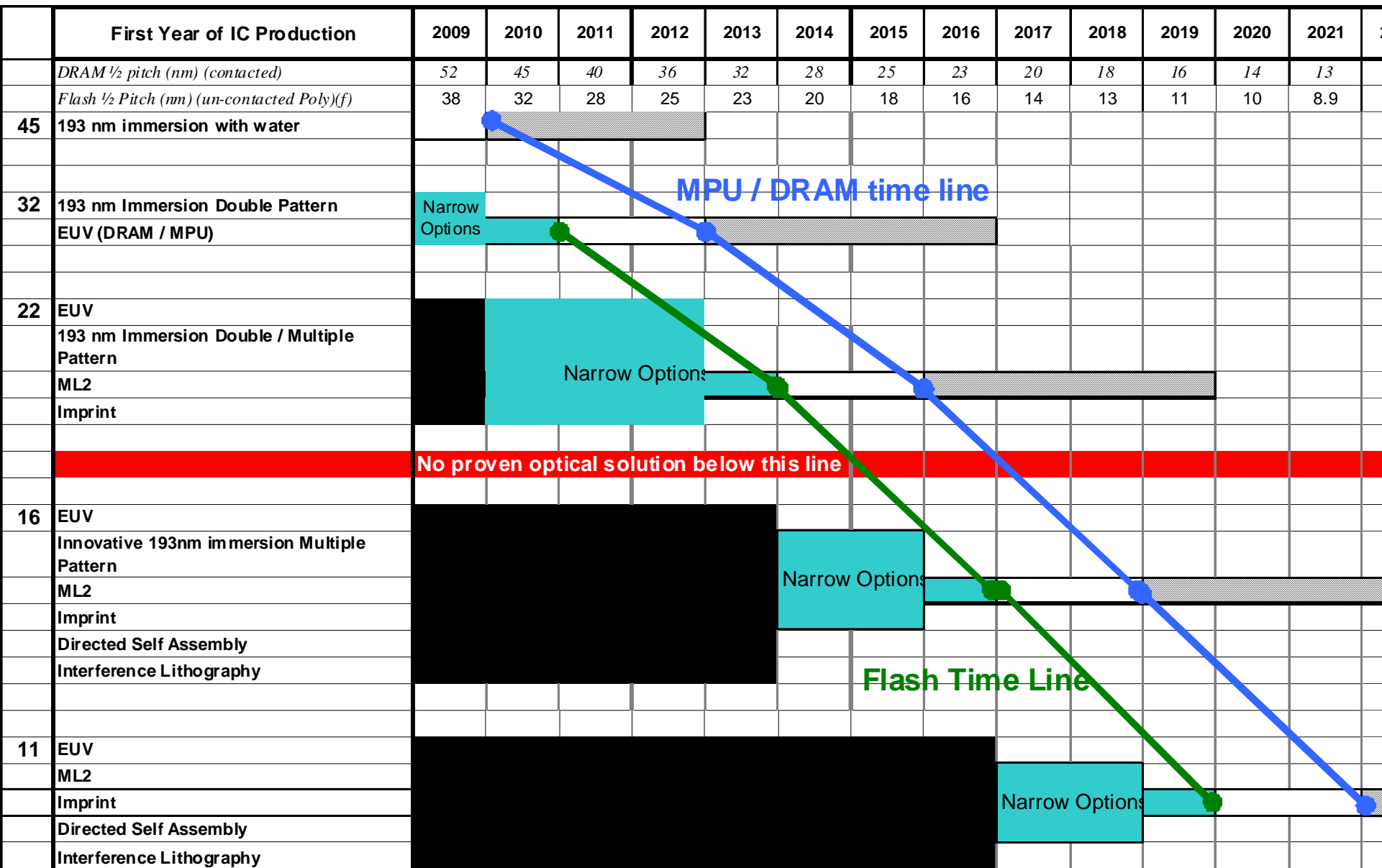
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FROZEN FINAL ORTC FILE VERSION 8--08/27/200

## Table LITH5B Double Patterning / Spacer Requirements

Year of Production	2009	2010	2011	2012	2013
DRAM/ MPU/ ASIC (M1) ½ pitch (nm) (contacted)	52	45	40	36	32
<b>Generic Mask Requirements</b>					
Mask magnification [B]	4	4	4	4	4
Mask nominal image size (nm) [C]	186	162	141	126	112
Mask minimum primary feature size [D]	130	114	99	88	78
Mask sub-resolution feature size (nm) opaque [E]	93	81	71	63	56
Image placement (nm, multipoint) [F]	6.2	5.4	4.8	4.3	3.8
CD mean to target (nm) [M]	4.1	3.6	3.2	2.9	2.5
<b>Pitch Splitting - Double Patterning Specific Mask Requirements</b>					
Image placement (nm, multipoint) for double patterning of dependent layers [V]	4.4	3.8	3.4	3.0	2.7
Difference in CD Mean-to-target for two masks used as a double patterning set (nm) [W]	2.1	1.8	1.6	1.4	1.3

# Potential Solutions



# Summary

- Lithography solutions for 2010
  - 45 nm half-pitch CoO is Driving 193 Immersion Single Exposure for DRAM/MPU
  - Flash using Double Patterning (Spacer) for 32 nm half-pitch
- Lithography solutions for 2013
  - 32 nm half-pitch Double patterning or EUV? for DRAM/MPU
  - 22 nm half-pitch Double patterning or EUV for Flash
- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single layers
- LER and CD Control Still remain as a Dominant Issue
- Mask Complexity for Double patterning
- Mask Infrastructure for EUV