Design and System Drivers - 2009

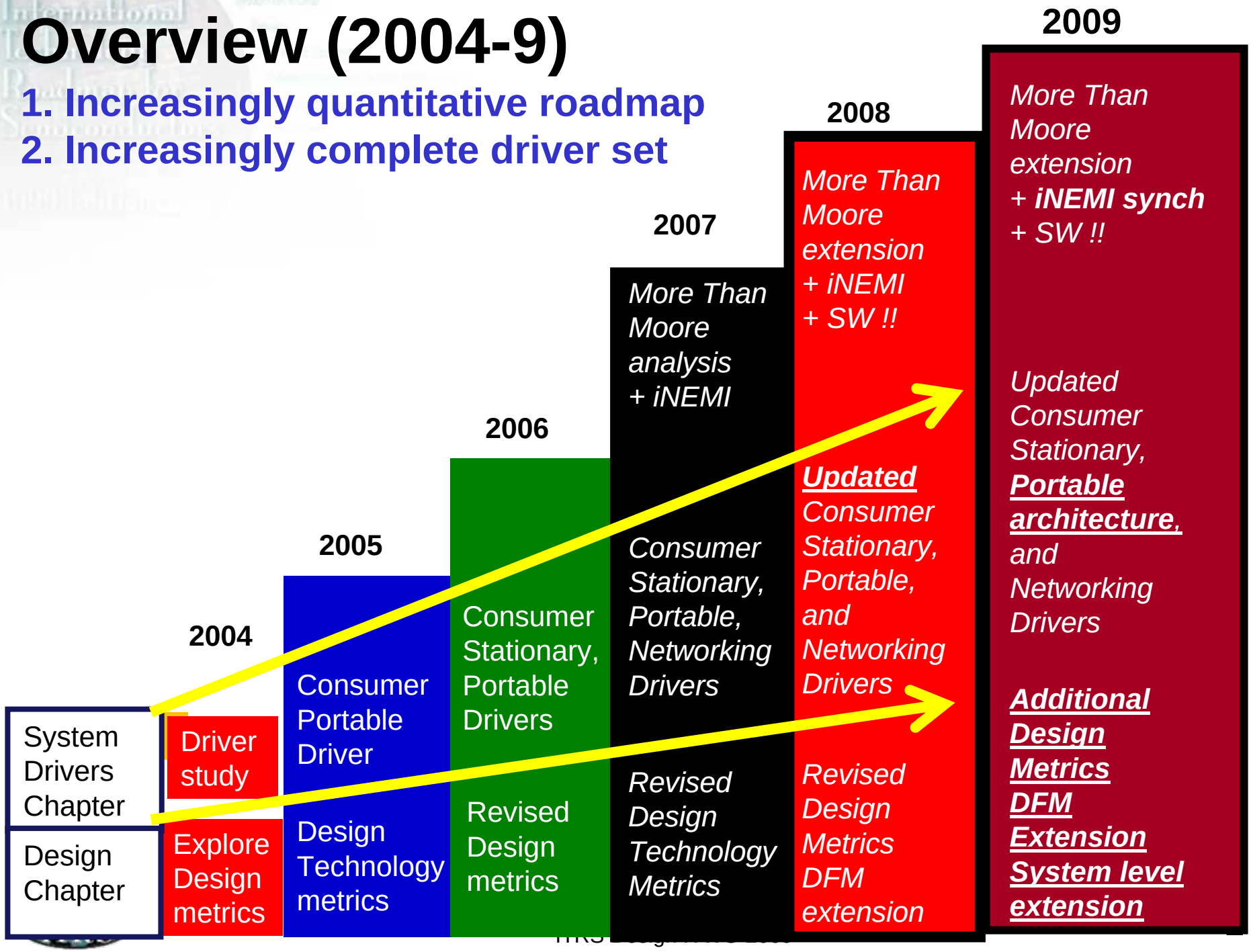
Worldwide Design ITWG

Key actions / messages:

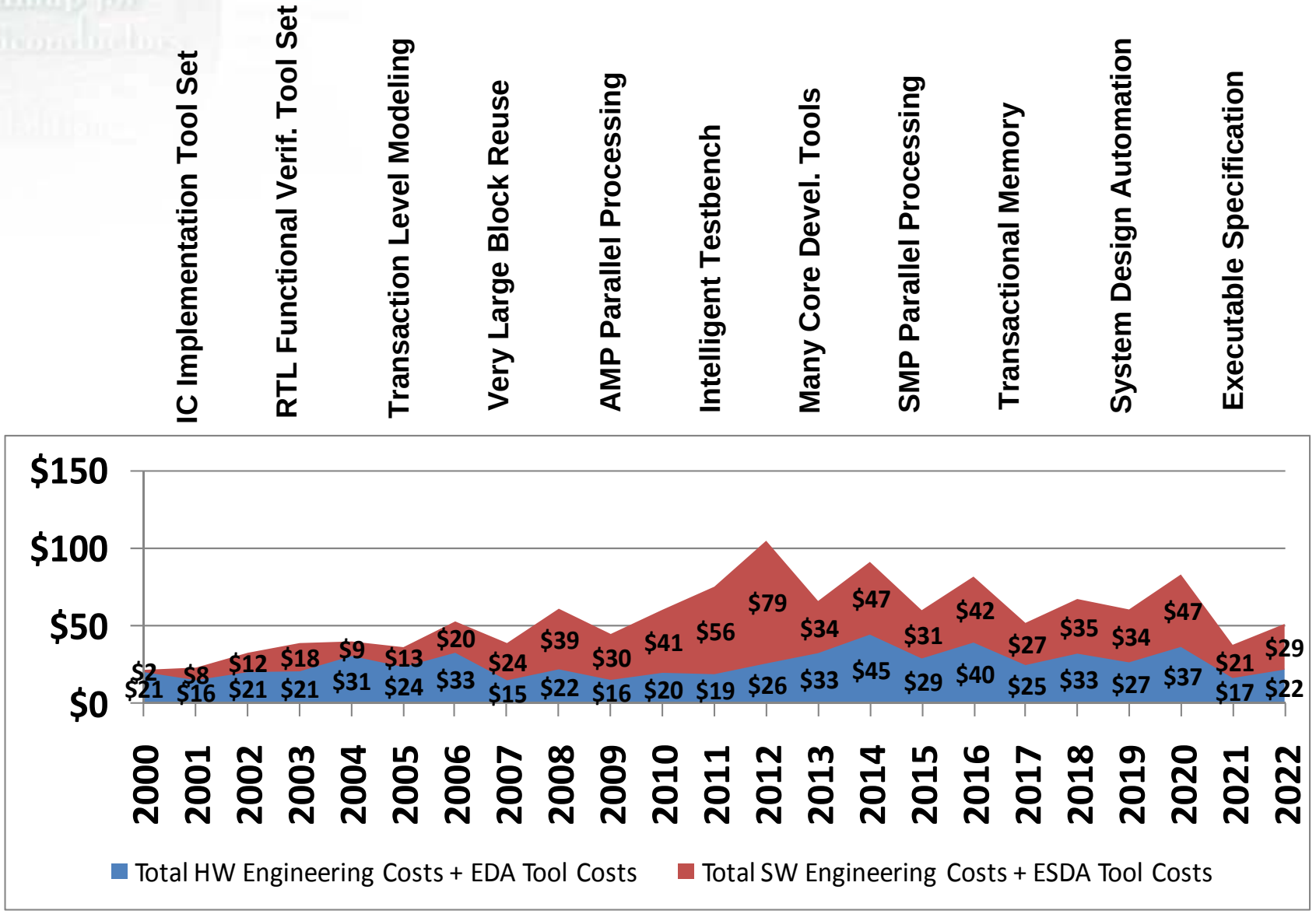
1. **Software, system level design productivity critical to roadmap**
2. **Initiated reliability / resilience roadmap**
3. **System-level design technology is key to power efficiency**
4. **Design cost will be contained through innovation**

Overview (2004-9)

1. Increasingly quantitative roadmap
2. Increasingly complete driver set

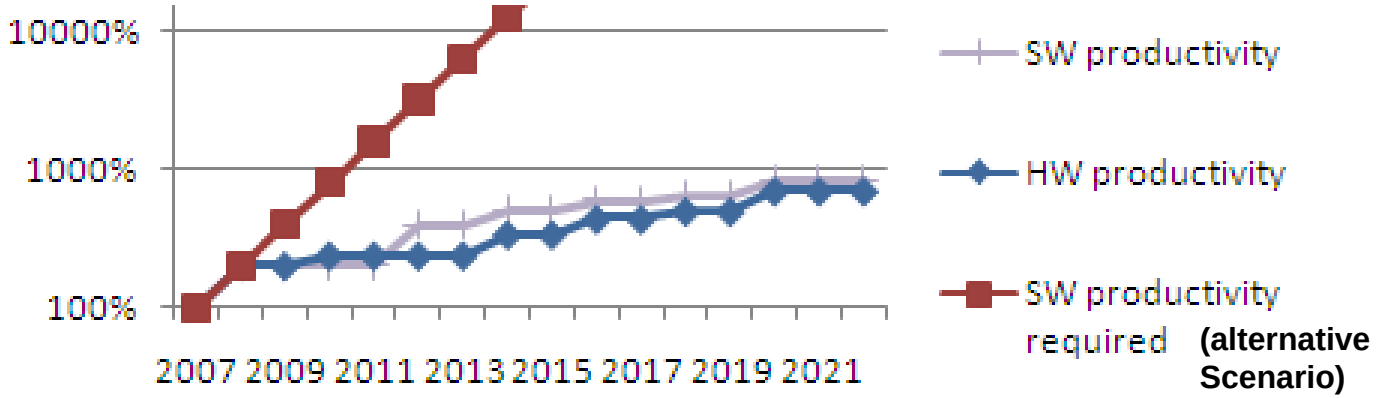


ITRS Cost Chart 2009 (Millions of Dollars)

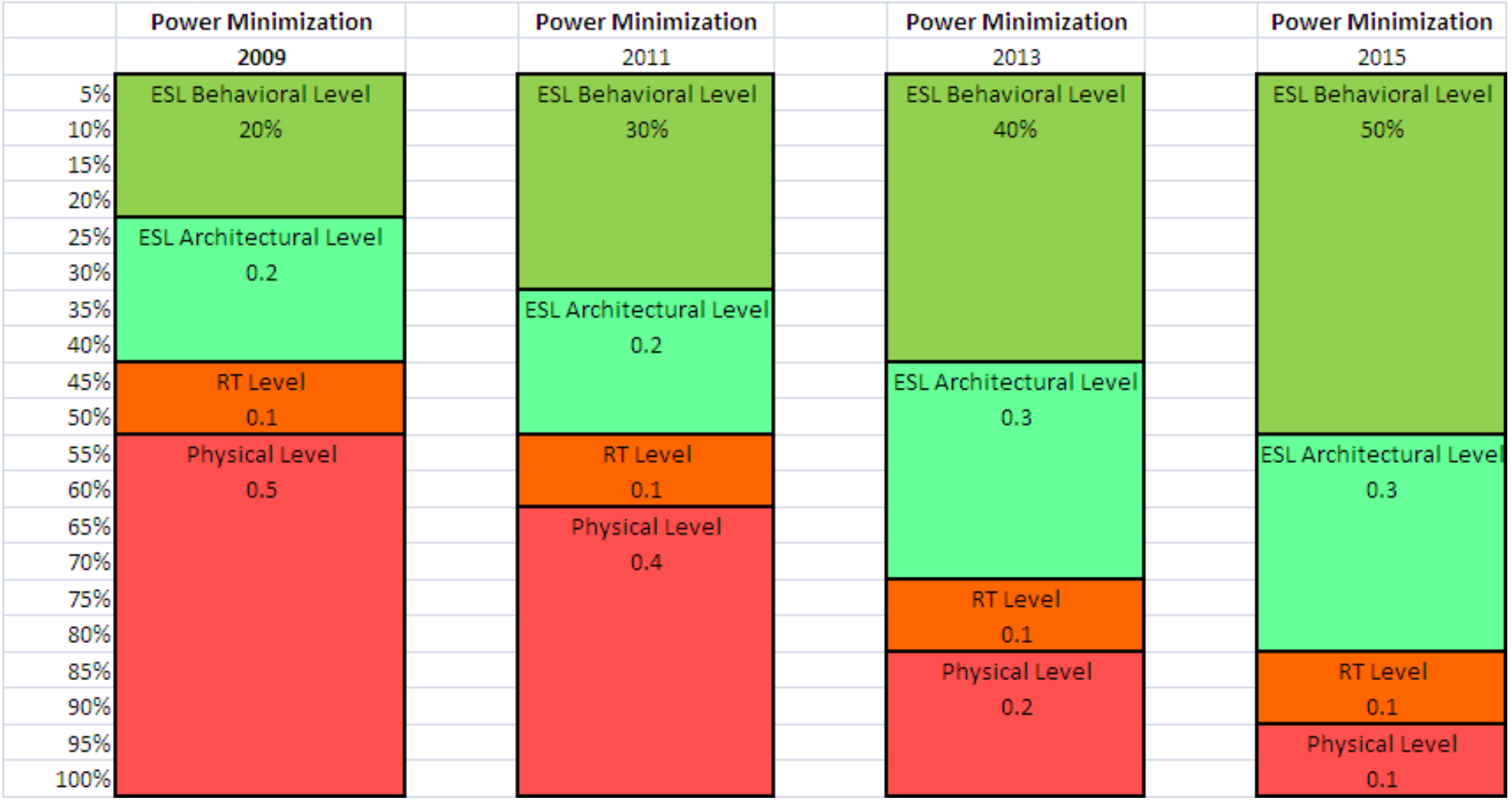


System Level Design & SOFTWARE

- **Hardware design productivity is growing appropriately**
  - Requirements correspond roughly with solutions
  - Innovations pacing properly (transistors / designer / year)
- **Large gap in software productivity possibly opening up**
  - If hardware accelerators are heavily leveraged, problem mitigated
  - Otherwise, possibly 100X gap can affect memory size, other
- **Adding new parameters to requirements/solutions tables**
  - Hardware design productivity - **requirement**
  - Software design productivity - **requirement**
  - Software design productivity (assuming only software implementation)
  - System design productivity innovations – **solutions** (Fig. 1 in chapter)



Impact of Design on Power
Emphasis on System Level [SW/HW]



Design and System Drivers - 2010

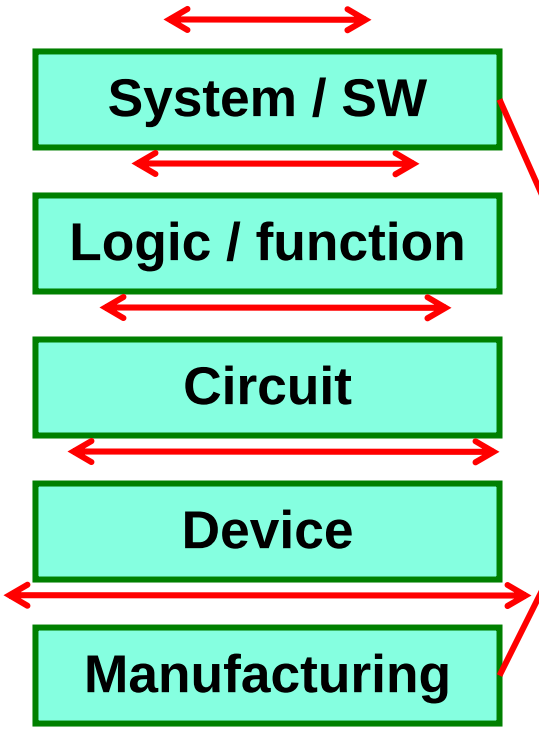
Worldwide Design ITWG

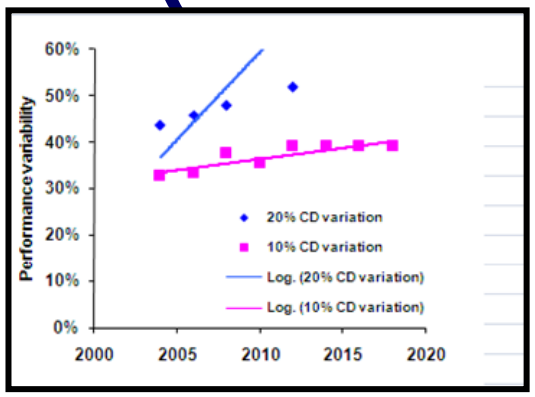
Key actions / messages:

1. **Continue expanding importance of SW and system level**
2. **Quantify design technology impact on variability, “sigma” control in process**
3. **Update “design cost control through innovation” chart**
4. **Develop design technology roadmap for 3D / TSV**
5. **Develop new set of Design requirements/solutions from MtM**
6. **Complete reliability roadmap for 2011**

Impact of Design on “Sigma” (Variability)

- **Goal**
  - Quantify “how many sigmas” can design “reduce”
- **Approach**
  - Inventory of design techniques / tools
  - Match inventory to parameters or correlations in model
  - Use variability model to capture “delta” in sigmas

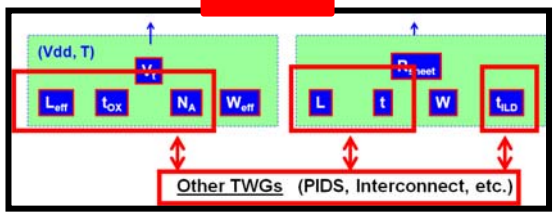




Check overall variation

	CD variation	CD % variation	delay variation	Power variation	Leakage power variation
2004	0.012	12%	44%	45%	123%
2006	0.0084	12%	46%	50%	201%
2008	0.00684	12%	48%	62%	240%
2010	0.00552	12%	61%	68%	289%
2012	0.0042	12%	52%	60%	306%
2014	0.00336	12%	77%	89%	397%
2016	0.00276	12%	89%	107%	335%
2018	0.00216	12%	93%	112%	551%
2020	0.00156	12%	115%	113%	545%
2022	0.00096	12%	126%	103%	548%

Use variability model



Inputs (manufacturing)

More Than Moore (Design)

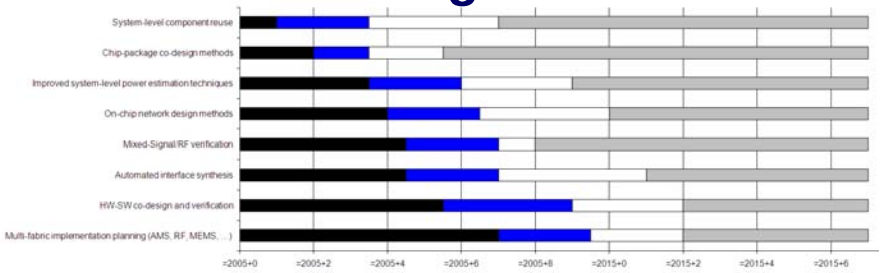
- **More than Moore brings new set of requirements/solutions**
  - Will create additional inventory of parameters

Existing

Existing requirements

TABLE 16	Year of Production		2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
	Technology Node		hp90		hp65		hp45			hp32			hp22			hp16		
Design Reuse																		
2	Design block reuse	% to all logic size	32%	33%	35%	36%	38%	40%	41%	42%	44%	46%	48%	49%	51%	52%	54%	55%
Platform Based Design																		
3	Available platforms	normalized to 100% in the start year	100%	91%	87%	83%	75%	70%	60%	55%	52%	48%	45%	43%	40%	37%	35%	32%
4	Platforms supported	% of platforms fully supported by tools	3%	6%	10%	25%	35%	50%	57%	64%	75%	80%	85%	90%	92%	94%	95%	97%
High Level Synthesis																		
5	Accuracy of high level estimates (performance, area, power, costs)	% vs. measurements	53%	56%	60%	63%	66%	70%	73%	76%	80%	83%	86%	90%	92%	94%	95%	97%
Reconfigurability																		
6	SOC reconfigurability	% of SoC functionality	23%	26%	28%	28%	30%	35%	38%	40%	42%	45%	48%	50%	53%	56%	60%	62%
Analog/Mixed Signal																		
7	Analog automation	% vs. digital automation	12%	14%	17%	17%	24%	24%	27%	30%	32%	35%	38%	40%	43%	46%	50%	52%
8	Modelling methodology, description languages, and simulation environments	% vs. digital methodology	53%	55%	58%	60%	62%	65%	67%	70%	73%	76%	78%	80%	83%	85%	90%	92%

Existing solutions



Additional

Additional requirements

Additional solutions

E.g.

- System-level (packaging)
- Circuit (inter-chip parasitics modeling/simulation)
- Layout (SiP global layout)
- DFM (package-chip, SiP DFM)

Design and System Drivers 2009

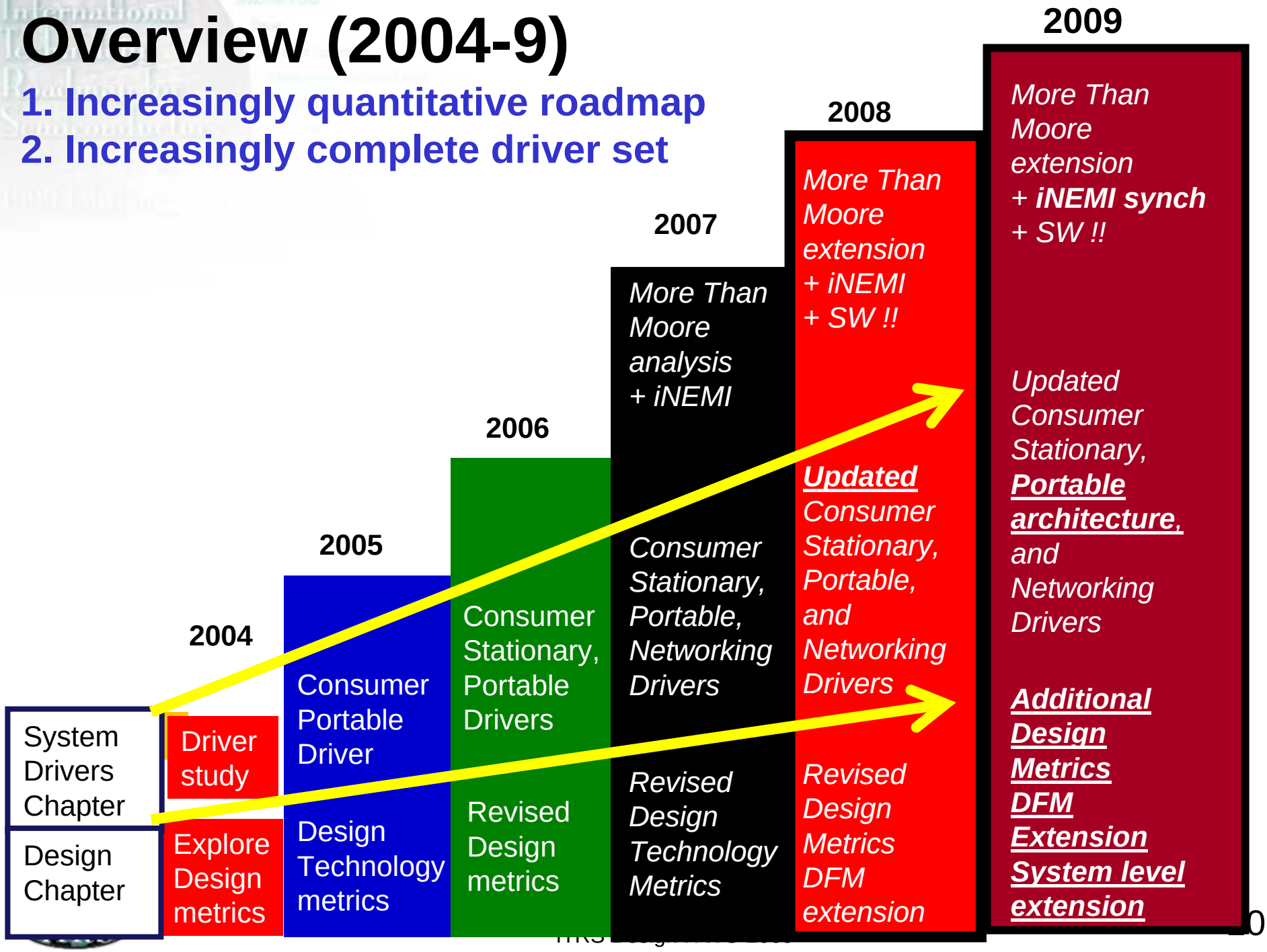
Worldwide Design ITWG

Key actions / messages:

1. **Design update to ORTCs: SRAM, logic, defect density models**
2. **Updated key system drivers: SOC-Consumer Portable, MPU**
3. **Frequency-power envelope remains critical for industry**
4. **Updated System Drivers, no new drivers**
5. **Expanded cross-TWG and public activity (DAC '09 workshop)**

Overview (2004-9)

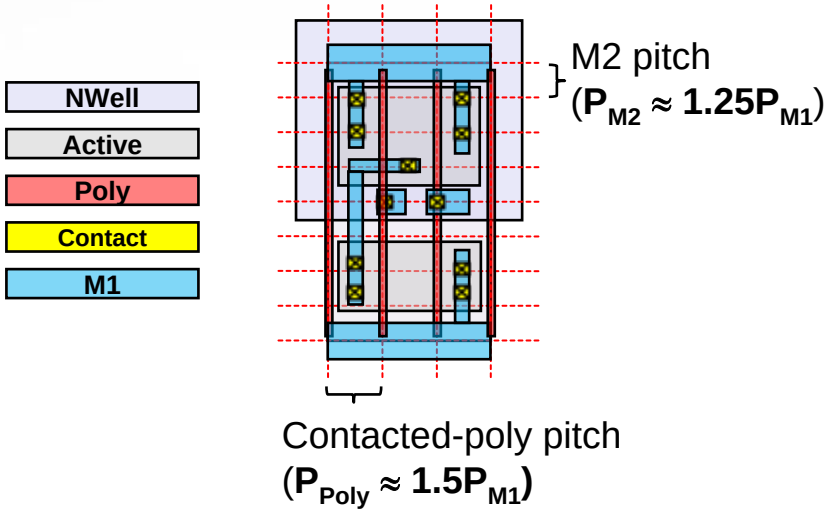
1. Increasingly quantitative roadmap
2. Increasingly complete driver set



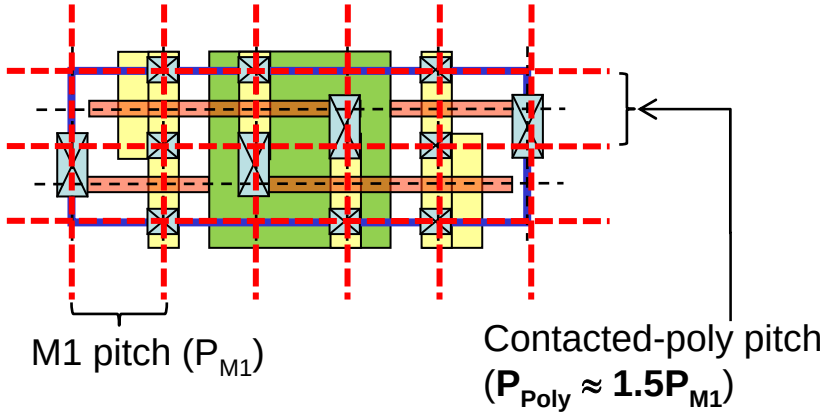
ORTCs: New A-Factor Models

(Area = A-factor × F^2)

- **Logic: A-factor = 175**



- **SRAM: A-factor = 60**



NAND2 Area

$= 3\ P_{Poly} \times 8\ P_{M2}$

$\approx (3 \times 1.5\ P_{M1}) \times (8 \times 1.25\ P_{M1})$

$= 45\ (P_{M1})^2$

$= 180\ F^2$ ➔ **175** F^2

SRAM Bitcell Area

$= 2\ P_{Poly} \times 5\ P_{M1}$

$= 3\ P_{M1} \times 5\ P_{M1} = 15\ (P_{M1})^2$

$= 15\ (2\ F)^2 =$ **60** F^2

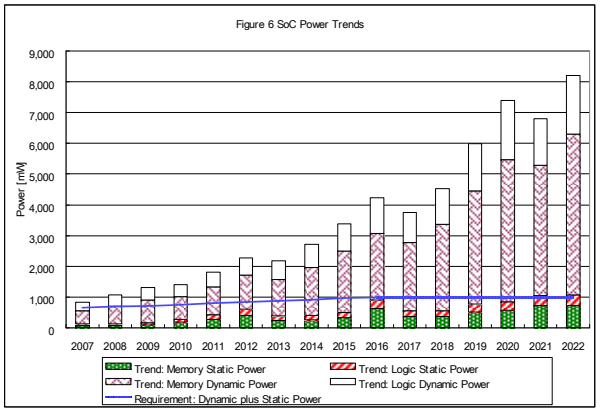
Fitted to industry data

Key System Drivers Constantly Updated

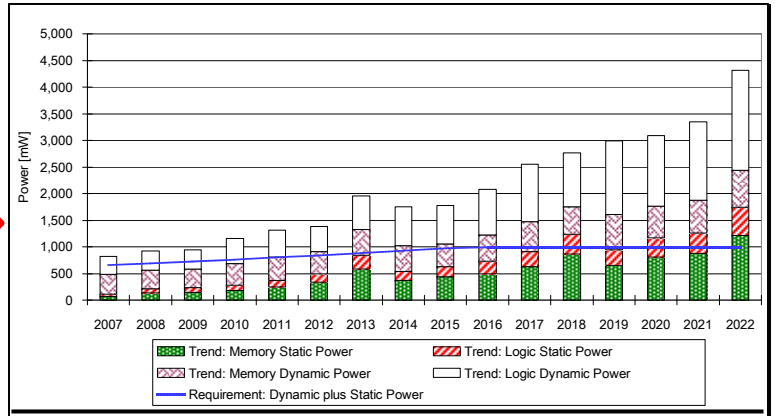
Consumer Driver Model

- **2008: Updated power model with realistic dynamic power**
  - Memory dynamic power 10X less than modeled previously

8 W max total (2022)



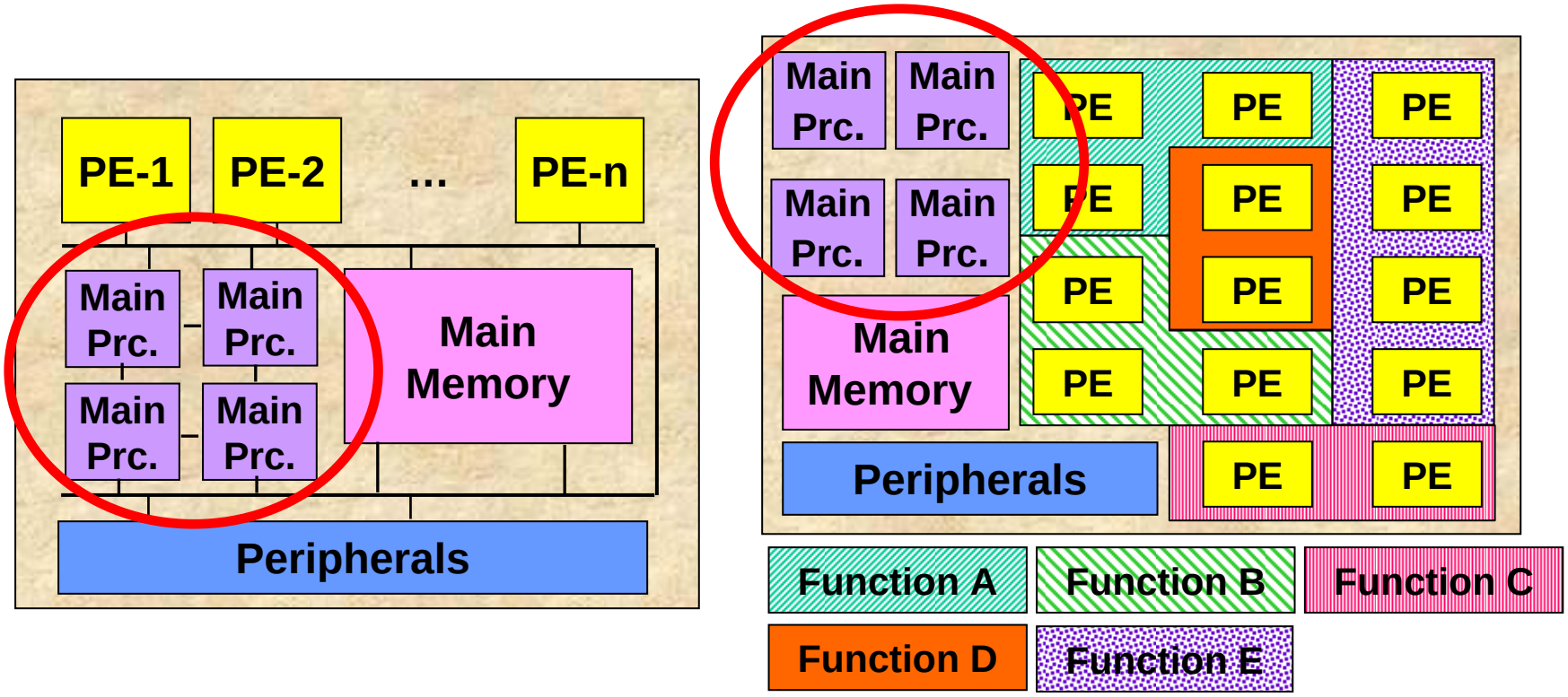
4.3 W max total (2022)



- **Will identify key driver requirements, explore coloring**
  - E.g., excessive power beyond portable limit (1 W → 0.5W)
- **Exploring RF/A/MS for future portable consumer drivers**
  - Extends existing driver (or, future "wireless" driver is possible)
- **Exploring additional parameters per Test requests**
  - #clocks, #power domains, #unique cores, #IOs, etc.

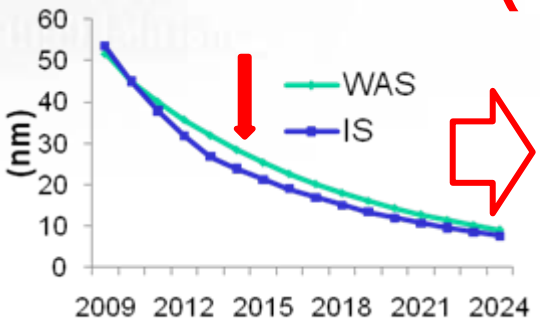
SOC Consumer Portable Architecture Model (updated)

- #Main Processors grows to 2, 4 and beyond
- Power budget reduced to 0.5W
- Die size reduces slowly to 44mm^2



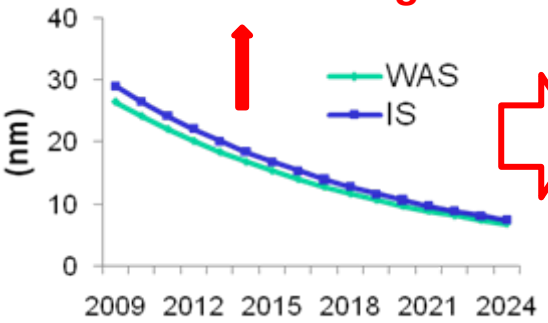
Updated MPU Density/Power/Frequency

M1 Half-Pitch (F)



Decrease P_{dyn} and P_{leak}

Physical L_{gate} (L)

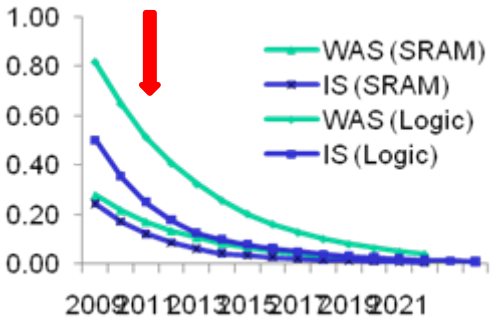


Increase P_{dyn}, decrease P_{leak}

A-Factor (A)

Logic: ~320 (WAS) → 175 (IS)
SRAM: ~100 (WAS) → 60 (IS)

Unit cell size



Growth of #Tr
2x / 3 year (WAS)
→ 2x / 2 year (IS)
up to 2013

Die size reduction
310mm² (WAS)
→ 260mm² (IS)

#core/die, #tr/core

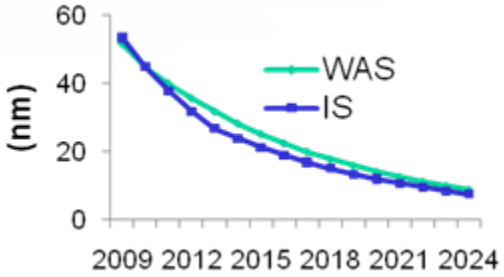
12.2% / year (WAS)
→ 18.9% / year (~2013, IS),
→ 12.2% / year (2014~, IS)

Increased P_{dyn} and P_{leak}

Design Pacing, Challenges Unabated

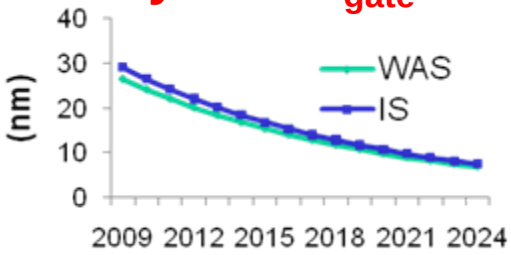
- **2009: Final Lgate and M1 HP scaling impact on Drivers**

M1 Half Pitch



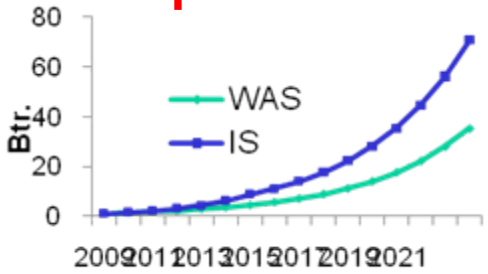
2 year delay, but faster scaling
0.7x / 3yr → 0.7 / 2yr (~2013), 0.7x / 3yr (2014~)

Physical L_{gate}



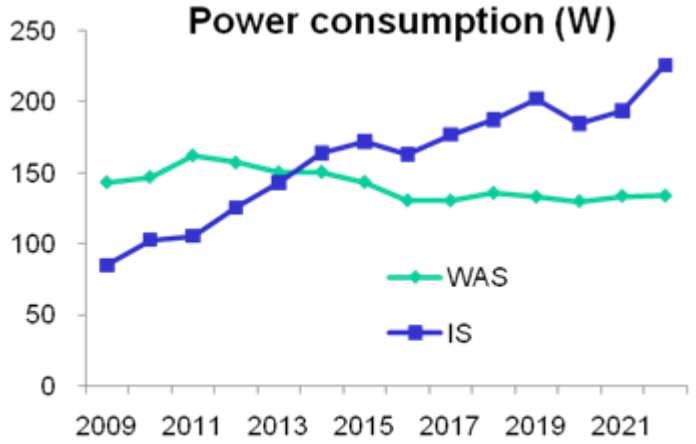
1 year shift

#Tr per die



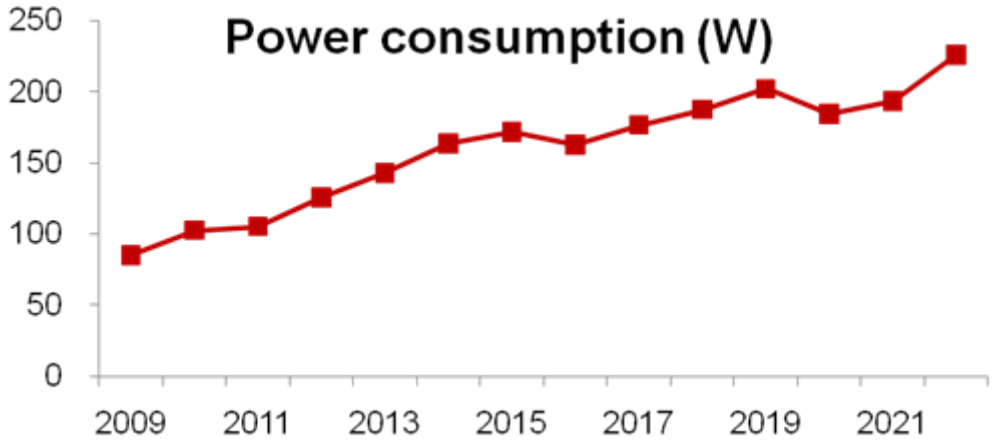
New A-factors
Faster M1 half pitch reduction

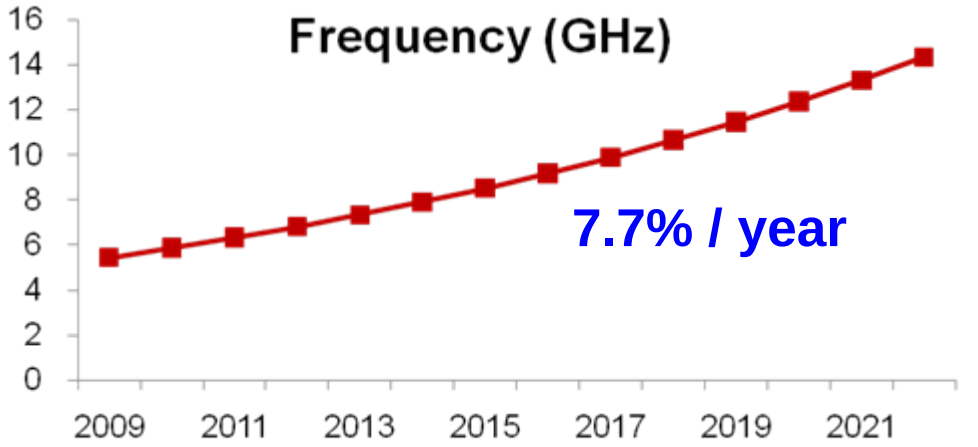
***Updated* MPU model (power)**

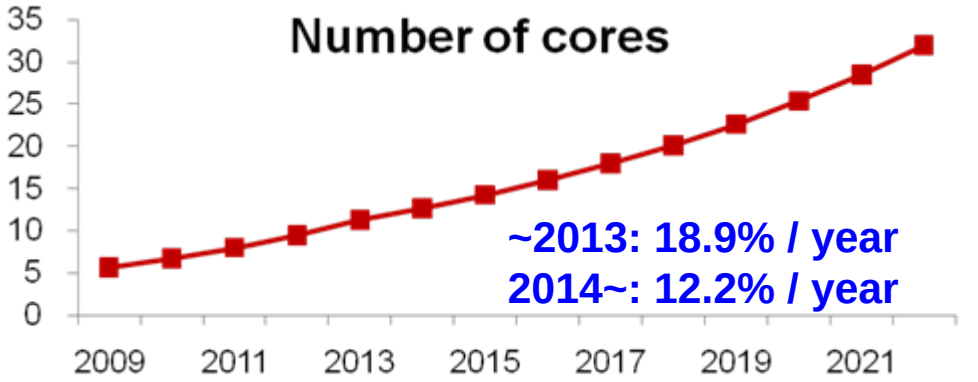


Frequency-Power Envelope Remains Critical System Issue

- **Current priorities**
  - Power #1 goal
  - Frequency slowdown
  - Multi-core enables tradeoff
- **Need to track trade-off**
  - Market vigilance
  - Yearly adjustment
  - Possible 2009 survey







DAC-2009 Roadmapping Workshop

San Francisco, July 27, 2009 9am – 3pm

35 Attendees

- **9:15am - 10:00am Plenary**
  - The ITRS Semiconductor Industry Roadmap --- Alan K. Allan (Intel)

- **10:00am - noon Session I: EDA Roadmaps and Perspectives**
  - The CATRENE (Europe) EDA Roadmap --- W. Rosenstiel (U. Tubingen)
  - The STRJ/WG1 (Japan) EDA Roadmap --- (STRJ representative)
  - The ITRS Design / System Drivers Roadmap – Carballo/Kahng (ITRS)
  - Synopsys Roadmap Perspective --- A. Domic (Synopsys)
  - Cadence Roadmap Perspective --- D. Noice (Cadence)
  - Mentor Roadmap Perspective --- R. Hum (Mentor)
  - Design Technology Coalition Perspective --- J. Darringer (IBM)
  - SI2 Perspective --- S. Dasgupta (SI2)
  - **Mini-Panel Discussion: "Can We Roadmap EDA? For whom?"**

  - **Noon - 1:30pm: Creating the Right EDA Industry Roadmap**

Design and System Drivers 2010

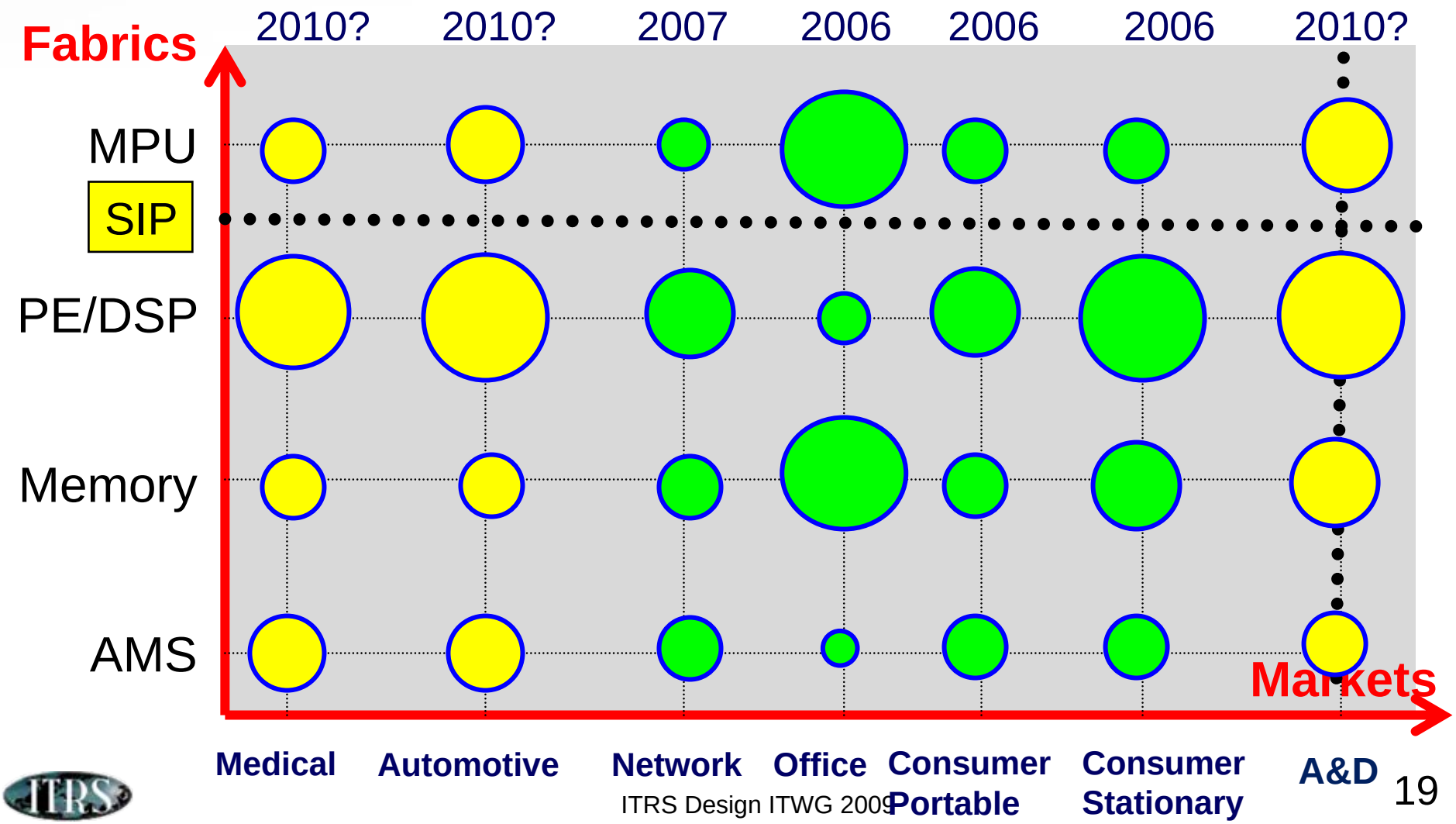
Worldwide Design ITWG

Key actions / messages:

1. **Update key system drivers: SOC-Consumer Portable, MPU**
2. **Update frequency-power MPU roadmap**
3. **Continue to broaden System Drivers, but more cautiously**
4. **Develop new "MtM" System Driver parameters, "SIP fabric"**
5. **Continue cross-TWG and public activity (DAC2010 workshop)**
6. **Maintain iNEMI relationship/linkage around portable driver**

New System Drivers? At the right pace…

- **New SIP Fabric driver effort started in 2009**
- **Others** (aerospace & defense, medical, auto, FPGA) **deferred**



More Than Moore

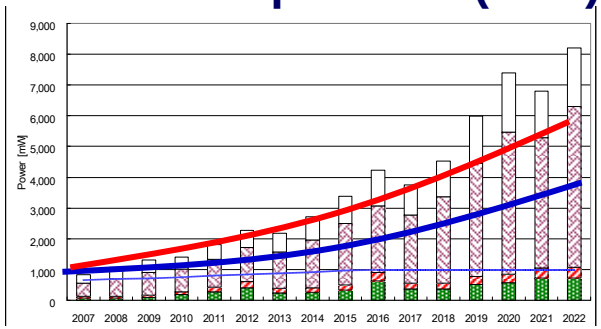
Brings Alternative Set of Parameters (2010-)

- Will create additional inventory of parameters

CONCEPT: Current SoC scenario vs. Additional SiP scenario

System Drivers

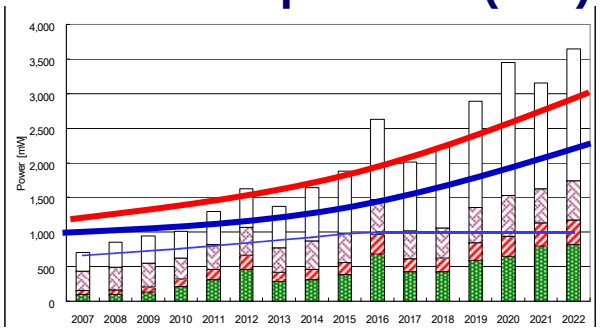
Consumer portable (SoC)



Power

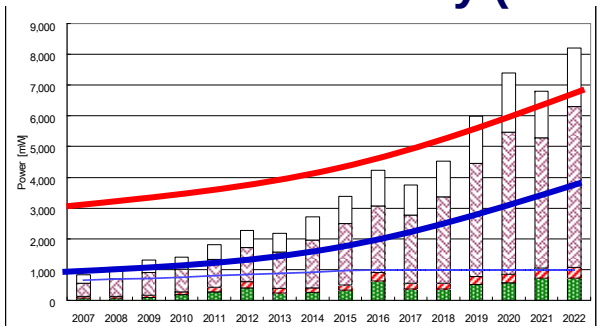
Normalized Cost

Consumer portable (SiP)



System Drivers

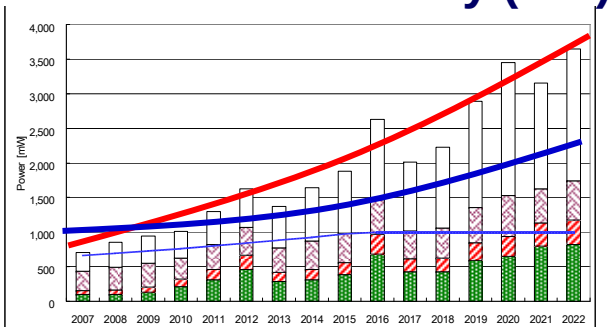
Consumer stationary (SoC)



Performance

Normalized Cost

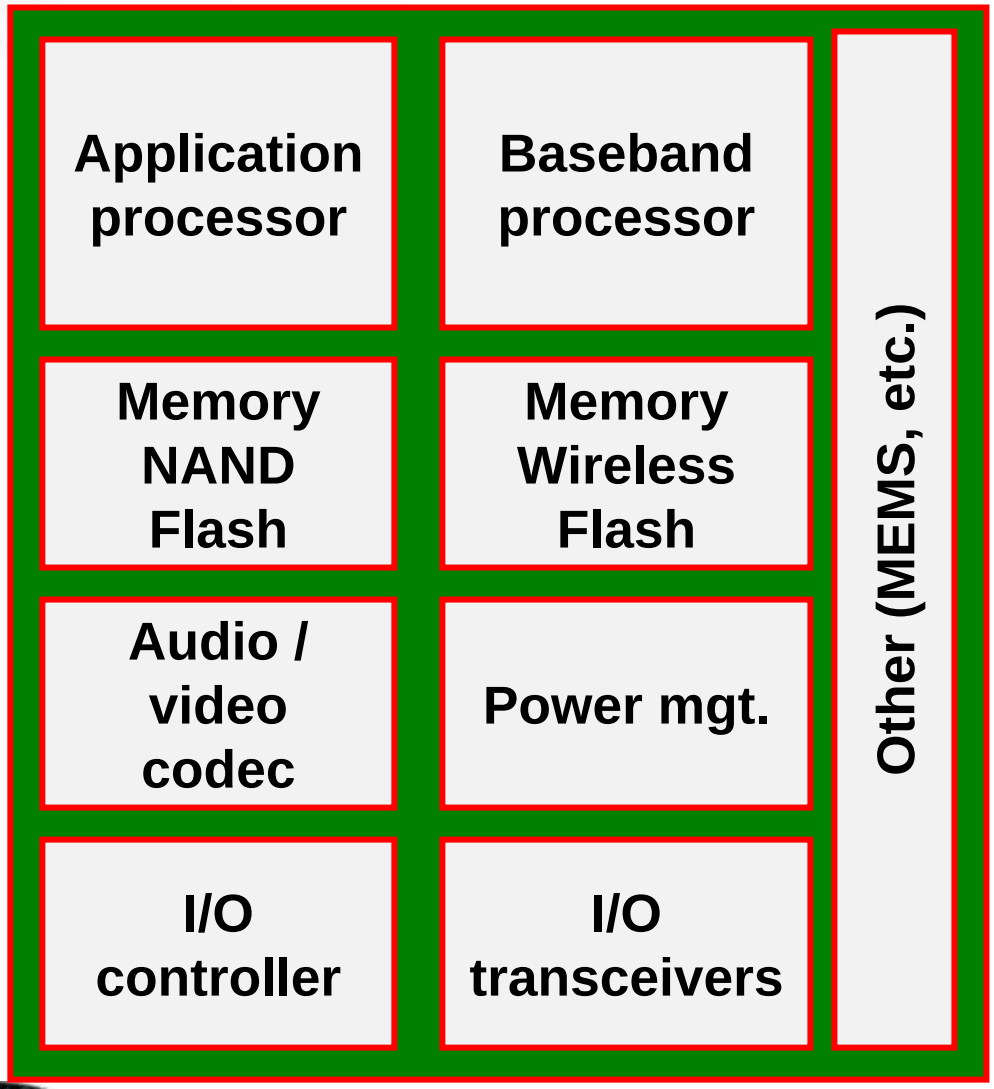
Consumer stationary (SiP)



System Drivers and iNEMI (2009)

Proposal to iNEMI: develop Portable *System* Architecture Template

New Chair with domain expertise – expect deeper commitment



→ **Processing**
POWER

→ **Memory / Flash**
COST

→ **Analog / I/O**
NOISE SENSITIVITY

Design & Key ITRS Cross-TWG Initiatives

- **With Interconnect (A&P): 3D / TSV roadmapping survey**
- **With PIDS, FEP, IRC: Power-driven roadmap; modeling and requirements support for CV/I → RO-based transistor metric**
- **With CSTNSG: Updated frequency, SRAM area, active area (yield) projects**
- **With More Than Moore Study Group: Definition of SIP-scenario System Driver roadmaps to complement existing SOC-scenario Driver roadmaps**

Summary

Design Actions **2010**

1. **Continue expanding importance of SW and system level**
2. **Quantify design tech. impact on variability / "sigma" control**
3. **Update "design cost control through innovation" chart**
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