

Interconnect Working Group



2009 Revision
16 December 2009
Hsinchu, Taiwan



ITWG Regional Chairs

Europe

Hans-Joachim Barth

Alexis Farcy

Korea

Hyeon-Deok Lee

Sibum Kim

Japan

Hideki Shibata

Masayuki Hiroi

Taiwan

Douglas CH Yu

US

Christopher Case

Partial List of Contributors

- Shuhei Amakawa
- Nobuo Aoi
- Sitaram Arkalgud
- Lucile Arnaud
- Koji Ban
- Hans-Joachim Barth
- Eric Beyne
- Christopher Case
- Chung-Liang Chang
- Hsien-Wei Chen
- Jinn-P. Chu
- Alexis Farcy
- Paul Feeney
- Masayuki Hiroi
- Harold Hosack
- Masayoshi Imai
- Raymond Jao
- Shin-Puu Jeng
- Sibum Kim
- Mauro Kobrinsky
- Nohjung Kwak
- Hyeon Deok Lee
- Scott List
- Anderson Liu
- Didier Louis
- JD Luttmmer
- Toshiro Maekawa
- Mike Mills
- Azad Naeemi
- NS Nagaraj
- Tomoji Nakamura
- Yuichi Nakao
- Eiichi Nishimura
- Akira Ouchi
- Peter Ramm
- Rick Reidy
- Scott Pozder
- Philip Pieters
- Andy Rudack
- Gunther Schindler
- Larry Smith
- Mark Scannell
- Hideki Shibata
- Michele Stucchi
- Katsuhiko Tokushige
- Kazuyoshi Ueno
- Weng Hong Teh
- Thomas Toms
- Manabu Tsujimura
- Detlef Weber
- Osamu Yamazaki

1209



2009 Interconnect Topics

- Outline renewal
 - Requirements from device function, and solution by process modules
- Small change in bulk low- κ
 - No change in κ_{eff}
 - Accelerating Air-gap
- Reliability improvement challenge
 - Metal capping for EM resistance booster.
 - Red brick wall decline in J_{max} , new material's introducing
- New 3D TSV roadmap tables
- Emerging interconnect categorization for Cu extension and Cu replacement

2009 Interconnect Chapter Outline

1. Scope

2. Introduction & executive summary

- Product drivers & interconnect roadmap progression
 - Logic
 - Memory
 - More Moore vs. more than Moore
 - Interconnect approaches
 - Current, near term, emerging
- Tables
 - Technology requirements
 - Difficult Challenges

3. Interconnect architectures

- 3D
- Passives

4. Reliability & performance

- Reliability
 - Electromigration, dielectric breakdown, ...
- Performance
 - RC-delay, Power, ...

5. Process modules

- Introduction
- Dielectric
 - Conventional low-k, PMD, airgaps, ...
- Metallization
 - Barrier
 - Nucleation layers
 - Contact, Cu, W, Al, ...
- Etch / strip / clean
- Planarization
- TSV processes

6. Emerging interconnects

- Optical, CNT, graphene, wireless...

Interconnect scope

- **Conductors and dielectrics**
 - Starts at contact
 - Metal 1 through global levels
 - Includes the pre-metal dielectric (PMD)
- **Associated planarization**
- **Necessary etch, strip and cleans**
- **Embedded passives**
- **Global and intermediate TSVs for 3D**
- **Reliability and system and performance issues**
- **“Needs” based replaced by – scaled, equivalently scaled or functional diversity drivers.**

Technology Requirements

Now restated and organized as

- **General requirements**
 - Resistivity
 - Dielectric constant
 - Metal levels
 - Reliability metrics
- **Level specific requirements (M1, intermediate, global)**
 - Geometrical
 - Via size and aspect ratio
 - Barrier/cladding thickness
 - Planarization specs
 - Materials requirements
 - Conductor effective resistivity and scattering effects
 - Electrical characteristics
 - Delay, capacitance, crosstalk, power index

Technology Drivers Expanding

- **Traditional geometric scaling**
 - Cost
 - Necessary to enable transistor scaling
- **Performance**
 - Dielectric constant scaling for delay, and power improvements
- **Reliability**
 - EM
 - Crosstalk
- **Increasing value by adding functionality using CMOS-compatible solutions:**
 - 3D, optical components, sensors
 - Contributing to More than Moore

Difficult challenges (1 of 2)

- *Meeting the requirements of scaled metal/dielectric systems*
 - Managing RC delay and power
 - New dielectrics (including air gap)
 - Controlling conductivity (liners and scattering)
 - Filling small features
 - Barriers and nucleation layer
 - Conductor deposition
 - Reliability
 - Electrical and thermo-mechanical
- Engineering a manufacturable interconnect stack compatible with new materials and processes
 - Defects
 - Metrology
 - Variability

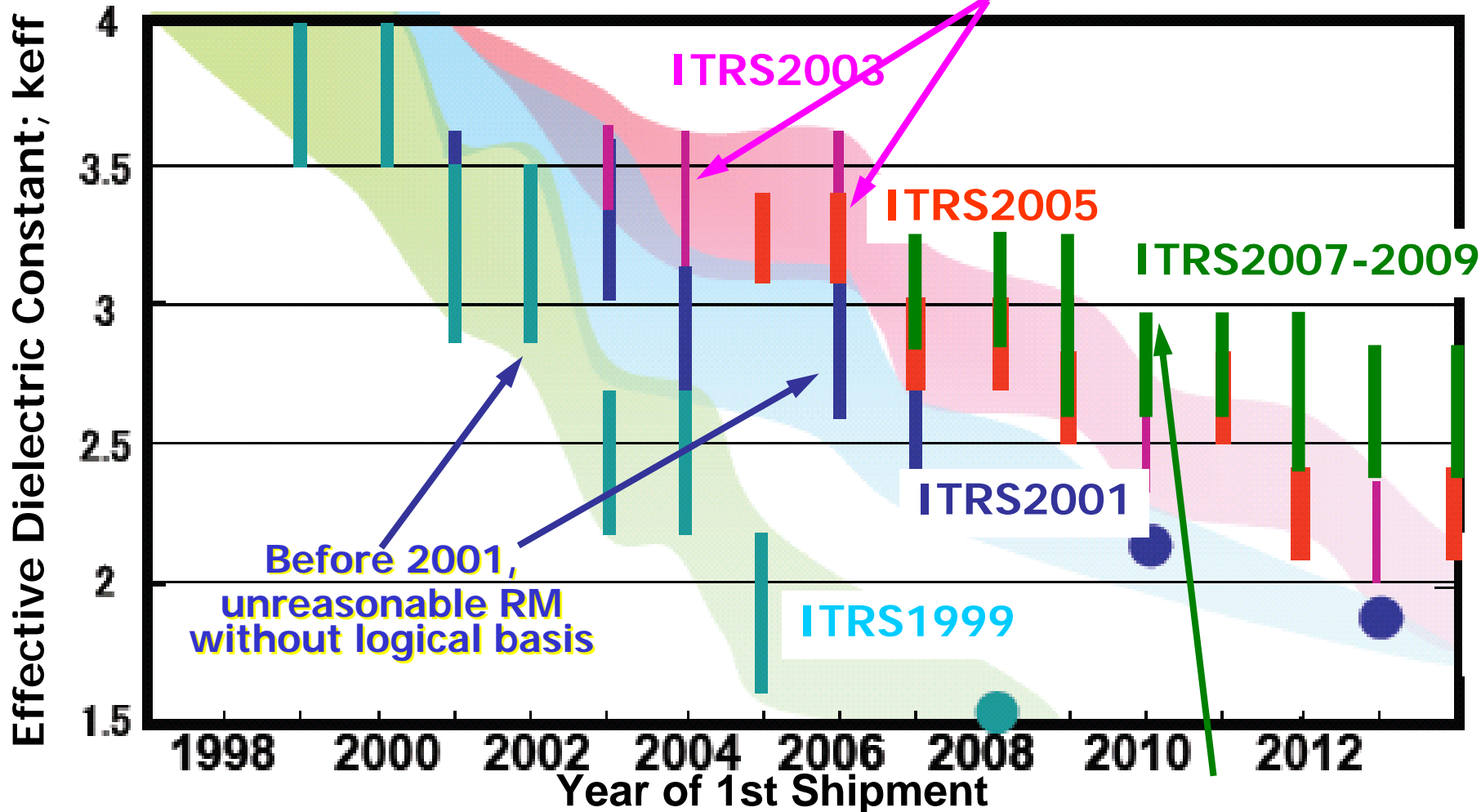


Difficult challenges (2 of 2)

- *Meeting the requirements with equivalent scaling*
 - Interconnect design and architecture (includes multi-core benefits)
 - Alternative metal/dielectric assemblies
 - 3D with TSV
 - Interconnects beyond metal/dielectrics
 - 3D
 - Optical wiring
 - CNT/Graphene
 - Reliability
 - Electrical and thermo-mechanical
- Engineering a CMOS-compatible manufacturable interconnect system
 - Non-traditional materials (for optical, CNT etc.)
 - Unique metrology (alignment, chirality measurements, turning radius etc)

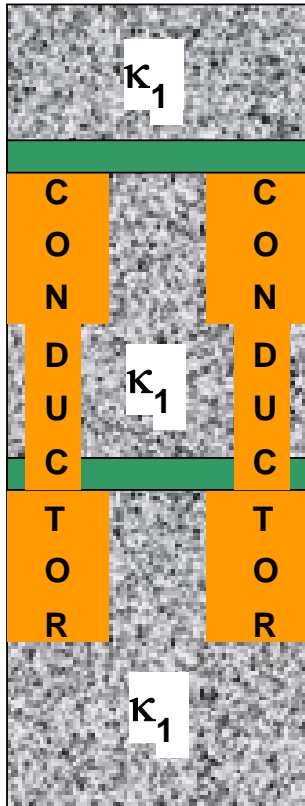
Historical Transition of ITRS Low- κ Roadmap

Since 2003, based on wiring capacitance calculation of three kinds of dielectric structures and validated against publications

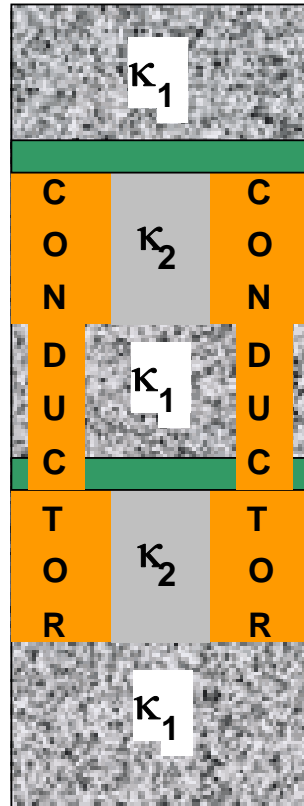


2009 decreased max bulk κ by 0.1 - no significant change on k_{eff} in 2009

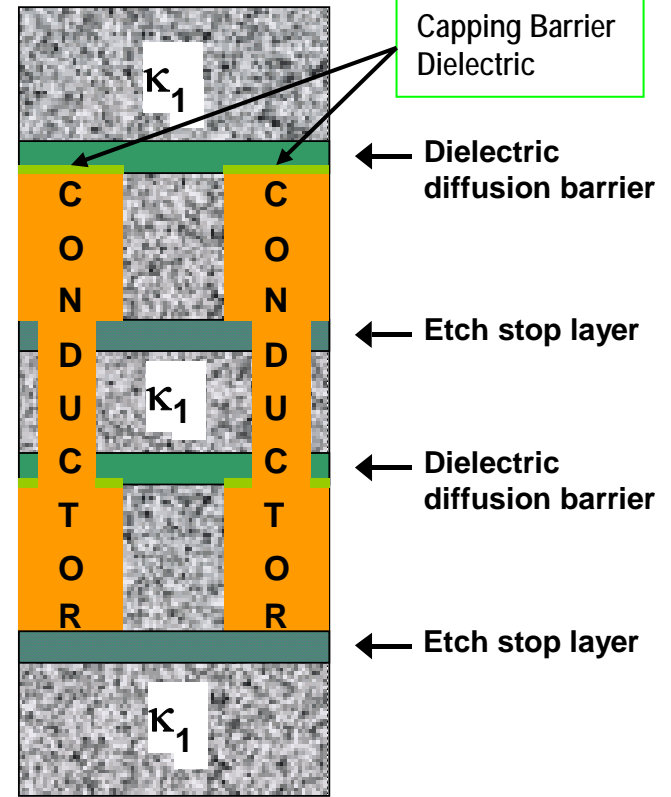
Integration Schemes



Homogeneous ILD
without trench etch stop



Embedded low κ ILD
($\kappa_1 > \kappa_2$)



Homogeneous ILD
with trench etch stop

Capping Barrier
Dielectric


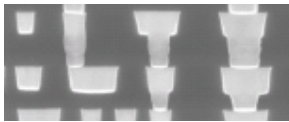
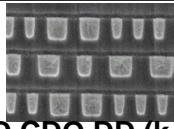
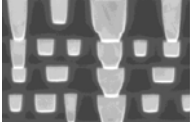
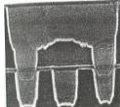





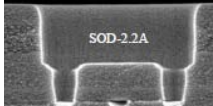

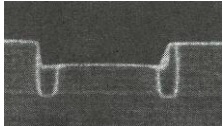

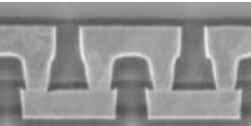

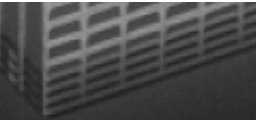
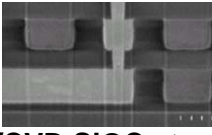




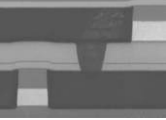
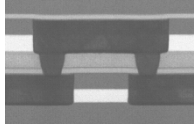
Dielectric
diffusion barrier

Etch stop layer

Dielectric
diffusion barrier

Etch stop layer

Low- κ Trend from Conference Papers (2003-09 IITC, IEDM, VLSI, AMC)

Company	90 nm	65 nm	45 nm	32nm
A	 CVD CDO DD ($k=2.9$)	 CVD CDO DD ($k=2.9$)	 CVD CDO DD ($k=2.7$) with thin SiCN	 CVD CDO DD ($k=2.5$)
B	 CVD SiOC DD ($k=3.0$)	 CVD SiOC DD ($k=2.75$)	 CVD SiOC DD ($k=2.45$)	 CVD SiOC DD ($k=2.45$)
C	 CVD SiOC DD ($k=3.0$)	 CVD SiOC DD ($k=2.7$)	 CVD SiOC DD ($k=2.55$)	 CVD SiOC(LK-1) DD ($k=2.5$)
D	 CVD SiOC DD ($k=2.9$)	 CVD SiOC stack DD ($k=2.6/3.0$)	 CVD SiOC DD ($k=2.65$)	 CVD SiOC DD ($k=2.65$)
E	 CVD SiOC DD ($k=2.9$)	 NCS/CVD SiOC stack DD ($k=2.25/2.9$)	 NCS/NCS stack DD ($k=2.25/2.25$)	 Full-NCS DD with EB-Cure ($k=2.25$)
F	 CVD SiOC DD ($k=2.9$)	 PAr/SiOC hybrid DD ($k=2.6/2.5$)	 P-PAr/p-SiOC hybrid DD ($k=2.3/2.3$)	 ULK-PAr/SiOC hybrid DD ($k=2.0/2.0$)

Little change from 2008; large variation (~ 0.5) of κ below 45 nm

Actual Low- κ Trend for Manufacturing

Company	90 nm	65 nm	45 (40) nm	32 (28)nm
A	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=2.7$)	CVD SiOC DD ($k=2.5$)
B	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=2.5$)	CVD SiOC DD ($k=2.3$)
C	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=2.8$)	CVD SiOC DD ($k=2.4$)
D	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=2.75$)	CVD SiOC DD ($k=2.4$)
E	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=2.75$)	CVD SiOC DD ($k=2.4$)
F	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=3.0$)	CVD SiOC DD ($k=2.8$)	CVD SiOC DD ($k=2.3$)

- One generation delay from Conference Papers.
- Narrower variation of bulk κ range to 0.2 for 32 (28) nm

2009 Low-k Roadmap Update

45 (40) nm

32 (28) nm

22 (20) nm

Year of Production		2009	2010	2011	2012	2013	2014	2015
Was	Interlevel metal insulator – effective dielectric constant (κ)	2.6-2.9	2.6-2.9	2.6-2.9	2.4-2.8	2.4-2.8	2.4-2.8	2.1-2.5
Is	Interlevel metal insulator – effective dielectric constant (κ)	2.9-3.3	2.6-2.9	2.6-2.9	2.6-2.9	2.4-2.8	2.4-2.8	2.4-2.8
Was	Interlevel metal insulator – bulk dielectric constant (κ)	2.3-2.6	2.3-2.6	2.3-2.6	2.1-2.4	2.1-2.4	2.1-2.4	1.9-2.2
Is	Interlevel metal insulator – bulk dielectric constant (κ)	2.5-2.8	2.3-2.5	2.3-2.5	2.3-2.5	2.1-2.3	2.1-2.3	2.1-2.3
Was	Copper diffusion barrier and etch stop – bulk dielectric constant (κ)	3.5-4.0	3.5-4.0	3.5-4.0	3.0-3.5	3.0-3.5	3.0-3.5	2.6-3.0
Is	Copper diffusion barrier and etch stop – bulk dielectric constant (κ)	4.0-4.5	3.5-4.0	3.5-4.0	3.5-4.0	3.0-3.5	3.0-3.5	3.0-3.5

Change tech.node timing from 2009 to 2010 for 32 (28) nm, and decrease maximum bulk κ value by 0.1 from 2.6 to 2.5 in 2010-2012 corresponding to 32 (28) nm actual introduction in manufacturing of low- κ material, 2.3-2.6→2.3-2.5 @2010-2012.

16 (15) nm

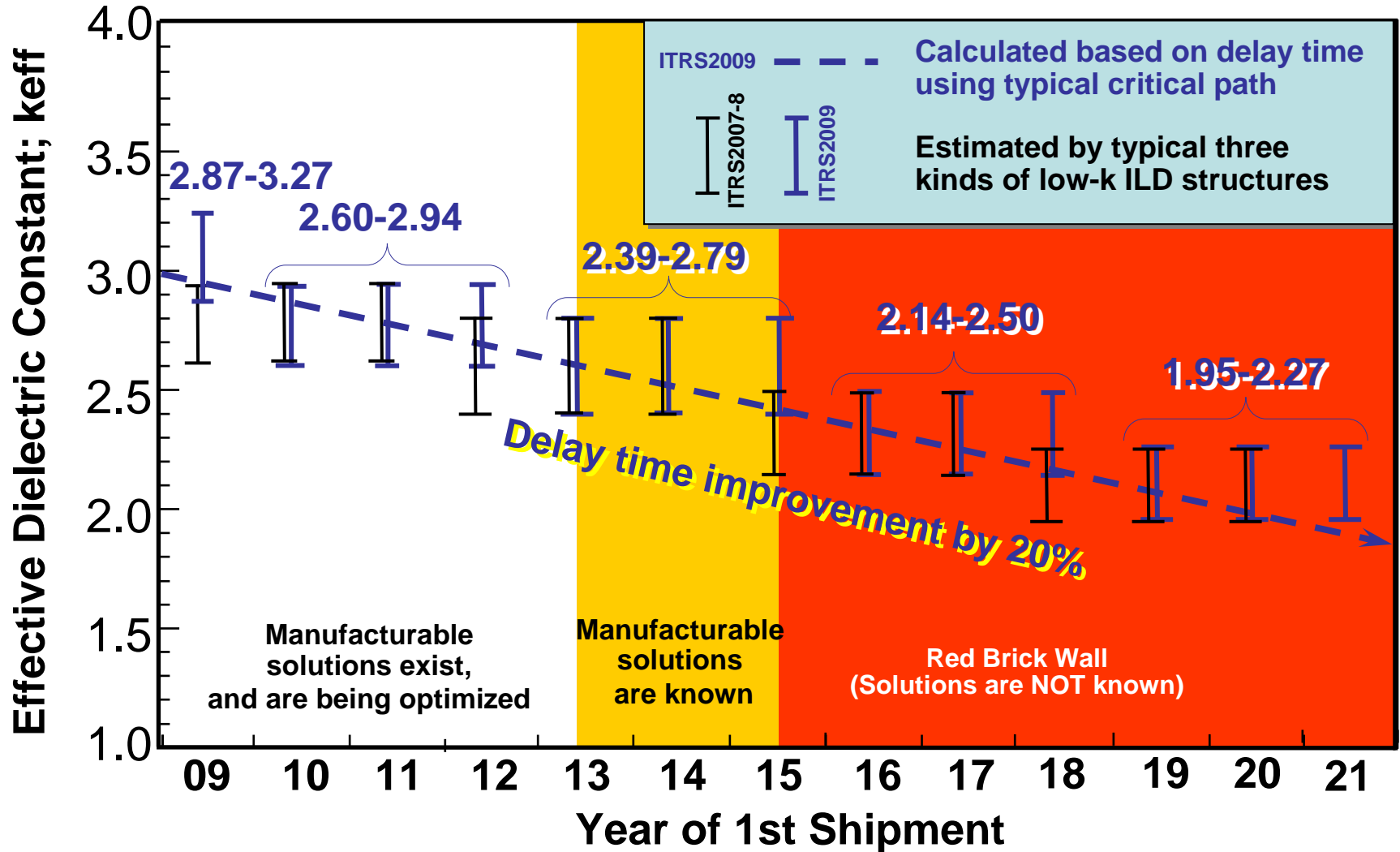
	2016	2017	2018	2019	2020	2021	2022	2023	2024
Was	2.1-2.5	2.1-2.5	2.0-2.3	2.0-2.3	2.0-2.3	1.7-2.0	1.7-2.0		
Is	2.1-2.5	2.1-2.5	2.1-2.5	2.0-2.3	2.0-2.3	2.0-2.3	1.7-2.0	1.7-2.0	1.7-2.0
Was	1.9-2.2	1.9-2.2	1.7-2.0	1.7-2.0	1.7-2.0	1.5-1.8	1.5-1.8		
Is	1.9-2.1	1.9-2.1	1.9-2.1	1.7-1.9	1.7-1.9	1.7-1.9	1.5-1.7	1.5-1.7	1.5-1.7
Was	2.6-3.0	2.6-3.0	2.4-2.6	2.4-2.6	2.4-2.6	2.1-2.4	2.1-2.4		
Is	2.6-3.0	2.6-3.0	2.6-3.0	2.4-2.6	2.4-2.6	2.4-2.6	2.2-2.4	2.2-2.4	2.2-2.4

Decrease maximum bulk κ value by 0.1 beyond 2013.

2.1-2.4→2.1-2.3 @'13-'15
 1.9-2.2→1.9-2.1 @'16-'18
 1.7-2.0→1.7-1.9 @'19-'21
 1.5-1.8→1.5-1.7 @'22-'24
 XX-XX→1.3-1.5 @'25-'27



2009 Low-k Roadmap Update (κ_{eff})



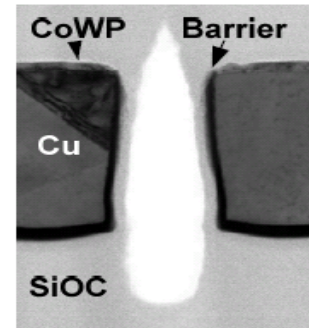
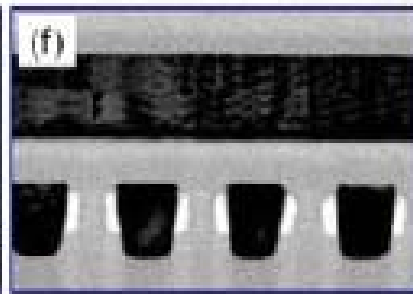
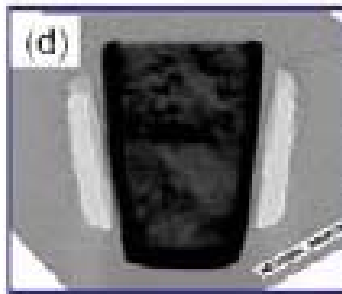
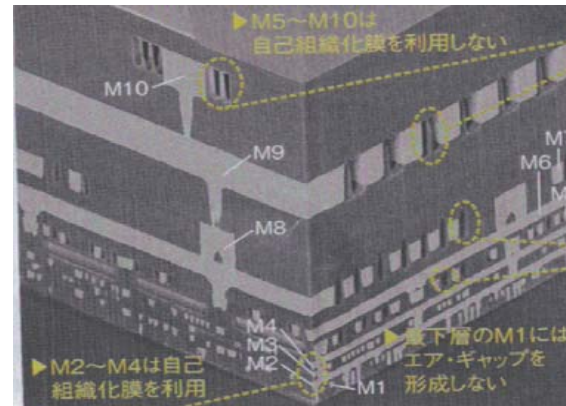
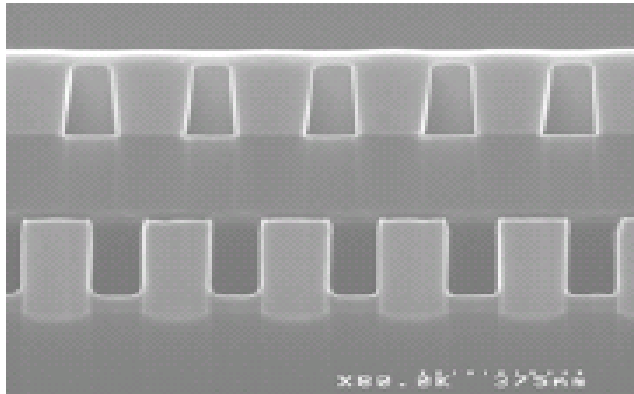
Revised transition timing and decreased maximum bulk k range, but almost the same κ_{eff} range as ITRS2007



Air Gap

Approaches

- Creation of air gaps with non-conformal deposition
- Removal of sacrificial materials after multi-level interconnects



Pictures (top left, clockwise): NXP, IBM, Panasonic, TSMC

2009 Low k or nothing?

<i>Year of Production</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>
<i>MPU/ASIC Metal 1 1/2 Pitch (nm)(contacted)</i>	<i>54</i>	<i>45</i>	<i>38</i>	<i>32</i>	<i>27</i>	<i>24</i>	<i>21</i>
Interlevel metal insulator – bulk dielectric constant (κ)	2.5-2.8	2.3-2.5	2.3-2.5	2.3-2.5	2.1-2.3	2.1-2.3	2.1-2.3

<i>Year of Production</i>	<i>2016</i>	<i>2017</i>	<i>2018</i>	<i>2019</i>	<i>2020</i>	<i>2021</i>	<i>2022</i>	<i>2023</i>	<i>2024</i>
<i>MPU/ASIC Metal 1 1/2 Pitch (nm)(contacted)</i>	<i>18.9</i>	<i>16.9</i>	<i>15.0</i>	<i>13.4</i>	<i>11.9</i>	<i>10.6</i>	<i>9.5</i>	<i>8.4</i>	<i>7.5</i>
Interlevel metal insulator – bulk dielectric constant (κ)	1.9-2.1	1.9-2.1	1.9-2.1	1.7-1.9	1.7-1.9	1.7-1.9	1.5-1.7	1.5-1.7	1.5-1.7

Air gap architectures will be required for $\kappa_{\text{bulk}} < 2.0$

- No viable materials expected to be available.
- Mechanical requirements easier to achieve with air-gaps.
- End of the material solution and the beginning of an architecture solution.

2009 Barrier/Nucleation/Resistivity

<i>Year of Production</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>
<i>MPU/ASIC Metal 1 1/2 Pitch (nm)(contacted)</i>	<i>54</i>	<i>45</i>	<i>38</i>	<i>32</i>	<i>27</i>	<i>24</i>	<i>21</i>
Barrier cladding thickness Metal 1 (nm)	3.7	3.3	2.9	2.6	2.4	2.1	1.9
Conductor effective resistivity ($\mu\Omega$-cm) Cu Metal 1	3.8	4.08	4.30	4.53	4.83	5.2	5.58

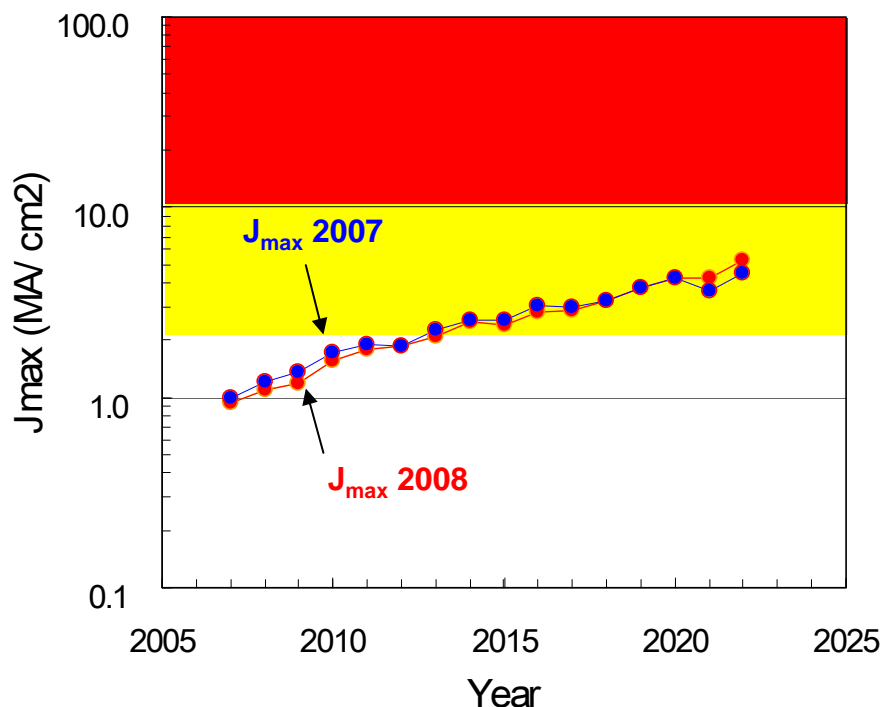
<i>Year of Production</i>	<i>2016</i>	<i>2017</i>	<i>2018</i>	<i>2019</i>	<i>2020</i>	<i>2021</i>	<i>2022</i>	<i>2023</i>	<i>2024</i>
<i>MPU/ASIC Metal 1 1/2 Pitch (nm)(contacted)</i>	<i>18.9</i>	<i>16.9</i>	<i>15.0</i>	<i>13.4</i>	<i>11.9</i>	<i>10.6</i>	<i>9.5</i>	<i>8.4</i>	<i>7.5</i>
Barrier cladding thickness Metal 1 (nm)	1.7	1.5	1.3	1.2	1.1	1.0	0.9	0.8	0.7
Conductor effective resistivity ($\mu\Omega$-cm) Cu Metal 1	6.01	6.33	6.7	7.34	8.19	8.51	9.84	11.30	12.91

- **ALD barrier processes and metal capping layers for Cu are lagging in introduction – key challenge**
- **Resistivity increases due to scattering and impact of liners**
 - **No known practical solutions**

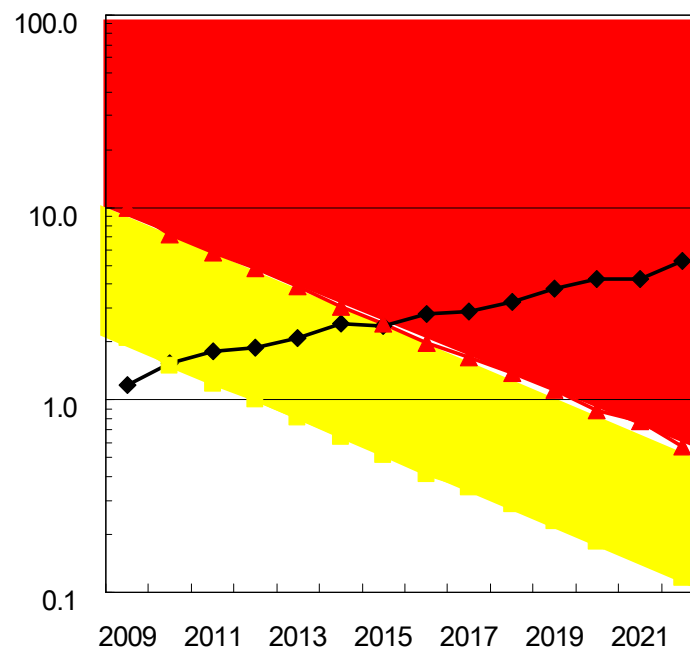
Wire current limit – width dependence

- The color boundaries may actually be width-dependent.
 - Yokogawa & Tsuchiya, 7th International Workshop on Stress-Induced Phenomena in Metallization, pp.124-134, 2004.
 - Hu et al., Microelectronics Reliability, vol.46, pp.213-231, 2006.

2008 Update

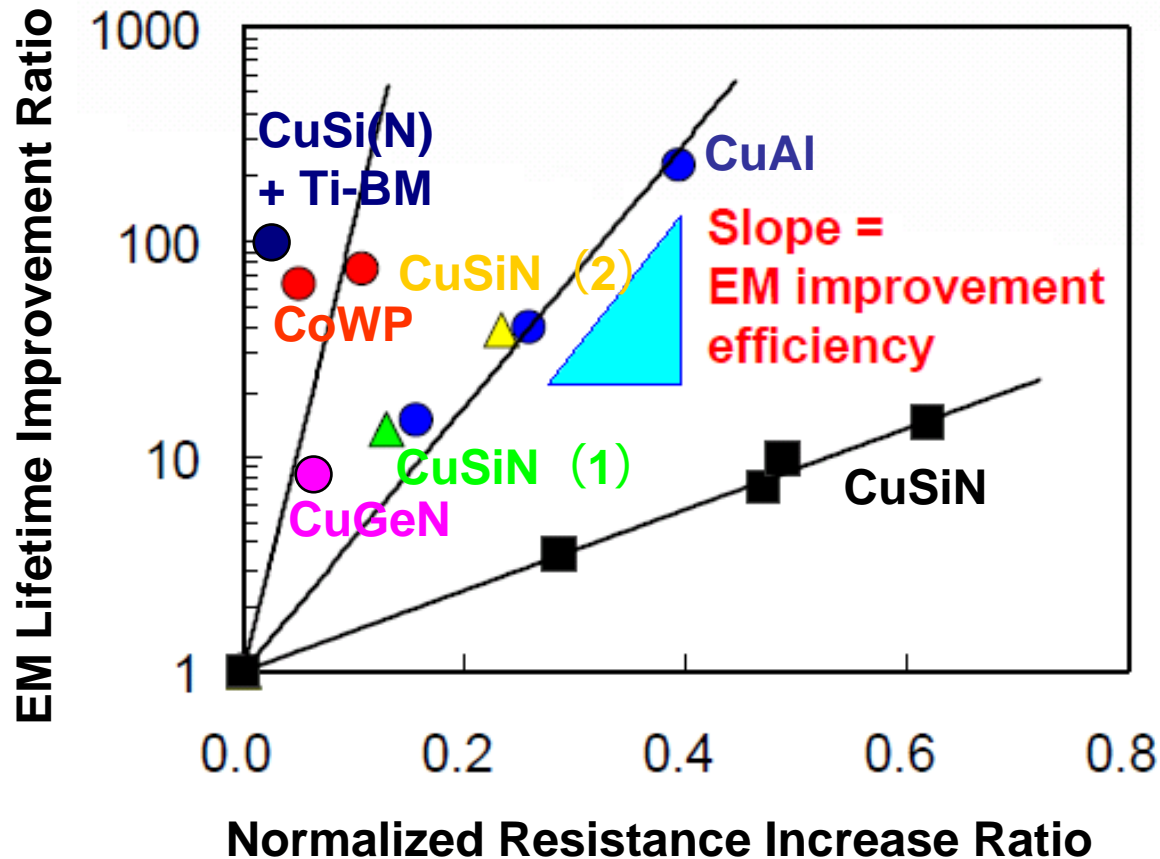


2009 Revision

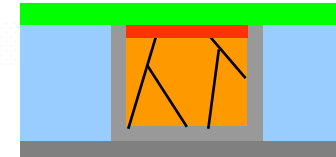


Metal Capping

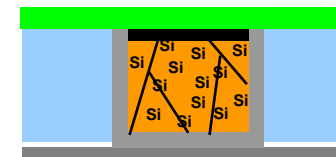
Various lifetime improvement approaches against the resistivity increase



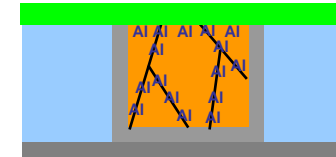
<CoWP-Cap>



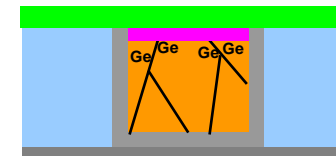
<CuSiN-Cap>



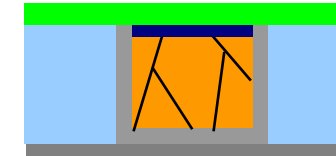
<CuAl-Alloy>



<CuGeN-Cap>



<CuSiN-Cap+Ti>



H. Shibata added published data based on Yokogawa et. Al. IEEE Trans on ED.2008



High Density TSV Roadmap or “enabling terabits/sec at femtojoules”

- The Interconnect perspective - examples:
 - High bandwidth/low energy interfaces between memory and logic
 - Heterogeneous integration with minimal parasitics (analog/digital, mixed substrate materials, *etc.*)
 - “Re-architect” chip by placing macros (functional units) on multiple tiers (wafers) and connect using HD TSVs
- Defined a 3D interconnect hierarchy
 - TSV tables updated to reflect these changes
 - TSV dimensions
 - Minimum contact pitches
 - Overlay accuracy
 - Described process modules

3D Interconnect Levels

Level	Suggested name	Supply chain	Key characteristics
Global	3D-SIC /3D-SOC 3D-Stacked-Integrated-Circuit, 3D-System-on-chip	Wafer Fab	<ul style="list-style-type: none"> Stacking of large circuit blocks (tiles, IP-blocks, memory –banks), similar to an SOC approach but having circuits physically on different layers. Unbuffered I/O drivers (Low C, little or no ESD protection on TSV's). TSV density requirement significantly higher than 3D-WLP : Pitch requirement down to 4-16μm
Intermediate	3D-SIC 3D-Stacked-integrated-circuit	Wafer Fab	<ul style="list-style-type: none"> Stacking of smaller circuit blocks, parts of IP-blocks stacked in vertical dimensions. Mainly wafer-to-wafer stacking. TSV density requirements very high: Pitch requirement down to 1-4 μm

TSV Roadmap - global and intermediate levels

GLOBAL LEVEL, WTW, DTW, or DTD 3D stacking		2009-2012	2012-2015
	Minimum TSV diameter	4-8 μm	2-4 μm
	Minimum TSV pitch	8-16 μm	4-8 μm
	Minimum TSV depth	20-50 μm	20-50 μm
	Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
	Bonding overlay accuracy	1.0-1.5 μm	0.5-1.0 μm
	Minimum contact pitch (thermocompression)	10 μm	5 μm
	Minimum contact pitch (solder or SLID)	20 μm	10 μm
	Number of tiers	2-3	2-4
INTERMEDIATE LEVEL, WTW 3D stacking		2009-2012	2012-2015
	Minimum TSV diameter	1-2 μm	0.8-1.5 μm
	Minimum TSV pitch	2-4 μm	1.6-3 μm
	Minimum TSV depth	6-10 μm	6-10 μm
	Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
	Bonding overlay accuracy	1.0-1.5 μm	0.5-1.0 μm
	Minimum contact pitch	2-3 μm	2-3 μm
	Number of tiers	2-3	8-16 (DRAM)



2009 Emerging Interconnect Changes

OUT:

- **Air gaps → Process Module Section**
 - **Increasing maturity of integrated air gap solutions**
- **3D → Process Module and Architecture Sections**
 - **3D with TSVs nearing production**

IN:

- **Focus on Cu Replacements**
- **Addition of New Section on Native Device Interconnects**
- **Identified need to jointly consider switch and interconnect properties of new switch options**

Emerging Interconnect Summary Table

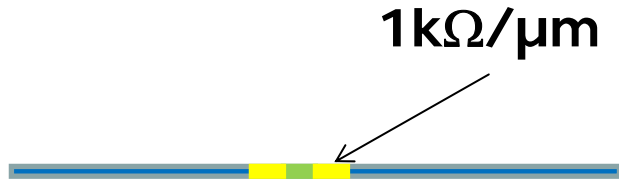
- Interconnect options include Cu Extensions, Cu Replacements and Native Device Interconnects

~ Example of Approaches for Cu Replacements ~

Option	Potential Advantages	Primary Concerns
Other metals (W, Ag, silicides)	Potential lower resistance in fine geometries	Grain boundary scattering, integration issues, reliability
Nanowires	Ballistic conduction in narrow lines	Quantum contact resistance, controlled placement, low density, substrate interactions
Carbon Nanotubes	Ballistic conduction in narrow lines	Quantum contact resistance, controlled placement, low density
Graphene Nanoribbons	Ballistic conduction in narrow films, planar growth	Quantum contact resistance, control of edges, deposition and stacking
Optical (interchip)	High bandwidth, low power and latency, noise immunity	Connection and alignment between die and package, optical /electrical conversions
Optical (intrachip)	Latency and power reduction for long lines, high bandwidth with WDM	Benefits only for long lines, need compact components, integration issues, need WDM
Wireless	Available with current technology, wireless	Very limited bandwidth, intra-die communication difficult, large area and power overhead
Superconductors	Zero resistance interconnect, high Q passives	Cryogenic cooling, frequency dependent resistance, defects, low critical current density

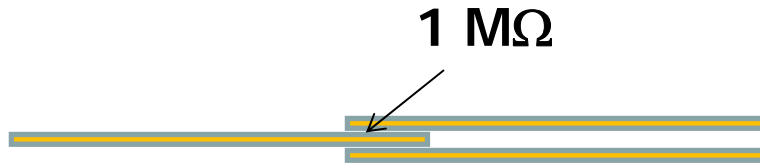
Native Device Interconnects

Nanowires



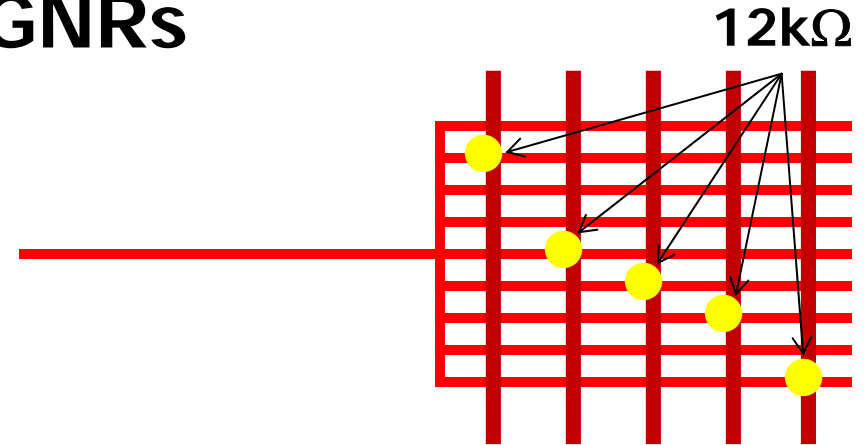
- Doped NWs require silicidation for lengths $> 1\mu\text{m}$

CNTs



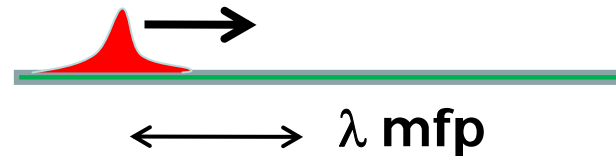
- Multi-fanouts are very difficult
- Serial, multi-input AND gates are easy

GNRs



- Multi-fanouts are easy
- Multi-layer routability incurs quantum resistance

Spin Transport



- Diffusion and spin wave transport are 1000 times slower than electron transport
- Spin relaxation lengths are $\sim 1\mu\text{m}$

Summary

- 3D and air gaps moved out of emerging sections
- Low-k slowdown – small
 - New range for bulk k
 - Air gaps expected to be solution for $k_{\text{bulk}} < 2.0$
- J_{max} current limits are width dependent - a new concern
- Barriers and nucleation layers are a critical challenge
 - ALD barrier processes and metal capping layers for Cu are lagging in introduction – sub 1 nm specs
 - Ru hybrid approaches proliferating
 - Capping metal for reliability improvement
- New Interconnect 3D TSV roadmap tables
- Introduction of a new *Emerging Interconnect Properties*
- First principle consideration of interconnects properties for new switches – CNT, graphene, nanowires etc.