

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) 2006 Update

Hsinchu, Taiwan
The Ambassador Hotel

Hosted
by
the Taiwan Semiconductor Industry Association (TSIA)

PRESS CONFERENCE
12/05/06



2006 UPDATE KEY MESSAGES

*presented by members of
the INTERNATIONAL ROADMAP COMMITTEE (IRC)*

ITRS History/Demographics

Technology Pacing

Lithography

Front End Processes/PIDS

Test

More than Moore

450 mm Wafer Size

Paolo Gargini

Alan Allan

Wolfgang Arden

Hidemi Ishiuchi

Mong Song Liang

Mart Graef

All

2006 Update Executive Overview

The International Technology Roadmap for Semiconductors (ITRS) is the result of a worldwide consensus-building process. This document predicts the main trends in the semiconductor industry spanning across 15 years into the future. The participation of experts from Europe, Japan, Korea, and Taiwan as well as the U.S.A. ensures that the ITRS is a valid source of guidance for the semiconductor industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. These five regions jointly sponsor the ITRS.

The Semiconductor Industry Association (SIA) coordinated the first efforts of producing what was originally *The National Technology Roadmap for Semiconductors (NTRS)*. The semiconductor industry became a global industry in the 1990s, as many semiconductor chip manufacturers established manufacturing or assembly facilities in multiple regions of the world. This realization led to the creation of the *International Technology Roadmap for Semiconductors* in the late 90s. The invitation to cooperate on the ITRS was extended by the SIA at the World Semiconductor Council in April 1998 to Europe, Japan, Korea, and Taiwan. Since then, full revisions of the ITRS were produced in 1999, 2001, 2003 and 2005; ITRS updates were produced in the even-numbered years (2000, 2002, and 2004).

The ITRS process is an ongoing event. The industry is dynamic—continually innovating; introducing new products; and achieving solutions. To keep the ITRS information as current as possible with this dynamic industry environment, during each year following an edition such as the *2005 ITRS*, the roadmap information is reviewed. Data adjustments, corrections, and new information items are agreed to among the ITWG members and by soliciting public feedback during the annual ITRS Summer Conference in San Francisco. For the *2006 ITRS Update* effort, all the ITRS tables were reviewed. If necessary, data and notations were updated to match industry advancements.



2006 Update Executive Overview (continued)

Overall, the *2006 ITRS Update* represents a minor modification to the *2005 ITRS*. The *2006 ITRS Update*, consistent with the *2005 ITRS*, removes the concept of “technology node” as the main pace setter for the IC industry. Users of the 2006 Update easily can determine specific numbers for DRAM metal half-pitch, NAND polysilicon half-pitch, or MPU and ASIC gate length, for example, to characterize the pace of that specific technology. The Overall Roadmap Technology Characteristics Tables and individual ITWG tables use these specific product timings to indicate the drivers for their requirements. For this purpose, the *2006 ITRS Update* addresses an independent measure of the technology pace of DRAM, of MPU, and of Flash products.

Several tables have been corrected or updated, as clearly indicated in blue. It is also rather easy to identify where the changes have occurred as indicated by “**IS**” in the far left column of an updated table. This Overview document contains an Appendix of all tables, figures, or textual changes for the *2006 Update* by chapter.

It is important to remind the reader that it is the purpose of the ITRS documents to provide a reference of requirements, potential solutions, and their timing for the semiconductor industry. This objective has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university, consortia, and government labs.

The ITRS documents have become and remain a truly common reference for the entire semiconductor industry. Indeed, the cooperative efforts of the ITRS participants have fostered cooperation among international consortia, universities, and research institutions around the world. It is hoped that the *2006 ITRS Update* will further contribute to fuel cooperative R&D investments so that the financial burden can be more uniformly shared by the whole industry. It is also hoped that the ITRS will continue to stimulate the fundamental elements that encourage innovation in individual companies.

NTRS* Roadmap Editions

USA Only

1991
Micro Tech 2000
Workshop Report

1992NTRS

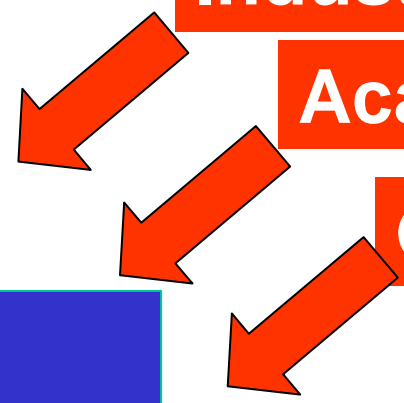
1994NTRS

1997NTRS

Industry

Academia

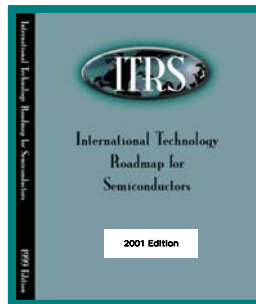
Government



*National Technology Roadmap for Semiconductors

Roadmap Editions

<http://public.itrs.net>



2006ITRS
Update

2005ITRS

2004ITRS
Update

2003ITRS

2002ITRS
Update

2001ITRS

2000ITRS
Update

1999ITRS

1998ITRS
Update

1997NTRS

1994NTRS

1992NTRS

1991
Micro Tech 2000
Workshop Report

Europe

Japan

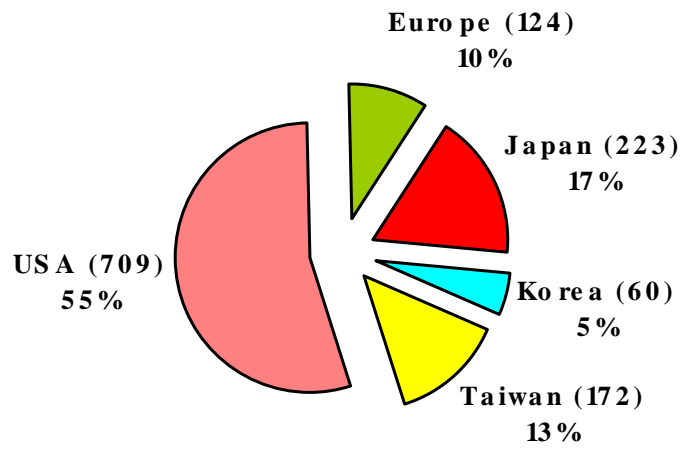
Korea

Taiwan

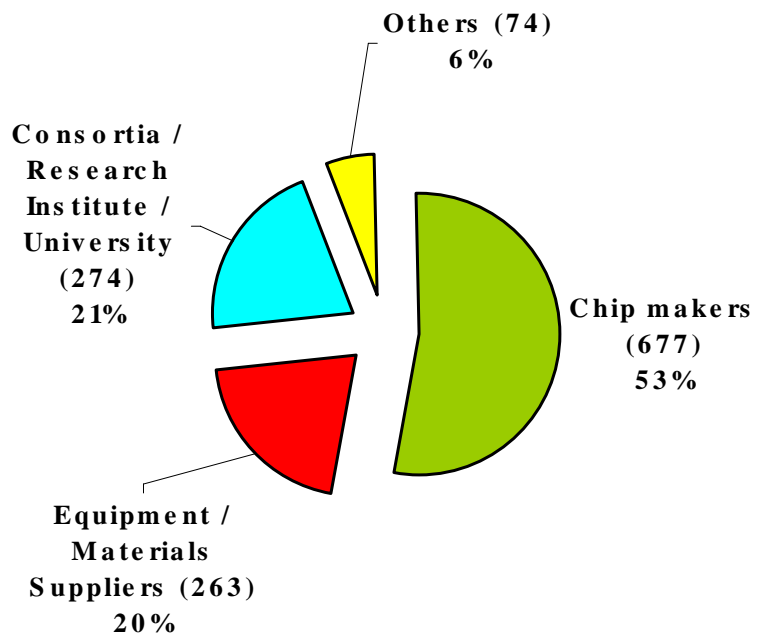
USA

ITRS Demographics

2005 ITRS Members by Region

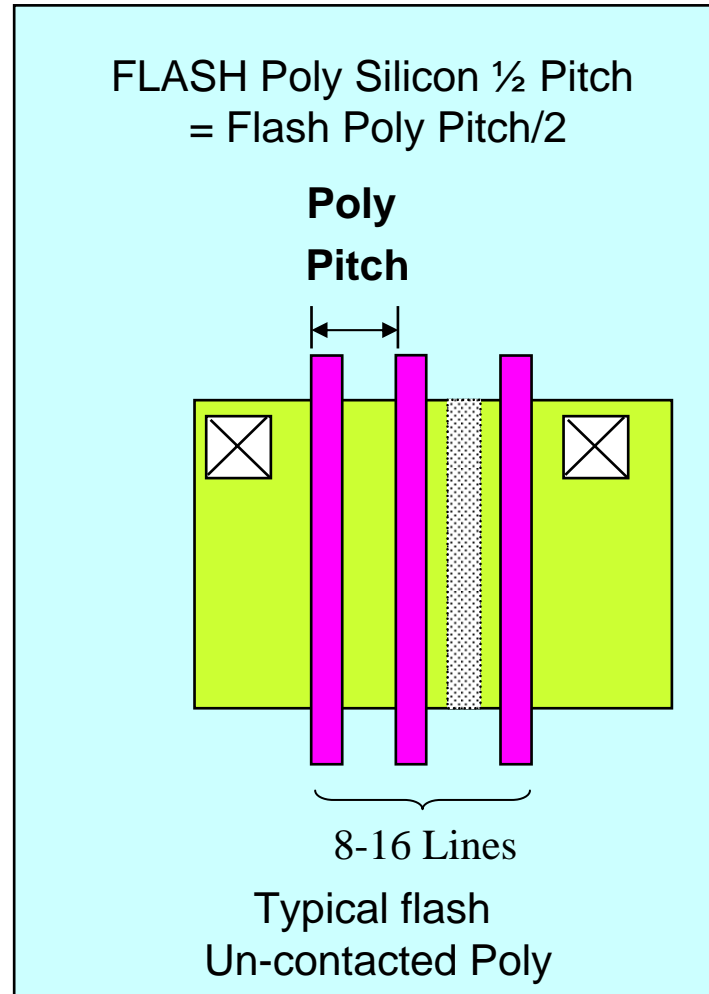
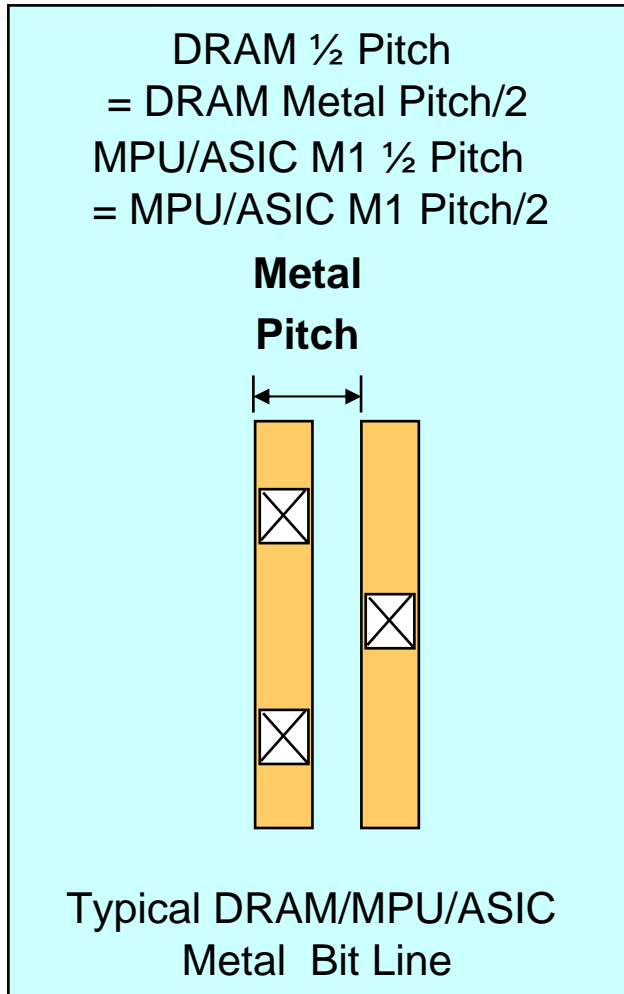


2005 ITRS Members by Affiliation



2005 Definition of the Half Pitch - **unchanged**

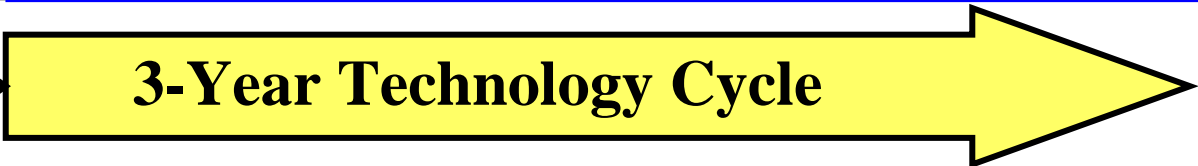
[No single-product “node” designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]



2006 ('05-'20) ITRS Technology Trends DRAM M1 Half-Pitch : 3-year cycle

All unchanged

Year of Production	<u>2000</u> [Actual]	2001	<u>2002</u> [Actual]	2003	<u>2004</u>	2005	2006	<u>2007</u>	2008	2009	<u>2010</u>	<u>2013</u>	<u>2016</u>	<u>2019</u>	2020
Technology - Contacted M1 H-P (nm)	180	151	130	107	90	80	71	65	57	50	45	32	22	16	14



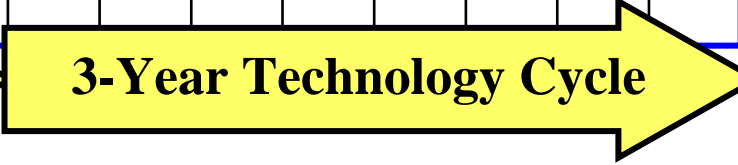
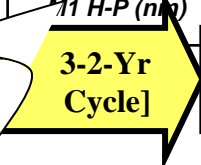
2005 ITRS Flash Poly Half-Pitch Technology: 2.0-year cycle until 1yr ahead of DRAM @65nm/'06

Year of Production	<u>2000</u> [Actual]	2001	<u>2002</u> [Actual]	2003	<u>2004</u>	2005	<u>2006</u>	2008	<u>2009</u>	<u>2012</u>	<u>2015</u>	<u>2018</u>	2019	2020
Technology - Uncontacted Poly H-P (nm)	180	151	130	107	90	76	65	57	50	45	32	22	16	13

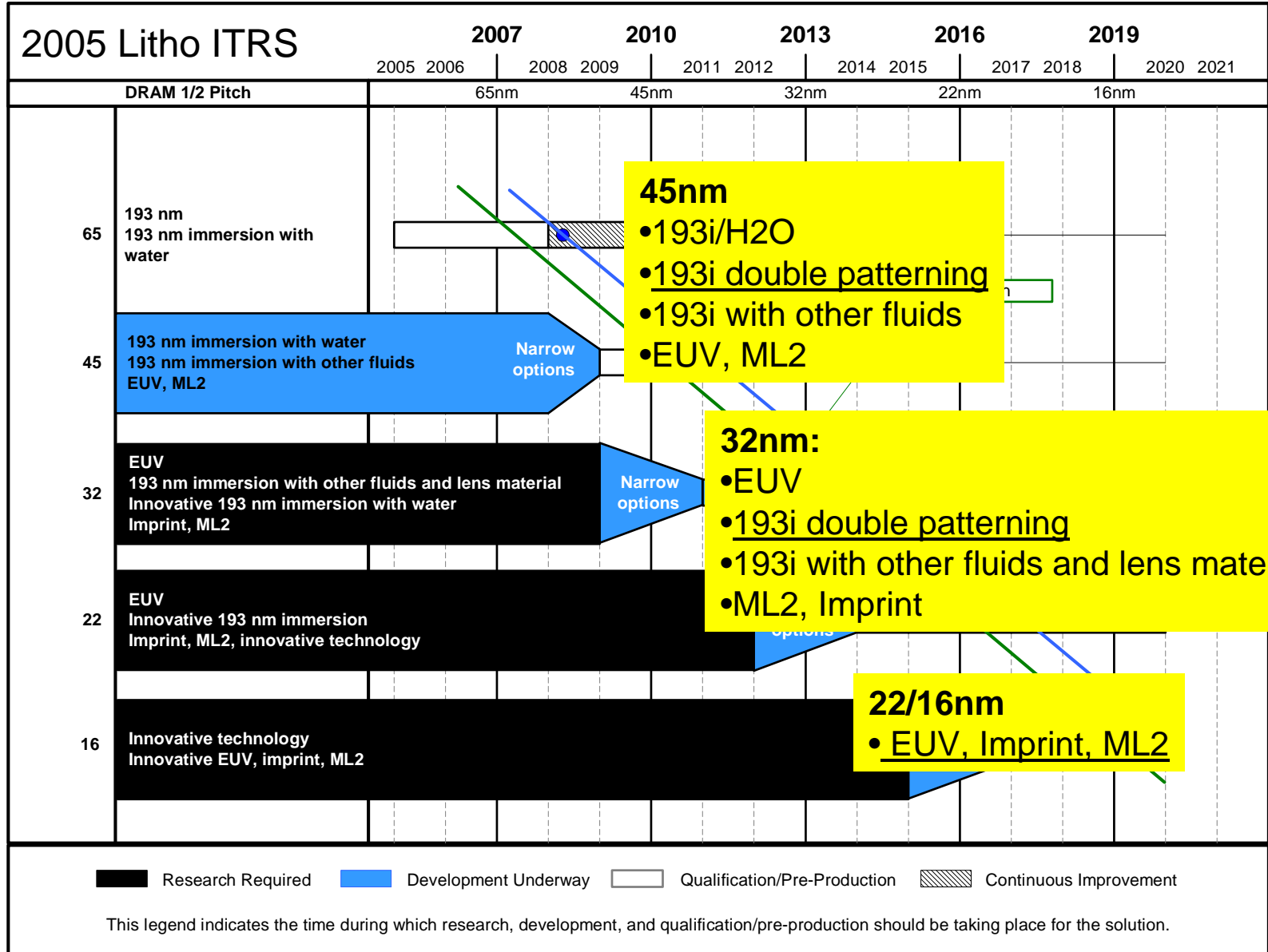


2005 ITRS MPU M1 Half-Pitch Technology: 2.5-year cycle; then equal DRAM @45nm/2010

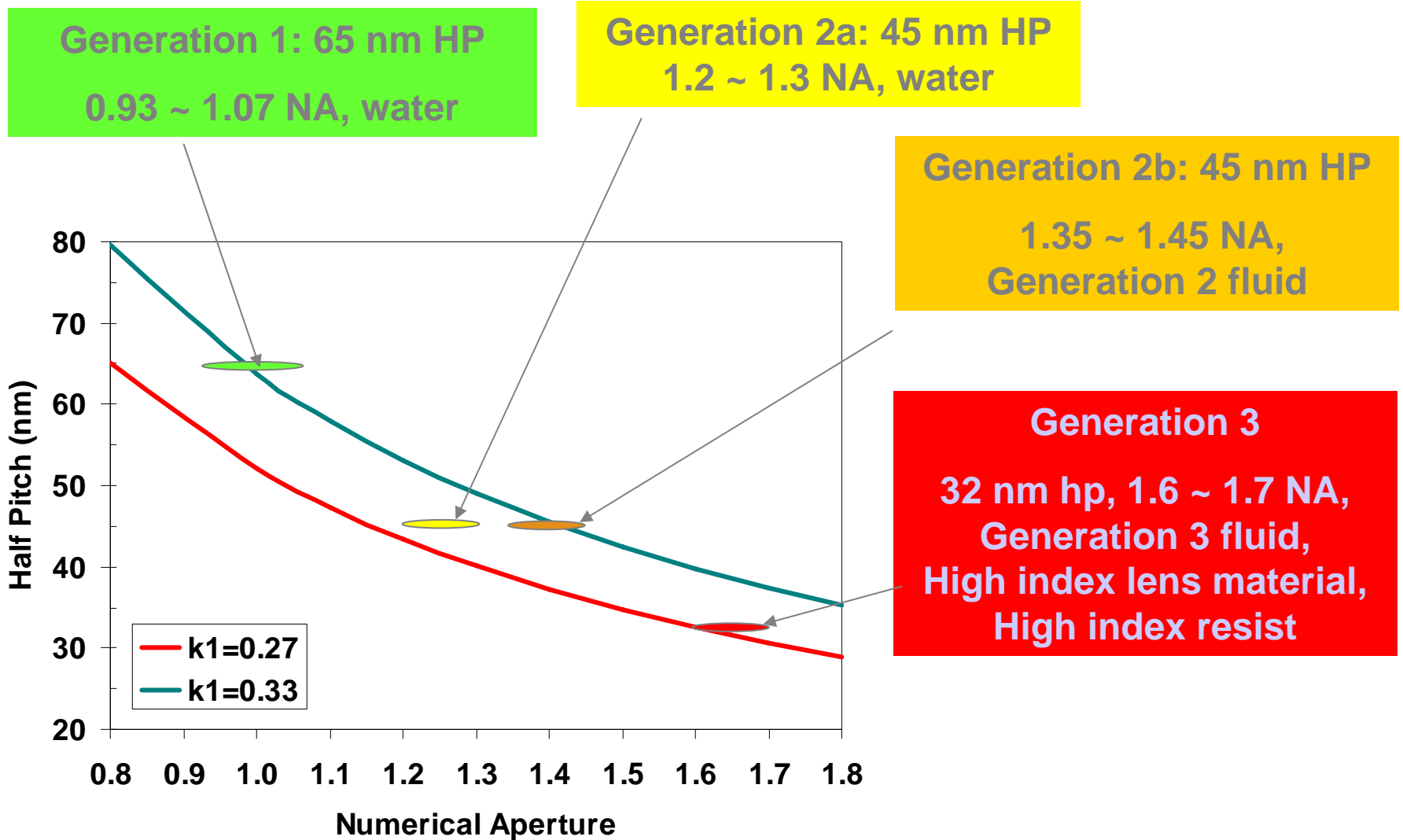
Year of Production	<u>2000</u>	2001	<u>[July'02]</u>	2003	2004	<u>2005</u>	2006	<u>[July'08]</u>	2008	2009	<u>2010</u>	<u>2013</u>	<u>2016</u>	<u>2019</u>	2020
Technology - Contacted M1 H-P (nm)	180	157	136 [130]	119	103	90	78	68 [65]	59	52	45	32	22	16	14



Lithography Potential Solutions 2006 Update



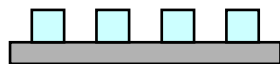
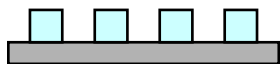
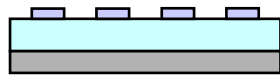
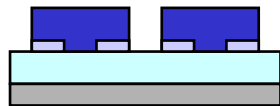
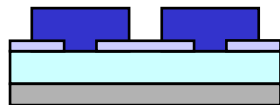
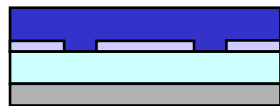
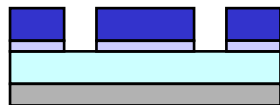
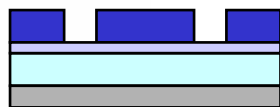
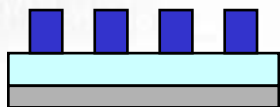
Optical Lithography Immersion Generations



Lithography Double Exposure/Etch (DE/DE)]

Conventional
Single Expose

Double Exp/
Double Etch



- Resist
- Hard Mask
- Under Layer
- Substrate

Expose #1

Hard Mask
Etch

Coat #2

Expose #2

Etch Hard Mask

Etch

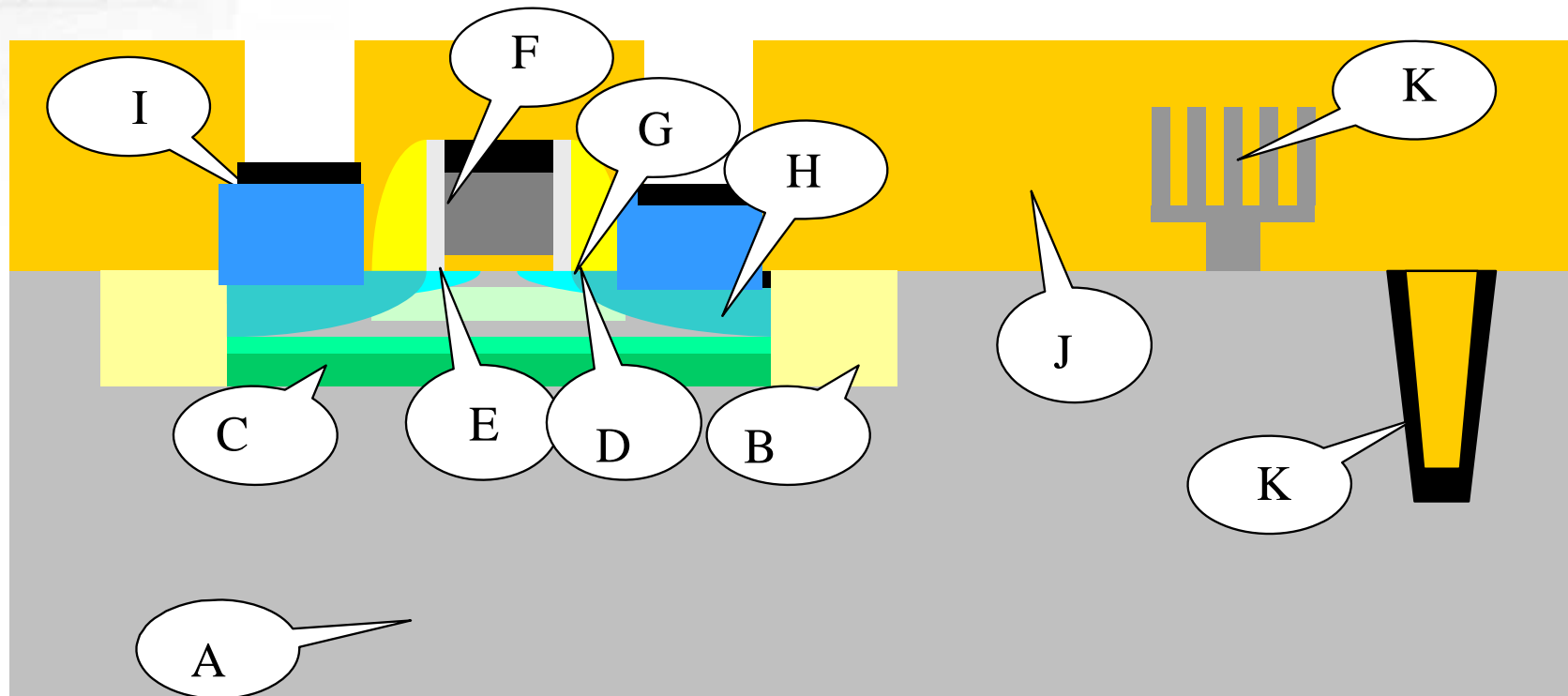
Double Exposure/Etch Challenges

- Resist / Process
- Overlay
- DFM: DE split CAD
- COO

Variety of application
dependent processes

From Andrew Grenville.

Front End Process (FEP)/Process Integration Devices & Structures (PIDS) - Transistor Challenges



A: Starting Material

C: Well Doping

E: Channel Doping and Channel Strain

G: Extension Junction and Halo

I: Elevated Junction and Contacts

K: DRAM Stack/Trench Capacitor & FeRAM Storage

B: Isolation

D: Channel Surface (Preparation)

F: Gate Stack (Including Flash) and Spacer

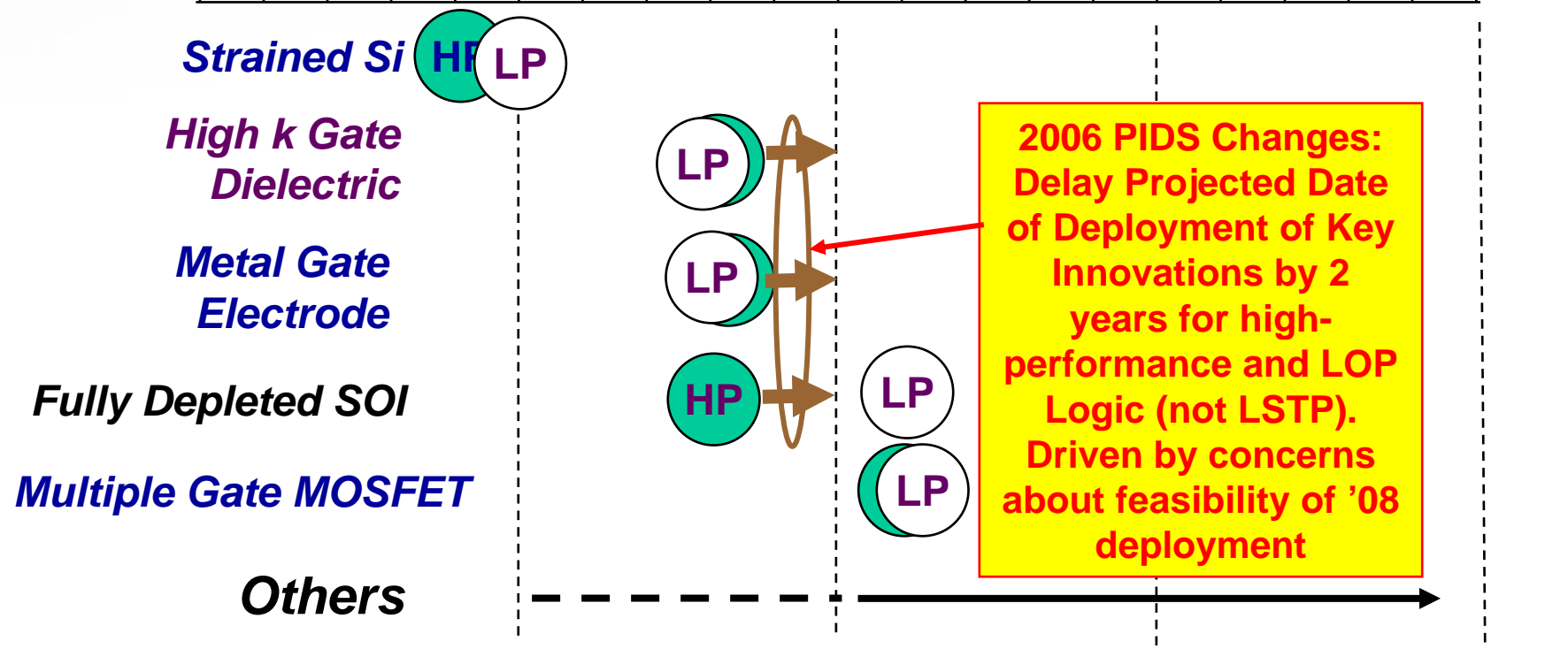
H: Contacting Source/Drain Junction

J: Premetal Dielectric

PIDS - The “CMOS Change Crunch” Multiple, Big Technology Innovations Over Next 5 Years

First Year of “Volume Production”

2000 2005 2010 2015 2020



Driver: (HP) = High Performance Applications (LP) = Low Power Applications

PIDS - Multiple Parallel Paths for High-Performance Logic in ITRS

Year in Production		2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Physical Lgate (High Performance)	nm	32	28	25	22	20	18	16	14	13	11	10	9	8	7	6	5

Planar Bulk CMOS

UTB FD SOI

DG or Multiple-Gate

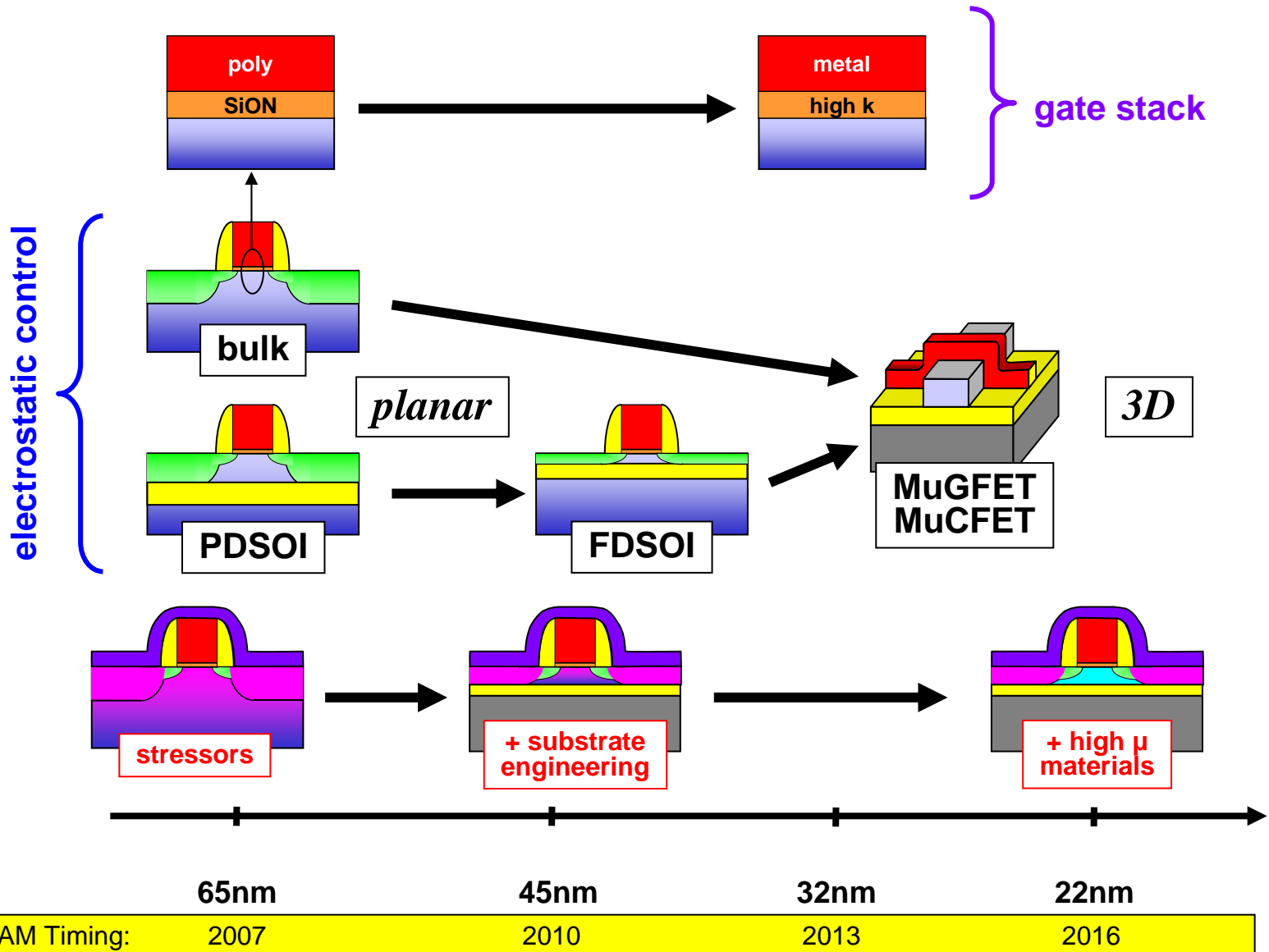
2006 ITRS

Delay

- Multiple parallel paths reflects most likely scenario:
- Some companies will extend planar bulk CMOS as long as possible
 - Others will switch to FDSOI and/or multiple gate earlier
 - Initial deployment of FDSOI is delayed in 2006 ITRS
 - Ultimate MOSFET is multiple gate
 - Similar multiple paths for low-power logic



PIDS/FEP - Simplified Transistor Roadmap



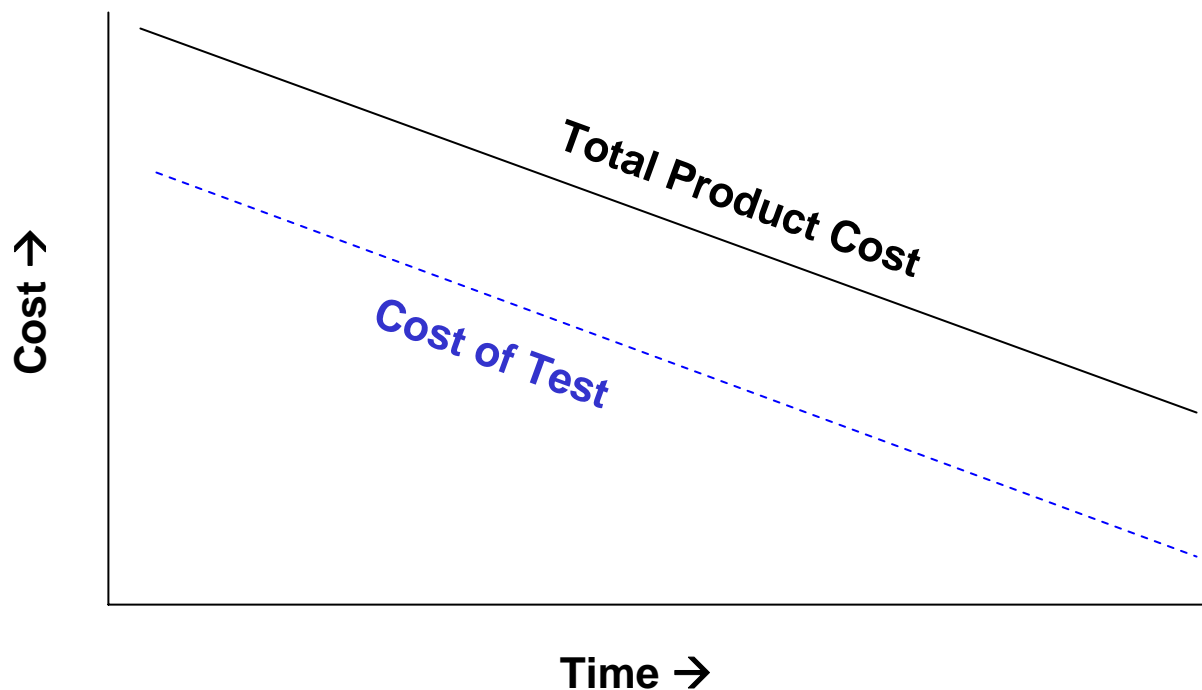
Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

Test TWG - Roadmap Drivers Since 2000

- Adoption of High speed serial I/O
- Widespread use of Known Good Die (KGD)
- Multi-Chip Package, System on Chip & System in Package need to become routine
- NAND!
- Increased integration of Analog/Radio Frequency
- Rapid increase in test parallelism
- Litho roadmap and core voltage reduction driving tightened Signal-to-Noise window

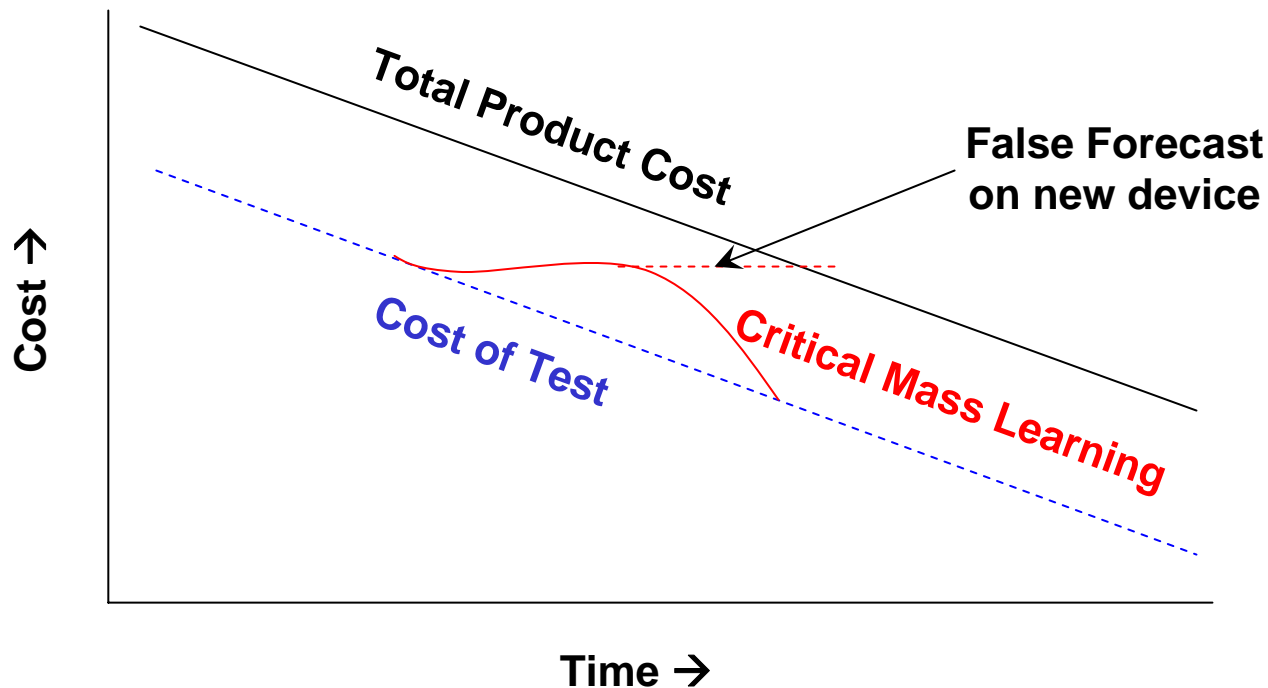
Test TWG - Cost of Test

- Goal: Keep test % of overall product cost flat
 - Test cost per transistor must follow Moore's Law
 - Predictable on well known devices



Test TWG - Cost of Test

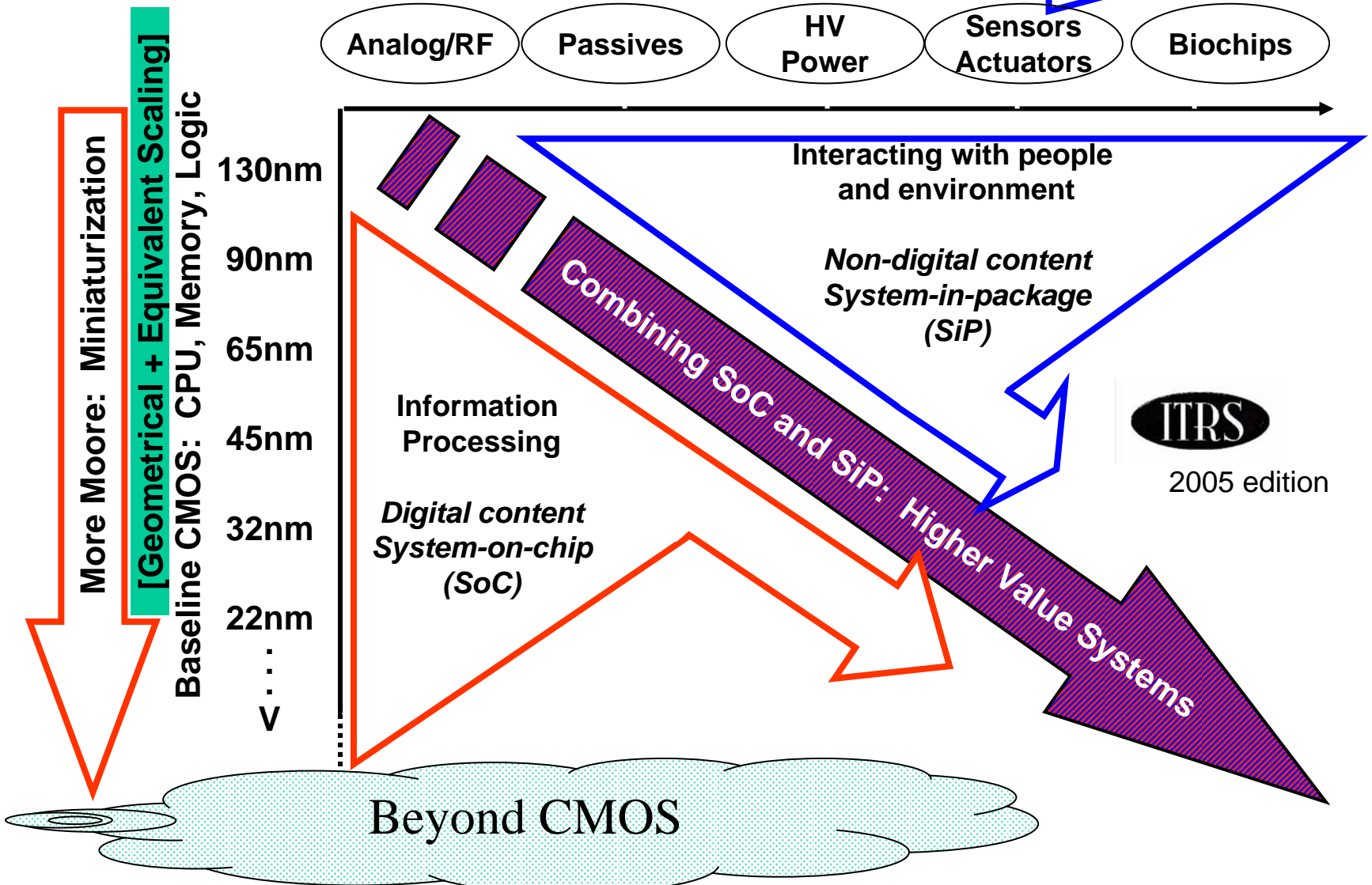
- Test may initially lag learning curve on new devices, integrations or architectures
 - Drove mid 90's forecast of increasing test cost > die cost
 - Critical mass learning necessary to define low cost methods



Pursuing the race for added value for the end customer by combining on-chip ULSI and off-chip integration

More than Moore: Diversification

- Analog/RF
- Passives
- HV Power
- Sensors Actuators
- Biochips



“More Moore” + “More than Moore”

- Past

 - Geometrical Scaling (G) → Moore’s Law

- Future

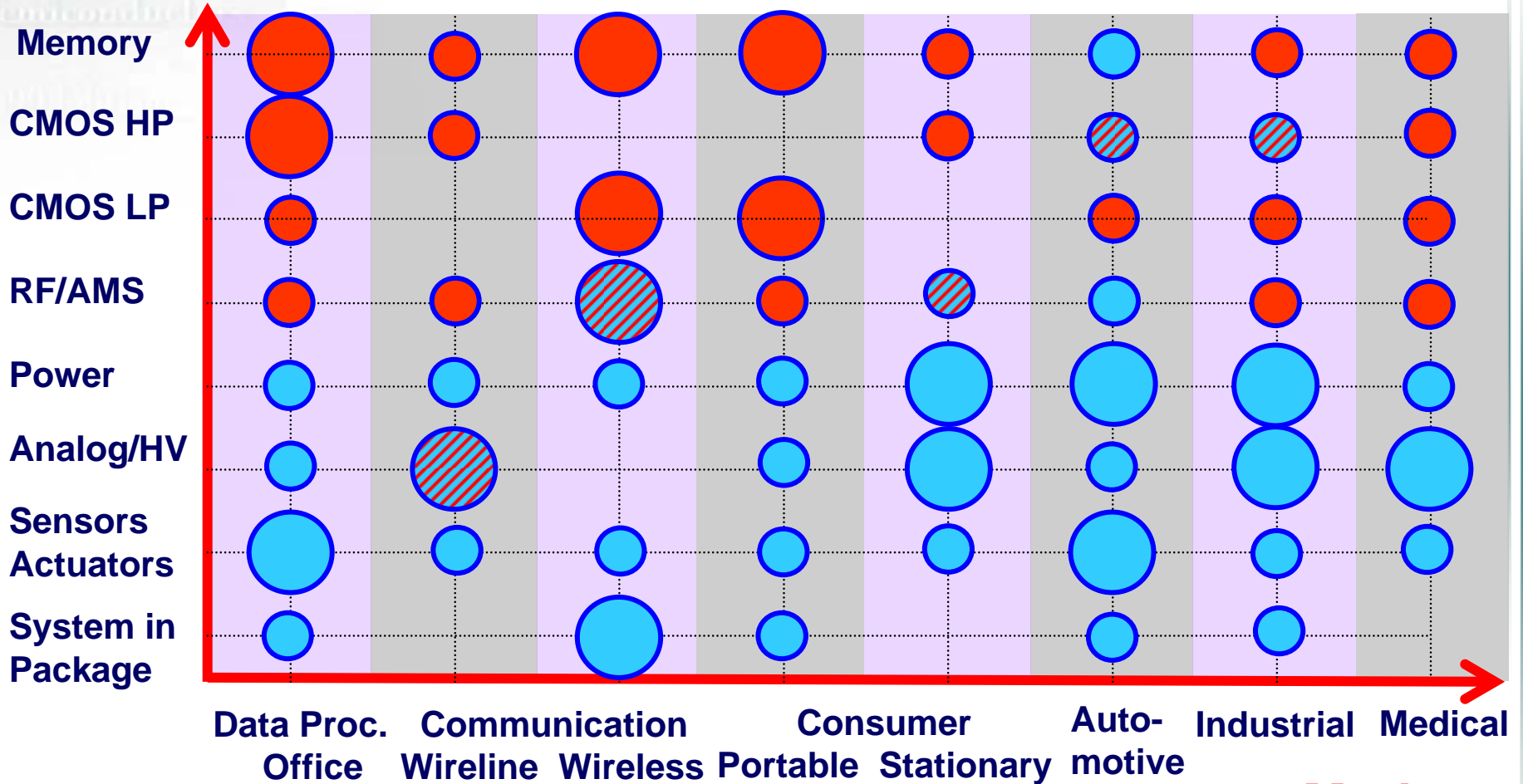
 - Equivalent Scaling (E) _(digital) → “More” Moore

+

Functional Diversification _(non-digital) → More than Moore
(MtM)

Market Drivers for Technology Roadmap

Technologies



Markets

Legend:



More Moore (scaling)



More than Moore (non-scaling)



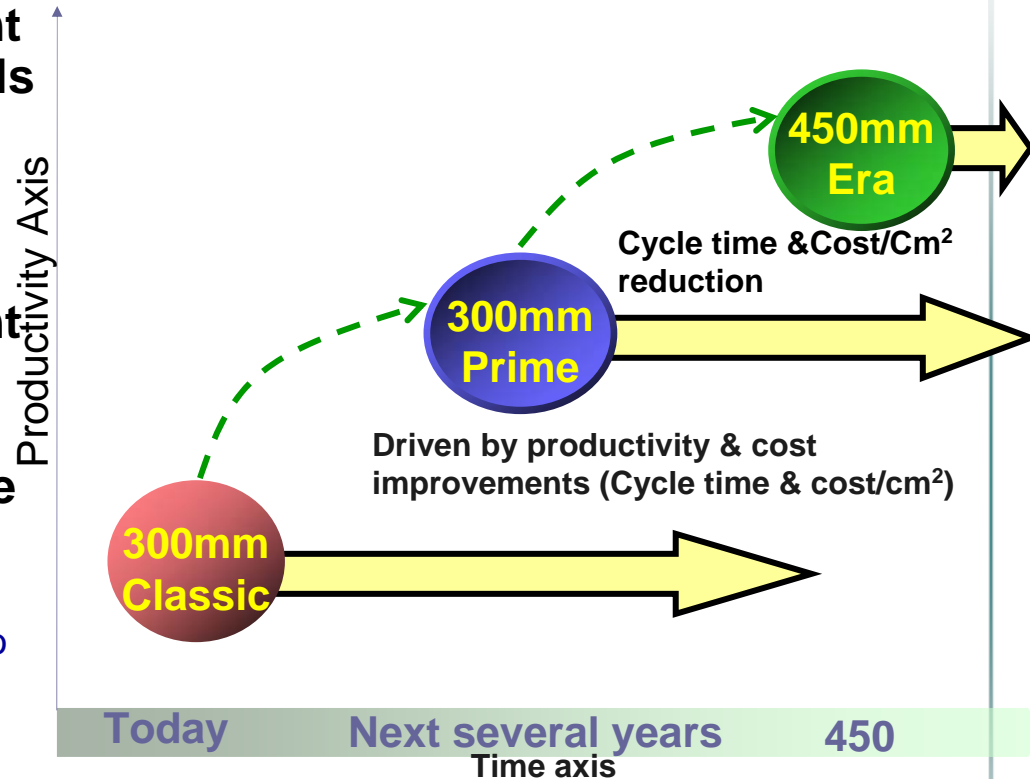
mixed

Bubble size = driver impact



Productivity Improvement Roadmap drivers

- **Comprehend the needs of different IC maker/Foundry business models**
 - These models (including high mix) will influence current 300mm configurations before transition to 450mm occurs
- **300 Prime will close the gaps identified in current 300 equipment**
 - New capabilities extendible to 450
- **450mm transition can be a simplified scale-up from 300 Prime**
 - Compared to 200mm → 300mm transition
 - Extending 300mm capability to 450mm
 - Minimizing the number of configurations to develop, test and deploy
- **Global participation is very important to define requirements, priorities and due dates**



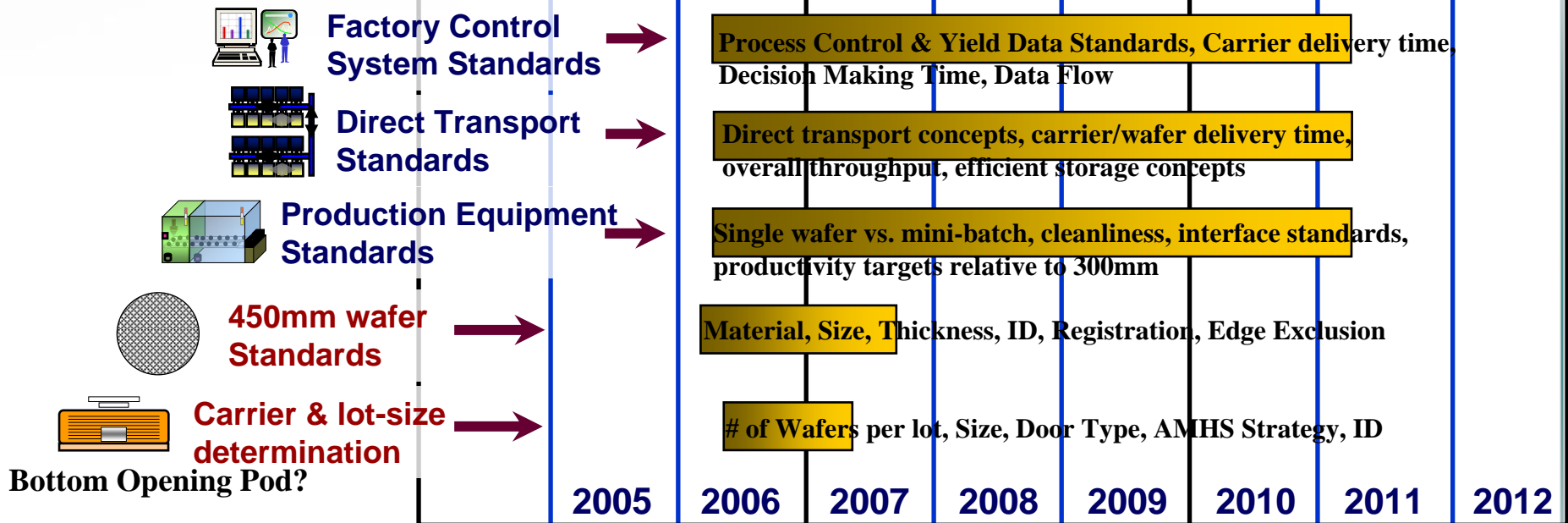
**Key drivers are significant cycle time and cost/cm² reduction
→ Productivity Improvements**



What is needed for 450mm transition



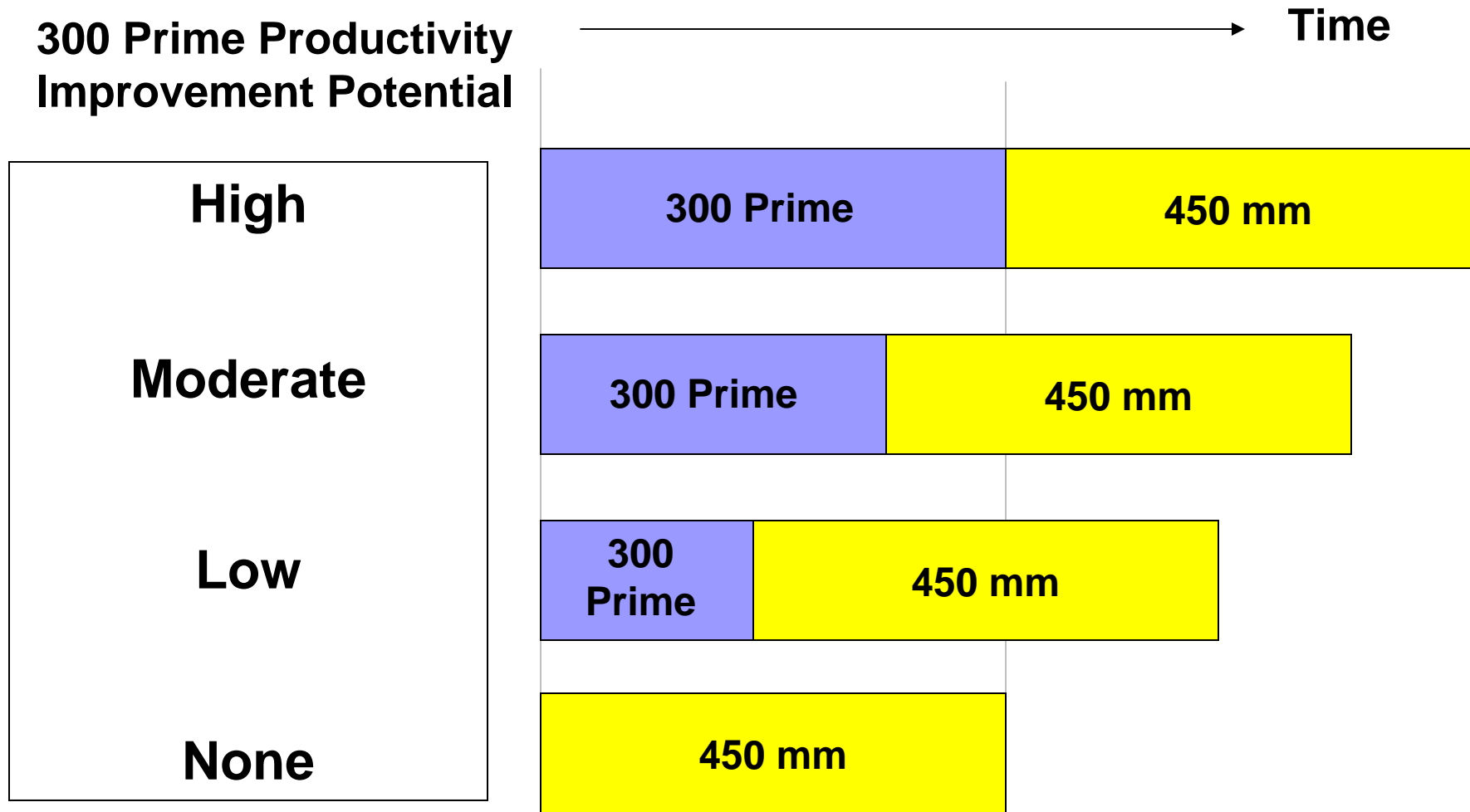
Scope/Timeline will be sync'd with ISMI 450mm program



Many technology issues in 300Prime/450mm need to be addressed!
 FI is working with ISMI 300Prime/450mm Program to be in-sync.
 Need to Sync. with IRC on 2012 interception point



Possible 300 Prime/450 mm Scenarios



Major factors affecting the realistic scope of 300 Prime are benefit potential, R&D difficulty, size of market, and implementation difficulty

Summary

- Over 1200 engineers, scientists, and technologists from five world-wide regions contributed to the 2006 Update.
- Technology pace for the top three leading-edge product groups is unchanged from the 2005 ITRS.
- Lithography—Double-patterning was added as an additional potential solution.
- Front-end Process and Process Integration—Delayed projected deployment of high-k and metal gate and FDSOI by two years, until 2010.
- Test—Test costs still challenging, but returning to historical trends
- More than Moore—ITRS to cover non-digital functionality and market drivers
- 450mm—Industry-wide planning for 300 Prime and 450mm is underway

for more information...

<http://www.itrs.net>