

The following corrections have been made to the figure numbers within the text:

LIST OF FIGURES

Figure 1—	Figure 68	Cu Resistivity
Figure 2—	Figure 69	Delay for Metal 1 and Global Wiring versus Feature Size
Figure 3—	Figure 70	Cross-section of Hierarchical Scaling—MPU Device
Figure 4—	Figure 71	Cross-section of Hierarchical Scaling—ASIC Device
Figure 5—	Figure 72	Typical ILD Architectures
Figure 6—	Figure 73	Dielectric Potential Solutions
Figure 7—	Figure 74	Barrier Potential Solutions
Figure 8—	Figure 75	Conductor Potential Solutions
Figure 9—	Figure 76	Nucleation Potential Solutions
Figure 10—	Figure 77	Planarization Potential Solutions
Figure 11—	Figure 78	Etch Potential Solutions
Figure 12—	Figure 79	Interconnect Surface Preparation Potential Solutions
Figure 13—	Figure A5	ITRS 2003 keff Roadmap Revision

In Dielectric Appendix

Figures 1(a)-(d) —Figures A1 through A4, respectively:

Figure A1	90 nm Potential Solutions (2004)
Figure A2	65 nm Potential Solutions (2007)
Figure A3	45 nm Potential Solutions (2010)
Figure A4	Critical Path in High-end SOC and RC Scaling Scenario

Table 1—Table A1 Assumption on Interconnect Parameter Estimation Model

Textual changes for 2006 Update

Page 2, line 6	Table 80 reference in text changed to Table 79
Page 13, table item	2014 Interlevel metal insulator effective dielectric constant (2.4 - 2.4) corrected value changed to (2.1 - 2.4)
Page 15, line 38	Table 81a and b reference in text changed to Table 80a and
Page 16, line 2	Figure A1-A4 reference in text changed to Figure A1-A3
Page 16, line 7	Figure A2 reference in text changed to Figure A4
Page 16, line 14	Figure A3 reference in text changed to Figure A5
Page 31, line 10	Table 83a & b reference in text changed to Table 82a & b
Page 43, line 2	Table 1A reference in text changed to Table 83
Page 43, line 6	Table 1 reference in text changed to Table 83
Page 43, lines 10-12	Deleted text "Figure A5 is provided to >illustrate the expected timing of the path for the most promising of these alternatives to proceed from research to development to being available (but not necessarily chosen) for implementation."
Page 45, lines 42-44	Add endnote number and reference for the sentence "Optical interconnects are considered a possible option for replacing the conductor/dielectric system for global interconnects. The optical approach has many variants, the simplest perhaps having emitters off-chip and only free space waveguides and detectors in top layers on-chip. Progressively more complex options culminate in monolithic emitters, waveguides, and detectors."
Pages 46-55 and Endnotes 9-64	Renumbered endnote references and endnotes numbering to reflect addition of new endnote 9 [see previous change notation]