INTERNATIONAL
TECHNOLOGY ROADMAP
FOR
SEMICONDUCTORS

2004 UPDATE

RF and Analog/Mixed-signal Technologies for Wireless Communications

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RF AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

2004 UPDATE HIGHLIGHTS

Analog and Mixed Signal: The technology requirements are now aligned for analog speed devices with the LSTP roadmap instead of, as in the past, with the LOP roadmap. It is becoming more challenging to keep a constant ratio of transconductance *gm* to drain conductance *gds* for high performance analog devices in new technologies. The challenges for reducing 1/f noise in high-k gate dielectrics are relaxed to a color coding of "yellow" from "red." However, 1/f noise in high-k gate dielectrics still remains challenging. The published reports about solutions for high density capacitors meeting density, leakage, and matching specifications suggested changes to capacitor color coding for the 2004 ITRS update from red to yellow for the years 2013 to 2016.

RF Transceivers: Similar to the Near Term Table, a lag between RFCMOS gate length and BiCMOS gate length now occurs in the Long Term Table. For RFCMOS, the technology requirements maintained one-year lag from the LSTP CMOS roadmap.

Power Amplifiers & Power Management: The major trends appear to have been correctly anticipated in 2003 for handsets. The first two RFCMOS Dual Band GSM power amplifiers (PAs) were sampled by cellular customers in 2004. These PAs are not expected to be players in the market until 2005. However, RFCMOS PAs could play a major role in 2006. The success of RFCMOS PA’s may erode price margins at a faster rate than anticipated. Multi-band cellular SiGe PAs also are being sampled. Highly integrated modules with multi-layer laminates of low temperature cintered ceramics (LTCC) are dramatically reducing total RF front-end area. The cost ($$/Watt) for basestation PAs will decrease more rapidly than shown in the 2003 Roadmap and are expected to reach $0.40 per watt in 2008. Saturated power density (W/mm) of all technologies will increase more rapidly and will reach 1.4 W/mm, 1.8 W/mm, 3 W/mm, and 5 W/mm by 2008 for LDMOS, GaAs, SiC, and GaN, respectively. Manufacturing solutions now exist for 28V GaAs FET’s, 60W SiC FET’s, and 28 V GaN FET’s. Linear operation is expected to achieve less than half the RF power of saturated operation. In the 2003 Roadmap, linear operation was expected to achieve half the RF power of saturated operation.

Millimeter Wave (10-100GHz): There are no major changes for the 2004 Update. InP HBTs are expected to advance more quickly due to aggressive R&D funding than they were predicted to do so in the 2003 ITRS. The 2005-2006 color coding for all InP HBT device requirmenets are changed from yellow to white. Also, the 2007-2008 figures of merit for device fT and fMAX are more aggressive. Copper interconnects are expected to be introduced in 2007. The use of today's gold and aluminum interconnects is expected to continue until at least 2009.

Link to the 2003 ITRS RF and Analog/Mixed-signal Technologies for Wireless Communications chapter

WORKING GROUP TABLES

Table 53a Analog and Mixed-signal Devices Technology Requirements—Near-term UPDATED

	[1]	Year of Production		2003	2004	2005	2006	2007	2008	2009
		Technology Node			hp90			hp65		
		DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
WAS	[2]	Minimum Supply Voltage	Digital design (V)	1	1	0.95	0.9	0.85	0.8	0.75
IS	[2]	nMOS Analog Speed Device	Supply voltage (V)	1.5	1.2	1.2	1.2	1.1	1.1	1.1
WAS **	[3]	Minimum Supply Voltage	Analog design (V)	3.3–1.8	2.5–1.8	2.5–1.8	2.5–1.8	2.5–1.8	2.5–1.8	2.5–1.8
IS	[7]	entire row MOVED**	Supply voltage (V)							
WAS	[4]	NMOS Analog Speed Device	T_{ox} (nm)	1.2–1.8	1.1–1.6	1.1–1.6	1.1–1.6	0.7–1.2	0.7–1.2	0.7–1.2
IS	[3]	NMOS Analog Speed Device	T_{ox} (nm)	2.3	2.1	2.1	1.9	1.6	1.5	1.4
WAS	[5]	NMOS Analog Speed Device	g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	100	100	100	100	100	100	100
IS	[4]	NMOS Analog Speed Device	g_m / g_{ds} @ $5 \cdot L_{min\text{-}digital}$	100	100	100	100	100	100	100
WAS	[6]	NMOS Analog Speed Device	1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	300	200	200	200	150	150	150
IS	[5]	NMOS Analog Speed Device	1/f-noise ($\mu V^2 \cdot \mu m^2$ / Hz)	300	200	200	200	150	150	150
WAS	[7]	NMOS Analog Speed Device	σV_{th} matching (mV·μm)	5	4	4	4	3	3	3
IS	[6]	NMOS Analog Speed Device	σV_{th} matching (mV·μm)	5	4	4	4	3	3	3
MOVED **	[7]	nMOS Analog Precision Device	Supply voltage (V)	3.3-1.8	2.5 - 1.8	2.5 - 1.8	2.5 - 1.8	2.5 - 1.8	2.5 - 1.8	2.5 - 1.8
WAS	[8]	nMOS Analog Precision Device	T_{ox} (nm)	6.5–3	6.5–3	6.5–3	6.5–3	5–3	5–3	5–3
IS	[8]	nMOS Analog Precision Device	T_{ox} (nm)	6.5-3	5 - 3	5 - 3	5 - 3	5 - 3	5 - 3	5 - 3
WAS	[9]	nMOS Analog Precision Device	Analog V_{th} (V)	0.5–0.3	0.5–0.2	0.4–0.2	0.4–0.2	0.4–0.2	0.3–0.2	0.3–0.2
IS	[9]	nMOS Analog Precision Device	Analog Vth (V)	0.5-0.3	0.4 - 0.2	0.4 -0.2	0.4 - 0.2	0.3 - 0.2	0.3 - 0.2	0.3 - 0.2

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 53a Analog and Mixed-signal Devices Technology Requirements—Near-term UPDATED (continued)

				2003	2004	2005	2006	2007	2008	2009
	[1]	*Year of Production*		*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
		Technology Node			*hp90*			*hp65*		
		DRAM ½ Pitch (nm)		*100*	*90*	*80*	*70*	*65*	*57*	*50*
	[10]	***nMOS Analog Precision Device***	g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	**300**	**300**	**300**	**300**	**300**	**300**	**300**
	[11]	***nMOS Analog Precision Device***	*1/f Noise* ($\mu V^2 \cdot \mu m^2/Hz$)	**500**	**300**	**300**	**300**	**200**	**200**	**200**
	[12]	***nMOS Analog Precision Device***	σV_{th} *matching* ($mV \cdot \mu m$)	**15**	**12**	**12**	**12**	**9**	**9**	**9**
	[13]	*Analog Capacitor*	*Density* ($fF/\mu m^2$)	**2**	**3**	**3**	**3**	**4**	**4**	**4**
	[14]	*Analog Capacitor*	*Voltage linearity* (ppm/V^2)	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**	**<100**
	[15]	*Analog Capacitor*	*Leakage* ($fA / [pF \cdot V]$)	**7**	**7**	**7**	**7**	**7**	**7**	**7**
	[16]	*Analog Capacitor*	σ *Matching* ($\% \cdot \mu m$)	**1**	**0.7**	**0.7**	**0.7**	**0.5**	**0.5**	**0.5**
	[17]	*Analog Resistor*	*Parasitic capacitance* ($fF/\mu m^2$)	**0.1–0.02**	**0.1–0.02**	**0.1–0.02**	**0.1–0.02**	**0.1–0.02**	**0.1–0.02**	**0.1–0.02**
	[18]	*Analog Resistor*	*Temp. linearity* ($ppm/^\circ C$)	**50–80**	**40–80**	**40–80**	**40–80**	**30–60**	**30–60**	**30–60**
	[19]	*Analog Resistor*	*1/f-current-noise per current²* ($1/[\mu m^2/Hz]$)	$\leq 10^{-18}$	$\leq 10^{-18}$	$\leq 10^{-18}$	$\leq 10^{-18}$	$\leq 10^{-18}$	$\leq 6 \times 10^{-19}$	$\leq 6 \times 10^{-19}$
	[20]	*Analog Resistor*	σ *Matching* ($\% \cdot \mu m$)	**3**	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**
	[21]	*Bipolar Analog Device*	g_m/g_{ce} at $W_{e\text{-}min}$ *	**1200**	**1150**	**1150**	**1150**	**1100**	**1100**	**1100**
	[22]	*Bipolar Analog Device*	*1/f-noise* ($\mu V^2 \cdot \mu m^2/Hz$)	**5**	**3**	**3**	**3**	**2**	**2**	**2**
WAS	*[23]*	*Bipolar Analog Device*	σ *current matching* ($\% \cdot \mu m^2$)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
IS	*[23]*	*Bipolar Analog Device*	σ *current matching* ($\% \cdot \mu m$)	2	**2**	**2**	**2**	**2**	**2**	**2**

**Unusual measure for the voltage gain of bipolar devices, see notes. Added for 1:1 comparison with g_m/g_{ds} of MOS transistors (item 5).*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 53b Analog and Mixed-signal Devices Technology Requirements—Long-term UPDATED

	[1]	Year of Production		2010	2011	2012	2013	2014	2015	2016	2017	2018
		Technology Node		hp45			hp32			hp22		
		DRAM ½ Pitch (nm)		45	40	35	32	28	25	22	20	18
WAS	[2]	Minimum Supply Voltage	Digital design (V)	**0.7**		**0.7**	**0.65**		**0.65**	**0.6**		**0.6**
IS	**[2]**	**nMOS Analog Speed Device**	**Supply voltage (V)**	**1.0**	**1.0**	**1.0**	**0.9**	**0.9**	**0.8**	**0.8**	**0.7**	**0.7**
WAS **	[3]	Minimum Supply Voltage	Analog design (V)	**1.8–1.2**	**1.8–1.2**	**1.8–1.2**	**1.8–1.0**		**1.8–1.0**	**1.5–1.0**	**-**	**1.5–1.0**
IS	[7]	**entire row MOVED****	**Supply voltage (V)**									
WAS	[4]	NMOS Analog Speed Device	T_{ox} (nm)	**0.5–0.8**		**0.5–0.8**	**0.4–0.6**	**-**	**0.4–0.6**	**0.4–0.5**	**-**	**0.4–0.5**
IS		NMOS Analog Speed Device		**1.3**	**1.2**	**1.2**	**1.1**	**1.0**	**1.0**	**0.9**	**0.9**	**0.9**
WAS	[5]	NMOS Analog Speed Device	g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	**100**		**100**	**100**	**-**	**100**	**100**	**-**	**100**
IS		NMOS Analog Speed Device		**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
WAS	[6]	NMOS Analog Speed Device	1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	**150**		**150**	**100**	**-**	**100**	**75**	**-**	**75**
IS		NMOS Analog Speed Device		**150**	**150**	**150**	**100**	**100**	**100**	**75**	**75**	**75**
WAS	[7]	NMOS Analog Speed Device	σV_{th} matching (mV·µm)	**2.5**		**2.5**	**2**	**-**	**2**	**1.5**	**-**	**1.5**
IS		NMOS Analog Speed Device	□	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**	**1.5**	**1.5**	**1.5**
IS	**[7]**	**nMOS Analog Precision Device**	**Supply voltage (V)**	**1.8 - 1.2**	**1.8 - 1.2**	**1.8 - 1.2**	**1.8 - 1.0**	**1.8 - 1.0**	**1.8 - 1.0**	**1.5 - 1.0**	**1.5 - 1.0**	**1.5 - 1.0**
WAS	[8]	NMOS Analog Precision Device	T_{ox} (nm)	**3–2**		**3–2**	**3–1.3**	**-**	**3–1.3**	**2.5–1.3**	**-**	**2.0–1.3**
IS		NMOS Analog Precision Device		**3 - 2**	**3 - 2**	**3 - 2**	**3 - 1.3**	**3 - 1.3**	**3 - 1.3**	**2.5 - 1.3**	**2.5 - 1.3**	**2.0 - 1.3**
WAS	[9]	NMOS Analog Precision Device	Analog V_{th} (V)	**0.3–0.2**		**0.3–0.2**	**0.3–0.2**	**-**	**0.3–0.2**	**0.3–0.2**	**-**	**0.3–0.2**
IS		NMOS Analog Precision Device		**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**	**0.3 - 0.2**
WAS	[10]	NMOS Analog Precision Device	g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	**300**		**300**	**300**	**-**	**300**	**300**	**-**	**300**
IS		NMOS Analog Precision Device		**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**
WAS	[11]	NMOS Analog Precision Device	1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$)	**200**		**200**	**150**	**-**	**150**	**100**	**-**	**100**
IS		NMOS Analog Precision Device		**200**	**200**	**200**	**150**	**150**	**150**	**100**	**100**	**100**
WAS	[12]	NMOS Analog Precision Device	σV_{th} matching (mV·µm)	**7.5**		**7.5**	**6**	**-**	**6**	**5**	**-**	**5**
IS		NMOS Analog Precision Device	□	**7.5**	**7.5**	**7.5**	**6**	**6**	**6**	**5**	**5**	**5**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 53b Analog and Mixed-signal Devices Technology Requirements—Long-term UPDATED (continued)

	[1]	Year of Production		2010	2011	2012	2013	2014	2015	2016	2017	2018
		Technology Node		hp45			hp32			hp22		
		DRAM ½ Pitch (nm)		45	40	35	32	28	25	22	20	18
WAS	[13]	Analog Capacitor	Density (fF/μm^2)	5		5	7	-	7	10	-	10
IS		Analog Capacitor		5	5	5	7	7	7	10	10	10
WAS	[14]	Analog Capacitor	Voltage linearity (ppm/V²)	<100		<100	<100	-	<100	<100	-	<100
IS		Analog Capacitor		< 100	< 100	< 100	< 100	< 100	< 100	< 100	< 100	< 100
WAS	[15]	Analog Capacitor	Leakage (fA/[pF·V])	7		7	7	-	7	7	-	7
IS		Analog Capacitor		7	7	7	7	7	7	7	7	7
WAS	[16]	Analog Capacitor	σ Matching (%·μm)	0.4		0.4	0.3	-	0.3	0.2	-	0.2
IS		Analog Capacitor	□	0.4	0.4	0.4	0.3	0.3	0.3	0.2	0.2	0.2
WAS	[17]	Analog Resistor	Parasitic capacitance (fF/μm^2)	0.1–0.02		0.1–0.02	0.1–0.02		0.1–0.02	0.1–0.02		0.1–0.02
IS		Analog Resistor		0.1 - 0.02	0.1 - 0.02	0.1 - 0.02	0.1 - 0.02	0.1 - 0.02	0.1 - 0.02	0.1 - 0.02	0.1 - 0.02	0.1 - 0.02
WAS	[18]	Analog Resistor	Temp. linearity (ppm/ºC)	30–60		30–60	30		30	30		30
IS		Analog Resistor		30 - 60	30 - 60	30 - 60	30	30	30	30	30	30
WAS	[19]	Analog Resistor	1/f-current-noise per current^2 (1/[μm^2/Hz])	≤6×10^{-19}		≤3×10^{-19}	≤3×10^{-19}	-	≤3×10^{-19}	≤2×10^{-19}	-	≤2×10^{-19}
IS		Analog Resistor		> 4.5x10^{-19}	> 4.5x10^{-19}	> 4.5x10^{-19}	> 3x10^{-19}	> 3x10^{-19}	> 3x10^{-19}	> 2x10^{-19}	> 2x10^{-19}	> 2x10^{-19}
WAS	[20]	Analog Resistor	σ Matching (%·μm)	1.7		1.7	1.5	-	1.5	1.2	-	1.2
IS		Analog Resistor	□	1.7	1.7	1.7	1.5	1.5	1.5	1.2	1.2	1.2
WAS	[21]	Bipolar Analog Device	g_m/g_{ce} at $W_{e\text{-}min}$ *	1050		1050	1000	-	1000	950	-	950
IS		Bipolar Analog Device		1050	1050	1050	1000	1000	1000	950	950	950
WAS	[22]	Bipolar Analog Device	1/f-noise (μV^2·μm^2/Hz)	1.5		1.5	1	-	1	0.7	-	0.7
IS		Bipolar Analog Device		1.5	1.5	1.5	1	1	1	0.7	0.7	0.7
WAS	[23]	Bipolar Analog Device	σ current matching (%·μm^2)	20		20	20	-	20	20	-	20
IS		Bipolar Analog Device	□	2	2	2	2	2	2	2	2	2

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

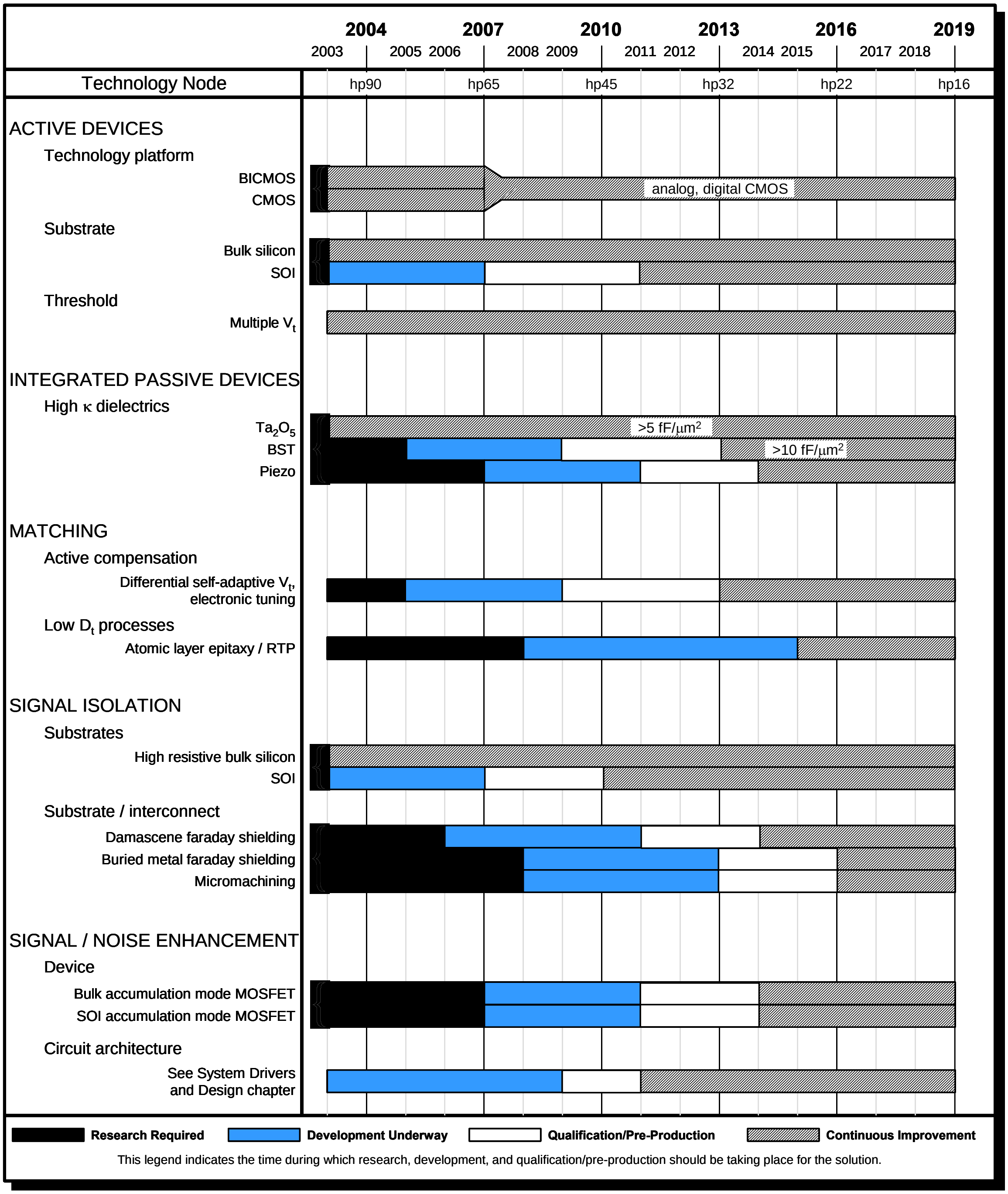

Figure 35 Analog and Mixed-signal Devices Potential Solutions UPDATED

Table 54a 0.8–10 GHz Transceiver Technology Requirements—Near-term UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	Circuit Block—LNA							
	NPN							
	V_{cc} (V)	2.5	2.5	1.8	1.8	1.5	1.5	1.5
WAS	Emitter width (µm)	0.2	0.18	0.15	0.15	0.13	0.12	0.1
IS	Emitter width (µm)	0.2	0.18	0.15	0.14	0.13	0.12	0.1
	I_c (µA/µm) [1]	75	59	43	37	28	22	16
WAS	Peak F_t (GHz) [Vbc=1v]	150	173	198	228	262	302	347
IS	Peak F_t (GHz) [Vbc=1v]	150	173	198	228	262	302	347
WAS	Peak F_{max} (GHz) [2]	180	203	239	256	295	330	387
IS	Peak F_{max} (GHz) [2]	180	203	239	256	295	330	387
WAS	NF_{min} (dB)	0.6	0.54	0.45	0.45	0.39	0.36	0.3
IS	NF_{min} (dB)	0.4	0.36	0.3	0.28	0.26	0.24	0.2
	NMOS							
	V_{dd} (V)	1.5	1.3	1.3	1.3	1.2	1.2	1.1
	I_{ds} (µA/µm) [3]	26	23	21	16	12	10	9
	Peak F_t (GHz)	110	120	140	170	200	240	280
	Peak F_{max} (GHz) [2]	120	140	160	190	220	260	310
WAS	NF_{min} (dB)	0.8	0.7	0.6	0.6	0.5	0.4	0.4
IS	NF_{min} (dB) [3]	0.4	0.33	0.3	0.25	0.22	0.2	<0.2
	Circuit Block Synthesizer/Logic							
	CMOS							
	Gate length (nm) [4]	80	75	65	53	45	37	32
	BiCMOS							
	Gate length (nm)	100	90	80	75	65	53	45
	Circuit Block—VCO							
	Inductor							
	Q (5 GHz) [5]	15	16	17	19	20	22	24
	Varactor							
	Tuning Range [6]	3.5	3.5	3.5	3.5	3.5	3.5	3.5
	Q (5 GHz)	30	32	35	38	41	44	48

Manufacturable solutions exist, and are being optimized	☐
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 54a 0.8–10 GHz Transceiver Technology Requirements—Near-term UPDATED (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
Circuit Block—Driver							
System Requirements							
Supply (V)	**3**	**3**	**3**	**3**	**2.4**	**2.4**	**2.4**
HV NPN							
BV_{CBO} (V)	**12**	**12**	**12**	**12**	**10**	**10**	**10**
Peak F_t (GHz) [Vbc=1V]	**35**	**40**	**46**	**53**	**61**	**70**	**81**
Peak F_{max} (GHz) [2]	**80**	**90**	**106**	**114**	**131**	**146**	**172**
HV MOS							
V_{ds} (V)	**3**	**3**	**3**	**3**	**2.4**	**2.4**	**2.4**
Peak F_t (GHz)	**30**	**30**	**40**	**40**	**50**	**50**	**60**
Peak F_{max} (GHz) [2]	**35**	**35**	**45**	**45**	**55**	**55**	**65**
Circuit. Block—Filters/Bypass							
Cap							
Density (fF/µm^2)	**5**	**7**	**9**	**12**	**15**	**19**	**23**
Q (5 GHz)	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**	**>50**
Resistor							
$C_{parasitic}$ (fF) [7]	**70**	**63**	**57**	**51**	**46**	**41**	**37**
TCR (ppm/C)	**100**	**90**	**81**	**73**	**66**	**59**	**53**
Circuit. Block— Isolation							
S21 dB [8]	**60**	**70**	**80**	**90**	**100**	**110**	**120**

NF—noise figure TCR—temperature coefficient for resistance HV—high voltage

Manufacturable solutions exist, and are being optimized	☐
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 54b 0.8–10 GHz Transceiver Technology Requirements—Long-term UPDATED

	Year of Production	*2012*	*2015*	*2018*
	DRAM ½ Pitch (nm)	*35*	*25*	*18*
	Circuit Block—LNA			
	NPN			
	V_{cc} (V)	**1.2**	**1.2**	**1.2**
	Emitter width (µm)	**0.09**	**0.08**	**0.07**
	I_c (µA/µm) [1]	**13**	**10**	**7**
	Peak F_t (GHz)	**400**	**460**	**530**
	Peak F_{max} (GHz) [2]	**438**	**498**	**572**
WAS	NF_{min} (dB)	**0.27**	**0.24**	**0.21**
IS	NF_{min} (dB)	**0.18**	**0.16**	**0.14**
	NMOS			
	V_{dd} (V)	**1**	**1**	**0.9**
	I_{ds} (µA/µm) [3]	**7**	**4**	**1.5**
	Peak F_t (GHz)	**400**	**700**	**1400**
	Peak F_{max} (GHz) [2]	**450**	**750**	**1500**
WAS	Nf_{min} (dB)	**0.2**	**0.2**	**0.2**
IS	Nf_{min} (dB) [3]	**<0.2**	**<0.2**	**<0.2**
	Circuit Block—Synthesizer/Logic			
	CMOS			
	Gate length (nm) [4]	**22**	**16**	**11**
	BiCMOS			
WAS	Gate length (nm) [4]	**22**	**16**	**11**
IS	Gate length (nm) [4]	**25**	**18**	**13**
	Circuit Block—VCO			
	Inductor			
	Q (5 GHz)	**26**	**28**	**30**
	Varactor			
	Tuning range [6]	**3.5**	**3.5**	**3.5**
	Q (5 GHz)	**52**	**60**	**70**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 54b 0.8–10 GHz Transceiver Technology Requirements—Long-term UPDATED (continued)

Year of Production	*2012*	*2015*	*2018*
DRAM ½ Pitch (nm)	*35*	*25*	*18*
Circuit Block—Driver			
System Requirements			
Supply (V)	**2.4**	**2**	**2**
HV NPN			
BV_{CBO} (V)	**10**	**8**	**8**
Peak F_t (GHz) [Vbc=1V]	**93**	**107**	**123**
Peak F_{max} (GHz) [2]	**195**	**221**	**254**
HV NMOS			
BV_{DSS} (V)	**2.4**	**2.0**	**2.0**
Peak F_t (GHz)	**60**	**100**	**100**
Peak F_{max} (GHz) [2]	**65**	**120**	**120**
Circuit. Block—Filters/Bypass			
Cap			
Density (fF/μm^2)	**27**	**30**	**33**
Q (5 GHz)	**>50**	**>50**	**>50**
Resistor			
$C_{parasitic}$ (fF) [6]	**33**	**30**	**27**
TCR (ppm/C)	**48**	**43**	**29**
Circuit Block—Isolation			
S21 dB [7]	**130**	**140**	**150**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 54a and 54b:

[1] I_c for F_t of 50 GHz for a minimum W_e and unit (1μm) L_e. F_t of 50 GHz is chosen for being 10× the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[2] Peak F_{max} (measured from unilateral gain extrapolated from 40 GHz with a 20 dB/dec slope).

[3] I_{ds} for F_t of 50 GHz for a minimum L and unit (1μm) W. F_t of 50 GHz is chosen for being 10× the application frequency for 5 GHz. An application frequency of 5 GHz is chosen as a mid-point for the frequency range of interest (1–10 GHz).

[4] RF CMOS technology nodes lag low standby power (LSTP) roadmap nodes by one year.

[5] Q at 5 GHz for a 1nH, 30,000 μm^2 inductor.

[6] Defined as C_{max}/C_{min}.

[7] Parasitic capacitance to substrate for a resistor of 1000 Ohms achieving 1% 3-sigma mismatch.

[8] Required to achieve direct modulation of the PA in short term (2–5 GHz). Required to achieve Tx/Rx integration in WCDMA (2 GHz).

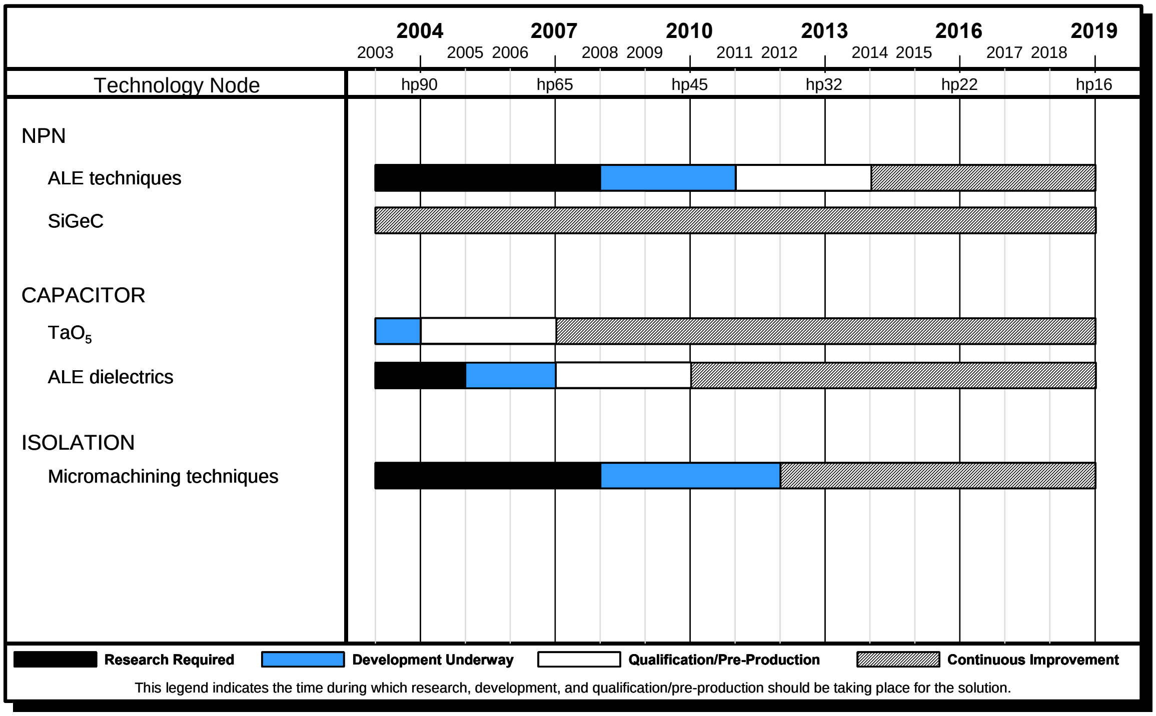

Figure 36 RF Transceivers Potential Solutions UPDATED

Table 55a Power Amplifier Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Nominal PA Supply Voltage (V)	**3**	**3**			**2.4**		
PA Product Solutions	**Integrated Module**		**Single Radio SIP [1]**			**Radio/ Baseband SIP [2]**	
PA Frequency (GHz)	**0.8–2.5**	**0.8–6**			**0.8–10**		
III-V HBT Transistor							
F_{max} (at V_{cc}) (GHz)	**45**	**45**	**45**	**45**	**75**	**75**	**75**
BV_{CBO} (V)	**25**	**25**	**25**	**25**	**18**	**18**	**18**
Linear efficiency (%) [3]	**52**	**52**	**52**	**52**	**55**	**55**	**55**
Area (mm^2) [4]	**2.5**	**2.5**	**2.5**	**2**	**2**	**2**	**2**
Cost/mm^2 (US$) [5]	**0.4**	**0.4**	**0.4**	**0.28**	**0.28**	**0.25**	**0.24**
III-V HBT Integration							
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Filter [8]	**N/A**	**N/A**	**N/A**	**Yes**	**Yes**	**Yes**	**Yes**
III-V PHEMT Transistor							
F_{max} (at V_{dd}) (GHz)	**45**	**45**	**45**	**45**	**75**	**75**	**75**
BV_{DGO} (V)	**20**	**20**	**20**	**20**	**16**	**16**	**16**
Linear Efficiency (%) [3]	**55**	**55**	**55**	**55**	**58**	**58**	**58**
PA Area (mm^2) [4]	**4**	**4**	**4**	**3.5**	**3.5**	**3.5**	**3.5**
Cost/mm^2 (US$) [5]	**0.4**	**0.4**	**0.4**	**0.28**	**0.28**	**0.25**	**0.24**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 55a Power Amplifier Technology Requirements—Near-term (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
III-V PHEMT Integration							
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**N/A**	**N/A**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Filter [8]	**N/A**	**N/A**	**N/A**	**Yes**	**Yes**	**Yes**	**Yes**
III-V Passives							
Inductors Q [9]	**15**	**15**	**15**	**25**	**25**	**25**	**25**
Capacitor Q [10]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
Bypass capacitor density (fF/μm^2) [12]	**0.6**	**0.6**	**0.6**	**2**	**2**	**2**	**2**
RF capacitor density (fF/μm^2) [13]	**0.6**	**0.6**	**0.6**	**2**	**2**	**2**	**2**
Silicon MOSFET Transistor							
T_{ox} (PA) (Å) [11]	**60**	**60**	**60**	**45**	**45**	**45**	**35**
F_{max} (at V_{dd})	**45**	**45**	**45**	**60**	**60**	**60**	**75**
BV_{DSS} (V)	**12**	**12**	**12**	**10**	**10**	**10**	**8**
Linear efficiency (%) [3]	**45**	**45**	**45**	**50**	**50**	**50**	**52**
PA Area (mm^2) [4]	**6**	**6**	**6**	**4.5**	**4.5**	**4.5**	**3**
Cost/mm^2 (US$) [5]	**0.1**	**0.08**	**0.08**	**0.06**	**0.06**	**0.06**	**0.05**
Silicon MOSFET Integration							
Power management [8]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch [9]	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter [10]	**NO**	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
SiGe HBT Transistor							
F_{max} (GHz)	**45**	**60**	**60**	**80**	**80**	**80**	**80**
BV_{CBO} (V)	**18**	**18**	**18**	**16**	**16**	**12**	**12**
Linear efficiency (%) [3]	**50**	**50**	**50**	**55**	**55**	**55**	**55**
PA Area (mm^2) [4]	**2.5**	**2.2**	**2.2**	**2**	**2**	**1.7**	**1.7**
Cost/mm^2 (US$) [5]	**0.15**	**0.15**	**0.12**	**0.12**	**0.11**	**0.11**	**0.11**
SiGe Integration							
Power management	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter	**NO**	**NO**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Silicon / SiGe Passives							
Inductors Q [9]	**10**	**10**	**10**	**14**	**14**	**14**	**14**
Capacitor Q [10]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
Bypass capacitor density (fF/μm^2) [12]	**2**	**4**	**4**	**20**	**20**	**30**	**30**
RF capacitor density (fF/μm^2) [13]	**2**	**4**	**4**	**6**	**6**	**8**	**8**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 55b Power Amplifier Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Nominal PA Supply Voltage (V)	**2.4**	**2.4**	**2.4**	**2**	**2**	**2**
PA Product Solutions	**Radio/Baseband SIP [2]**					
PA Frequency (GHz)	**0.8–10 GHz**					
III-V HBT Transistor						
F_{max} (at V_{cc}) (GHz)	**75**	**75**	**75**	**75**	**75**	**75**
BV_{CBO} (V)	**18**	**18**	**18**	**18**	**18**	**18**
Linear efficiency (%) [3]	**55**	**55**	**55**	**55**	**55**	**55**
Area (mm^2) *[4]*	**2**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**
*Cost/*mm^2 *(US$) [5]*	**0.24**	**0.22**	**0.2**	**0.15**	**0.15**	**0.15**
III-V HBT Integration						
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Filter [8]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
III-V PHEMT Transistor						
F_{max} (at V_{dd}) (GHz)	**75**	**75**	**75**	**75**	**75**	**75**
BV_{DGO} (V)	**16**	**16**	**16**	**16**	**16**	**16**
Linear efficiency (%) [3]	**58**	**58**	**58**	**58**	**58**	**58**
PA Area (mm^2) *[4]*	**3.5**	**3**	**3**	**3**	**3**	**3**
*Cost/*mm^2 *(US$) [5]*	**0.24**	**0.22**	**0.2**	**0.15**	**0.15**	**0.15**
III-V PHEMT Integration						
Power management [6]	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Switch [7]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Filter [8]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
III-V Passives						
Inductors Q [9]	**25**	**30**	**30**	**30**	**30**	**30**
Capacitor Q [10]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
Bypass capacitor density (fF/μm^2) *[12]*	**2**	**2**	**2**	**2**	**2**	**2**
RF capacitor density (fF/μm^2) *[13]*	**2**	**2**	**2**	**2**	**2**	**2**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 55b Power Amplifier Technology Requirements—Long-term (continued)

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
Silicon MOSFET Transistor						
T_{ox} *(PA) (Å) [11]*	**35**	**35**	**35**	**35**	**35**	**35**
F_{max} *(at* V_{dd}*)*	**75**	**75**	**75**	**35**	**35**	**35**
BV_{DSS} *(V)*	**8**	**8**	**8**	**2**	**2**	**2**
Linear efficiency (%) [3]	**52**	**52**	**52**			
PA Area (mm^2*) [4]*	**3**	**3**	**3**	**1.5**	**1.5**	**1.5**
Cost/mm^2 *(US$) [5]*	**0.05**	**0.05**	**0.05**			
Silicon MOSFET Integration						
Power management [8]	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch [9])	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter [10]	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
SiGe HBT Transistor						
F_{max} *(GHz)*	**80**	**80**	**80**	**TBD**	**TBD**	**TBD**
BV_{CBO} *(V)*	**12**	**12**	**10**	**10**	**10**	**10**
Linear efficiency (%) [3]	**55**	**55**	**55**	**TBD**	**TBD**	**TBD**
PA Area (mm^2*) [4]*	**1.7**	**1.5**	**1.5**	**TBD**	**TBD**	**TBD**
Cost/mm^2 *(US$) [5]*	**0.11**	**0.1**	**0.1**	**TBD**	**TBD**	**TBD**
SiGe Integration						
Power management	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Switch	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Filter	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**	**MEMS**
Silicon / SiGe Passives						
Inductors Q [9]	**14**	**18**	**18**	**18**	**18**	**18**
Capacitor Q [10]	**>100**	**>100**	**>100**	**>100**	**>100**	**>100**
Bypass capacitor density (fF/μm^2*) [12]*	**30**	**40**	**40**	**40**	**40**	**40**
RF capacitor density (fF/μm^2*) [13]*	**8**	**10**	**15**	**20**	**20**	**20**

Manufacturable solutions exist, and are being optimized	☐
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Notes for Tables 55a and 55b:

[1] Single radio SIP—system-in-package implementation of a complete post-baseband radio design, including power management, transceiver, power amplifier, filters, and switch functions.

[2] Radio/baseband SIP—system-in-package implementation of a complete baseband and radio design, including [1].

[3] Linear efficiency—power added efficiency of the final PA stage under personal communication service (PCS) CDMA (IS-95) modulation.

[4] Area—total semiconductor area necessary for the implementation of the quad-band GSM/general packet radio service (GPRS)/ Enhanced Data rates for GSM Evolution (EDGE) PA function, including matching/filtering.

[5] Cost/mm^2*—approximate commercial foundry cost of the area mentioned in [4].*

[6] Power management—capability of the technology to provide RF power detection/DC power management for the PA.

[7] Switch—capability of the technology to integrate cost-effectively a transmit/receive switch into the PA active die.

[8] Filter—capability of the technology to integrate high-quality band selection filters needed for the assumed PA solution; currently performed with surface acoustic wave (SAW) filter technology.

[9] Inductor Q—quality factor of a 5nH inductor at 1 GHz achievable with the technology with a metallization suitable for handling the power requirements of the PA.

[10] Capacitor Q—quality factor of a 10pF capacitor at 1 GHz achievable with the technology. Capacitor breakdown voltage must be rated for appropriate power amplification function.

[11] T_{ox} *(PA)—thickness of the MOSFET transistor in the RF power amplifier function.*

[12] Bypass capacitor density—bypass capacitor connected between V_{dd} *(or* V_{cc}*) and ground. Capacitor breakdown voltage must be rated for appropriate power amplification function.*

[13] RF capacitor density—capacitor used for all other functions (matching, harmonic filtering, coupling, etc). Capacitor must have adequate breakdown for the given application.

Table 56a Base Station Devices Technology Requirements—Near-term UPDATED

	Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	Application frequency (GHz)	0.8–2	0.8–2.7			0.8–3.5		
WAS	*Cost ($$/Watt)*	1	0.9	0.8	0.7	0.6	0.5	
IS	*Cost ($$/Watt)*	1	0.8	0.7	0.6	0.5	0.4	
	Packaging (C-Ceramic, P-Plastic)	C/P	C/P	C/P	Plastic			
	Si LDMOS							
	Operating voltage (V)	28	28	<40	<40	<50	<50	<50
	Saturated power (Watt)	240	240	240	240	240	240	240
WAS	Saturated power density (W/mm)	0.7	0.7	0.9	0.9	1.2	1.2	1.2
IS	Saturated power density (W/mm)	0.7	0.8	1	1.2	1.4	1.4	1.4
	Saturated PAE (%)	60	63	65	68	65	68	70
WAS	Linear power (Watt)	120	120	120	120	120	120	120
IS	Linear power (Watt)	<120	<120	<120	<120	<120	<120	<120
	Linear PAE (%)	45	48	50	52	50	52	54
	GaAs FET							
WAS	Operating voltage (V)	12	12	12	28	28	28	28
IS	Operating voltage (V)	12	12	28	28	28	28	28
	Saturated power (Watt)	180	180	180	180	180	180	180
WAS	Saturated power density (W/mm)	0.7	0.7	0.7	1	1.2	1.5	1.5
IS	Saturated power density (W/mm)	0.7	0.7	1	1.2	1.5	1.8	1.8
	Saturated PAE (%)	65	65	68	70	68	70	72
WAS	Linear power (Watt)	90	90	90	90	90	90	90
IS	Linear power (Watt)	<90	<90	<90	<90	<90	<90	<90
	Linear PAE (%)	50	50	52	55	57	55	57
	SiC FET							
	Operating voltage (V)	48	48	48	48	48	48	48
	Saturated power (Watt)	10	30	60	60	60	60	60
WAS	Saturated power density (W/mm)	2	2	2	2	2	2	2
IS	Saturated power density (W/mm)	2		3	3	3	3	3
WAS	Saturated PAE (%)	45	45	45	45	45	45	45
IS	Saturated PAE (%)	45	45	45	45	47	47	47
	GaN FET							
	Operating voltage (V)	-	-	28	28	48	48	48
WAS	Saturated power (Watt)	-	-	10	30	60	60	180
IS	Saturated power (Watt)	-	-	30	30	60	60	180
WAS	Saturated power density (W/mm)	-	-	2	2	4	4	4
IS	Saturated power density (W/mm)	-	-	3	3	5	5	5
	Saturated PAE (%)	-	-	52	55	50	52	55

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 56b Base Station Devices Technology Requirements—Long-term UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
	Application frequency (GHz)	**0.8–5**								
WAS	*Cost ($$/Watt)*	**0.4**			**0.3**					
IS	*Cost ($$/Watt)*	**0.3**			**0.25**					
	Packaging (C–Ceramic, P–Plastic)	**Plastic**								
	Si LDMOS									
	Operating voltage (V)	**<50**		**<50**	**<50**		**<50**	**<50**		**<50**
	Saturated power (Watt)	**240**		**240**	**240**		**240**	**240**		**240**
WAS	Saturated power density (W/mm)	**1.2**		**1.2**	**1.2**		**1.2**	**1.2**		**1.2**
IS	Saturated power density (W/mm)	**1.4**	_	**1.4**	**1.4**	_	**1.4**	**1.4**	_	**1.4**
	Saturated PAE (%)	**65**		**65**	**70**		**70**	**70**		**70**
WAS	Linear power (Watt)	**120**		**120**	**120**		**120**	**120**		**120**
IS	Linear power (Watt)	**<120**	_	**<120**	**<120**	_	**<120**	**<120**	_	**<120**
	Linear PAE (%)	**50**		**50**	**52**		**52**	**52**		**52**
	GaAs FET									
	Operating voltage (V)	**28**		**28**	**28**		**28**	**28**		**28**
	Saturated power (Watt)	**180**		**180**	**180**		**180**	**180**		**180**
WAS	Saturated power density (W/mm)	**1.5**		**1.5**	**1.5**		**1.5**	**1.5**		**1.5**
IS	Saturated power density (W/mm)	**1.8**	_	**1.8**	**1.8**	_	**1.8**	**1.8**	_	**1.8**
	Saturated PAE (%)	**68**		**68**	**70**		**70**	**72**		**72**
WAS	Linear power (Watt)	**90**		**90**	**90**		**90**	**90**		**90**
IS	Linear power (Watt)	**<90**	_	**<90**	**<90**	_	**<90**	**<90**	_	**<90**
	Linear PAE (%)	**52**		**52**	**55**		**55**	**57**		**57**
	SiC FET									
	Operating voltage (V)	**48**		**48**	**48**		**48**	**48**		**48**
	Saturated power (Watt)	**60**		**60**	**60**		**60**	**60**		**60**
WAS	Saturated power density (W/mm)	**2**		**2**	**2**		**2**	**2**		**2**
IS	Saturated power density (W/mm)	**3**	_	**3**	**3**	_	**3**	**3**	_	**3**
WAS	Saturated PAE (%)	**45**		**45**	**45**		**45**	**45**		**45**
IS		**47**	_	**47**	**47**	_	**47**	**47**	_	**47**
	GaN FET									
	Operating voltage (V)	**48**		**48**	**48**		**48**	**48**		**48**
	Saturated power (Watt)	**180**		**180**	**180**		**180**	**180**		**180**
WAS	Saturated power density (W/mm)	**4**		**4**	**4**		**4**	**4**		**4**
IS	Saturated power density (W/mm)	**5**	_	**5**	**5**	_	**5**	**5**	_	**5**
	Saturated PAE (%)	**50**		**50**	**52**		**52**	**55**		**55**

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term UPDATED

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—FET **							
GaAs MESFET (digital mixed-signal)							
Gate length—L physical (nm)	**250**	**250**	**150**	**150**	**-**	**-**	**-**
Minimum M1 pitch (nm)	**1200**	**1200**	**680**	**680**	**-**	**-**	**-**
F_t - enhancement mode (GHz)	**80**	**80**	**120**	**120**	**-**	**-**	**-**
F_t - depletion mode (GHz)	**70**	**70**	**100**	**100**	**-**	**-**	**-**
BV_{GD} (1mA/mm, V_g=0) (volts)	**7.5**	**7.5**	**5 to 10**	**5 to 10**	**-**	**-**	**-**
Power delay product at gate delay-FO=1 (fJ at pS)	**2 at 25**	**2 at 25**	**1.2 at 18**	**1.2 at 18**	**-**	**-**	**-**
Shortest DCFL gate delay (pS)	**10**	**10**	**6**	**6**	**-**	**-**	**-**
Interconnect metal layers	**4**	**4**	**5**	**5**	**-**	**-**	**-**
Interconnect metal	**Al**	**Al**	**Al**	**Al**	**-**	**-**	**-**
Inter line dielectric constant (effective)	**4.2**	**4.2**	**3.1**	**3.1**	**-**	**-**	**-**
GaAs PHEMT (low noise)							
Gate length (nm)	**100**	**100**	**70**	**70**	**50**	**50**	**32**
F_t (GHz)	**130**	**130**	**150**	**150**	**170**	**170**	**200**
Breakdown (volts)	**7**	**7**	**7**	**7**	**6**	**6**	**5.5**
I_{max} (mA/mm)	**650**	**650**	**600**	**600**	**550**	**550**	**550**
G_m (S/mm)	**0.65**	**0.65**	**0.8**	**0.8**	**0.9**	**0.9**	**1**
NF (dB) at 26 GHz, 18–20 dB associated gain	**3.1**	**3.1**	**2.5**	**2.5**	**2**	**2**	**1.5**
NF (dB) at 94 GHz, 8–10 dB associated gain	**4.8**	**4.8**	**4**	**4**	**3.5**	**3.5**	**3**
GaAs PHEMT (power)							
Gate length (nm)	**200**	**200**	**100**	**100**	**70**	**70**	**-**
F_{max} (GHz)	**75**	**75**	**150**	**150**	**200**	**200**	**-**
Breakdown (volts)	**11**	**11**	**11**	**11**	**9**	**9**	**-**
I_{max} (ma/mm)	**650**	**650**	**750**	**750**	**850**	**850**	**-**
G_m (S/mm)	**0.52**	**0.52**	**0.67**	**0.67**	**0.85**	**0.85**	**-**
P_{out} at 26 GHz and peak efficiency (mW/mm)	**500**	**500**	**550**	**550**	**600**	**600**	**-**
Peak efficiency at 26 GHz (%)	**20**	**20**	**30**	**30**	**40**	**40**	**-**
Gain at 26 GHz, at P_{1dB} (dB)***	**10**	**10**	**12**	**12**	**14**	**14**	**-**
P_{out} at 94 GHz and peak efficiency (mW/mm)	**250**	**250**	**-**	**-**	**-**	**-**	**-**
Peak efficiency at 94 GHz (%)	**15**	**15**	**-**	**-**	**-**	**-**	**-**
Gain at 94 GHz, at P_{1dB} (dB)***	**6**	**6**	**-**	**-**	**-**	**-**	**-**

DCFL—direct-coupled FET logic

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term UPDATED (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—FET **							
InP HEMT (low noise)							
Gate length (nm)	**-**	**100**	**70**	**70**	**50**	**50**	**32**
F_t (GHz)	**-**	**200**	**240**	**240**	**300**	**300**	**350**
Breakdown (volts)	**-**	**4**	**3.5**	**3.5**	**3**	**3**	**2.5**
I_{max} (ma/mm)	**-**	**700**	**700**	**700**	**650**	**650**	**600**
G_m (S/mm)	**-**	**1**	**1.2**	**1.2**	**1.5**	**1.5**	**1.8**
NF (dB) at 26 GHz, 20–23 dB associated gain	**-**	**2.2**	**1.8**	**1.8**	**1.5**	**1.5**	**1.2**
NF (dB) at 94 GHz, 10–13 dB associated gain	**-**	**3**	**2.5**	**2.5**	**2**	**2**	**1.8**
InP HEMT (power)							
Gate length (nm)	**-**	**-**	**150**	**100**	**100**	**100**	**100**
F_{max} (GHz)	**-**	**-**	**200**	**220**	**260**	**260**	**260**
Breakdown (volts)	**-**	**-**	**5**	**5**	**6**	**6**	**6**
I_{max} (ma/mm)	**-**	**-**	**750**	**700**	**650**	**650**	**650**
G_m (S/mm)	**-**	**-**	**0.8**	**0.9**	**0.9**	**0.9**	**0.9**
P_{out} at 26 GHz and peak efficiency (mW/mm)	**-**	**-**	**400**	**400**	**450**	**450**	**450**
Peak efficiency at 26 GHz (%)	**-**	**-**	**30**	**40**	**50**	**50**	**50**
Gain at 26 GHz, at P_{1dB} (dB)***	**-**	**-**	**12**	**15**	**15**	**16**	**16**
P_{out} at 94 GHz and peak efficiency (mW/mm)	**-**	**-**	**250**	**300**	**350**	**350**	**400**
Peak efficiency at 94 GHz (%)	**-**	**-**	**25**	**40**	**40**	**45**	**45**
Gain at 94 GHz, at P_{1dB} (dB)***	**-**	**-**	**6**	**8**	**10**	**10**	**12**
GaAs MHEMT (low noise)							
Gate length (nm)	**-**	**-**	**100**	**100**	**70**	**70**	**50**
F_t (GHz)	**-**	**-**	**250**	**250**	**300**	**300**	**400**
Breakdown (volts)	**-**	**-**	**5**	**5**	**4**	**4**	**3**
I_{max} (ma/mm)	**-**	**-**	**680**	**680**	**680**	**680**	**680**
G_m (S/mm)	**-**	**-**	**1**	**1**	**1**	**1**	**1**
NF (dB) at 26 GHz, 10–23 dB associated gain	**-**	**-**	**1.6**	**1.6**	**1.2**	**1.2**	**0.8**
NF (dB) at 94 GHz, 10–13 dB associated gain	**-**	**-**	**2.3**	**2.3**	**1.8**	**1.8**	**1.6**

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term UPDATED (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
*Device Technology—FET **							
GaAs MHEMT (Power)							
Gate length (nm)	-	-	-	**200**	**100**	**100**	**100**
F_{max} (GHz)	-	-	-	**200**	**250**	**275**	**300**
Breakdown (volts)	-	-	-	**8**	**8**	**8**	**9**
I_{max} (ma/mm)	-	-	-	**600**	**600**	**600**	**600**
G_m (S/mm)	-	-	-	**0.8**	**0.9**	**0.9**	**0.9**
P_{out} at 26 GHz and peak efficiency (mW/mm)	-	-	-	**350**	**500**	**600**	**750**
Peak efficiency at 26 GHz (%)	-	-	-	**45**	**55**	**55**	**60**
Gain at 26 GHz, at P_{1dB} (dB)***	-	-	-	**12**	**15**	**16**	**16**
P_{out} at 94 GHz and peak efficiency (mW/mm)	-	-	-	**200**	**350**	**400**	**450**
Peak efficiency at 94 GHz (%)	-	-	-	**25**	**40**	**45**	**45**
Gain at 94 GHz, at P_{1dB} (dB)***	-	-	-	**6**	**8**	**10**	**12**
GaN HEMT (low noise)							
Gate length (nm)	-	-	-	-	**150**	**100**	**100**
F_t (GHz)	-	-	-	-	**100**	**100**	**120**
Breakdown (volts)	-	-	-	-	**>40**	**60**	**60**
I_{max} (ma/mm)	-	-	-	-	**>1000**	**1200**	**1500**
G_m (S/mm)	-	-	-	-	**>0.3**	**0.4**	**0.5**
NF (dB) at 26 GHz, 14 dB gain	-	-	-	-	**2**	**2**	**1.5**
GaN HEMT (power)							
Gate length (nm)	-	-	-	-	**150**	**100**	**100**
F_{max} (GHz)	-	-	-	-	**100**	**100**	**150**
Breakdown (volts)	-	-	-	-	**>40**	**60**	**60**
I_{max} (ma/mm)	-	-	-	-	**>1000**	**1200**	**1500**
G_m (S/mm)	-	-	-	-	**>0.3**	**0.4**	**0.5**
P_{out} at 26 GHz and peak efficiency (mW/mm)	-	-	-	-	**3000**	**5000**	**5000**
Peak efficiency at 26 GHz (%)	-	-	-	-	**35**	**40**	**50**
Gain at 26 GHz, at P_{1dB} (dB)***	-	-	-	-	**10**	**12**	**12**

** Lithography dimensions are drawn dimensions.*

*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*

**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥

Table 57 Millimeter Wave 10–100 GHz Technology Requirements—Near-term UPDATED (continued)

	Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
	Technology Node		*hp90*			*hp65*		
	DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
	*Device Technology—HBT **							
	InP HBT							
WAS	Emitter width (nm)	**1200**	**800**	**350**	**350**	**250**	**250**	**150**
IS	Emitter width (nm)	**1200**	**800**	**350**	**350**	**250**	**250**	**150**
WAS	F_t (GHz)	**170**	**170**	**300**	**300**	**300**	**300**	**400**
IS	F_t (GHz)	**170**	**170**	**300**	**300**	**350**	**350**	**400**
WAS	F_{max} (GHz)	**170**	**200**	**300**	**300**	**350**	**350**	**450**
IS	F_{max} (GHz)	**170**	**200**	**300**	**300**	**400**	**400**	**450**
WAS	Breakdown (BV_{CEO}) (volts)	**7**	**7**	**4**	**4**	**4**	**4**	**3**
IS	Breakdown (BV_{CEO}) (volts)	**7**	**7**	**4**	**4**	**4**	**4**	**3**
WAS	$I_{max}/\mu m^2$ ($mA/\mu m^2$)	**1.5**	**2**	**5**	**4**	**4**	**4**	**5**
IS	$I_{max}/\mu m^2$ ($mA/\mu m^2$)	**1.5**	**2**	**4**	**5**	**5**	**5**	**7**
WAS	Beta	**20**	**50**	**50**	**50**	**50**	**50**	**50**
IS	Beta	**20**	**50**	**50**	**50**	**50**	**50**	**50**
WAS	3 sigma V_{BE} (mV)	**50**	**40**	**40**	**30**	**30**	**25**	**25**
IS	3 sigma V_{BE} (mV)	**50**	**40**	**40**	**30**	**30**	**25**	**25**
	Interconnect metal layers	**3**	**4**	**4**	**4**	**5**	**5**	**5**
WAS	Interconnect metal	**Al, Au**	**Al, Au**	**Al, Au**	**Al, Au**	**Cu**	**Cu**	**Cu**
IS	Interconnect metal	**Al, Au**	**Al, Au**	**Al, Au**	**Al, Au**	**Al, Au, Cu**	**Al, Au, Cu**	**Al, Au, Cu**
	Barrier	**PVD**	**PVD**	**PVD**	**PVD**	**IMP**	**IMP**	**IMP**
	Wafer diameter (mm)	**100**	**100**	**100**	**100**	**150**	**150**	**150**
	SiGe HBT							
	Emitter Width (nm)	**200**	**150**	**120**	**120**	**100**	**100**	**70**
	F_t (GHz)	**150**	**175**	**200**	**230**	**265**	**300**	**350**
	F_{max} (GHz)	**180**	**205**	**240**	**260**	**300**	**330**	**390**
	Breakdown (BV_{CBO}) (volts)	**6**	**5.5**	**5.3**	**5**	**5**	**4.5**	**4.5**
	Breakdown (BV_{CEO}) (volts)	**2.3**	**2**	**2**	**2**	**1.8**	**1.8**	**1.8**
	$I_{max}/\mu m^2$ ($mA/\mu m^2$)	**7**	**8**	**10**	**14**	**14**	**18**	**18**
	Beta	**140**	**200**	**200**	**200**	**250**	**250**	**300**
	Nf_{min} at 77 GHz (dB)	**6.6**	**6.1**	**5.5**	**5.1**	**4.6**	**4.3**	**3.9**

**Lithography dimensions are drawn dimensions.*
*** Output power at peak efficiency is generally at 2 to 3 dB into compression; P_{out} is normalized to total gate periphery.*
**** P_{1dB} (dB) is the point at which the device gain is 1 dB less than the linear gain, i.e., the gain is compressed by 1 dB.*

Manufacturable solutions exist, and are being optimized	⬜
Manufacturable solutions are known	🟨
Interim solutions are known	◆
Manufacturable solutions are NOT known	🟥