INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Process Integration, Devices, and Structures

Jointly Sponsored
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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

2004 UPDATE HIGHLIGHTS

The 2004 update for the Process Integration, Devices and Structures (PIDS) section of the ITRS has minor changes and corrections from the 2003 edition. The most notable change is that in the long-term technology requirements tables, the years 2011, 2014, and 2017 have been added, so that all years from 2010 through 2018 are now included. As expected, the parameter values for these added years are generally close to midway between the values for the previous and succeeding years. In Figure 23, which is for low standby power logic, the curve for maximum allowed gate leakage current density (labeled "Jg,limit") has been corrected. In the 2003 edition, this curve was low by a factor of 2 to 3. Even with the correction, the implication of the figure is unchanged, that oxynitride gate dielectric is projected to be unable to meet the gate leakage current limits by 2006.

Link to the 2003 ITRS Process Integration, Devices, and Structures chapter

WORKING GROUP TABLES

Table 46a Process Integration Difficult Challenges—Near-term

Difficult Challenges ≥45 nm/Through 2010	*Summary of Issues*
1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs	Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage Difficulty in controlling short-channel effects for highly scaled devices Negative impact of high channel doping needed for highly scaled devices. Also, the difficulty in controlling threshold voltage due to statistical fluctuations in the doping Need to reduce series S/D parasitic resistance Controlling static power dissipation in the face of rapidly increasing leakage: architecture and circuit design improvement and innovation will be needed.
2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs	Early availability of manufacturing-worthy high-κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. Slow scaling of V_{dd} for low standby power logic will make overall device scaling difficult. Rapid scaling of V_{dd} for low operating power logic will make overall device scaling difficult.
3. Assuring the reliability and implementing into manufacturing of multiple material, process, and structural changes in a relatively short period of time	Multiple material changes projected: high-κ gate dielectric, metal gate electrodes, strained Si, nickel silicide by 2008 or so Elevated S/D (selective epi) Ultra-thin body (UTB) SOI by 2008 or so, followed by multiple-gate structures. Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Difficulty in ensuring reliability of all these new materials, processes, and structures in a timely manner

Table 46a Process Integration Difficult Challenges—Near-term (continued)

4. Implementation of DRAM, SRAM, and high-density nonvolatile memory (NVM) for scaled technologies	DRAM main issues—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities with scaling. Also, difficult lithography and etch issues with scaling NVM, flash—Scaling of tunnel dielectric and interpoly dielectric involves many complex tradeoffs. Dielectric material properties and dimensional control are key issues NVM, FeRAM—Ferroelectric material properties and dimensional control. Sensitivity to IC processing temperatures and conditions NVM, SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy NVM, MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions
5. High-performance and low-cost RF and analog/mixed-signal solutions	Signal isolation Optimizing RF/analog CMOS devices with scaled technologies: mismatch, 1/f noise, and leakage with high-κ gate dielectrics High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors Reduced power supply voltages: degradation in SNR (signal-to-noise ratio) and signal distortion performance Reduced device breakdown voltage in scaled technologies High-frequency devices with increased operating voltage for base station applications Compound semiconductor substrates with good thermal dissipation and process equipment for fabrication at low cost See section on RF and A/MS Technologies for Wireless Communications for detailed discussion of these issues

Table 46b Process Integration Difficult Challenges—Long-term

Difficult Challenges < 45 nm/Beyond 2010	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate, ultra-thin body [UTB] MOSFETs) with lightly doped body will be needed to effectively scale MOSFETs to well under 20 nm gate length (L_g). Most likely, advanced material solutions such as strained Si (enhanced mobility) channels, elevated source/drain, high-κ gate dielectric, metal gate electrode, etc., will be utilized along with the advanced non-classical CMOS Particularly for the highly scaled UTB MOSFETs required towards the end of the Roadmap, with body thickness well under 10 nm, electrical performance and the impact of quantum effects are not well understood To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced carrier saturation velocity appears to be needed See Emerging Research Devices section for more detail.
7. Dealing with atomic-level fluctuations and statistical process variations in sub-20 nm MOSFETs	Fundamental issues of atomic-level statistical fluctuations for sub-20 nm MOSFETs are not completely understood, including the impact of quantum effects.
8. Identifying, selecting, and implementing new memory structures	Highly scaled, dense, fast, non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness, attaining the very low leakage currents that will be required, and reducing the cell area factor All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc,) are currently unclear.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate into a CMOS platform. Integration of the two may be difficult, especially for mixed signal. See Emerging Research Devices sections for more discussion and detail.

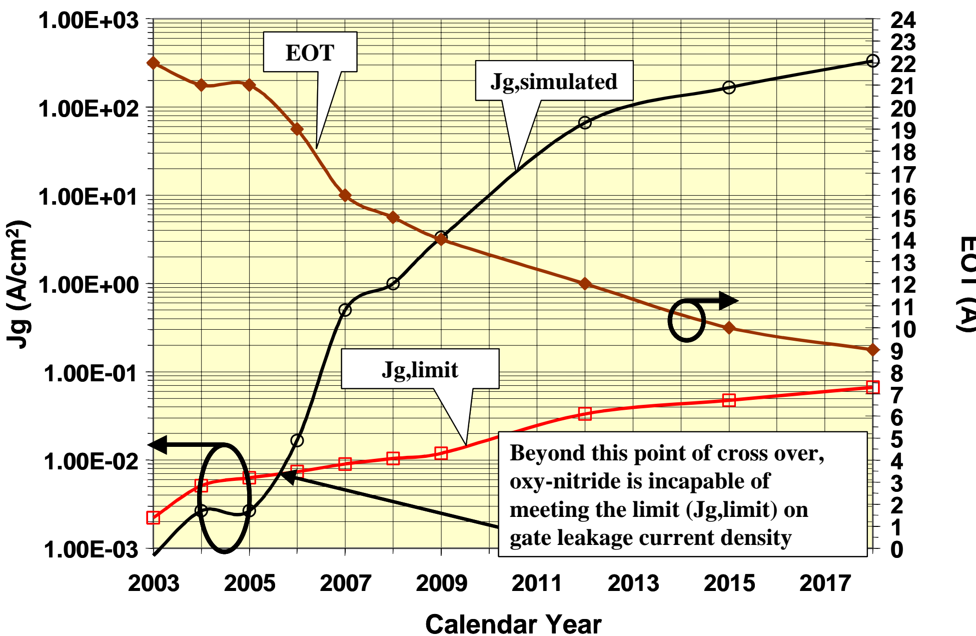


Figure 23 LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

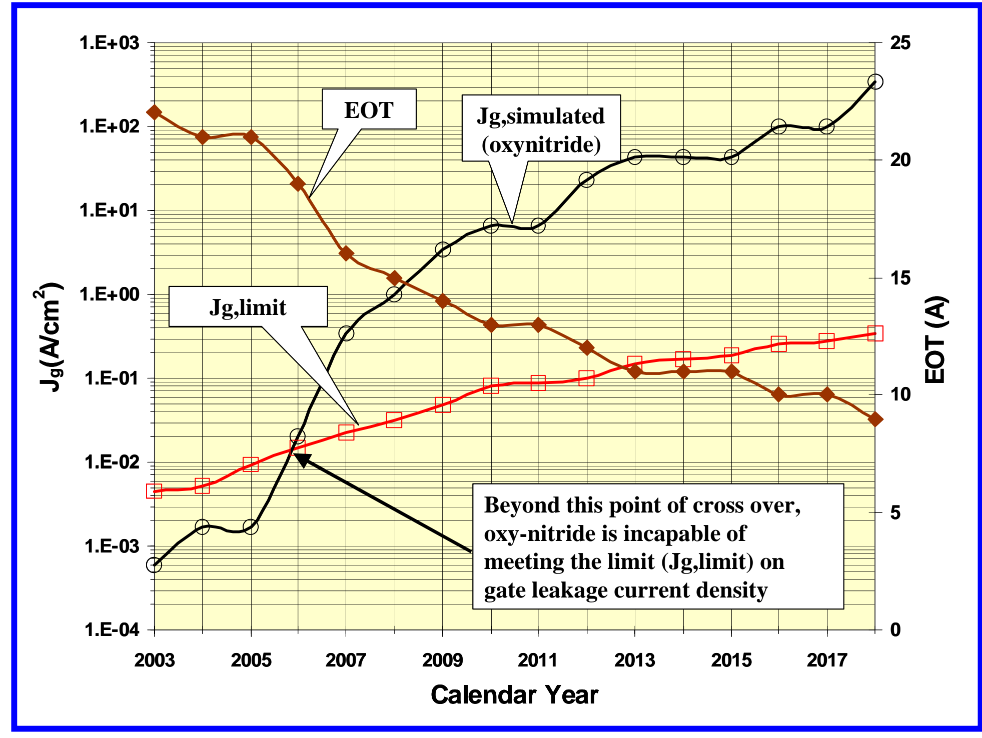


Figure 23 LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

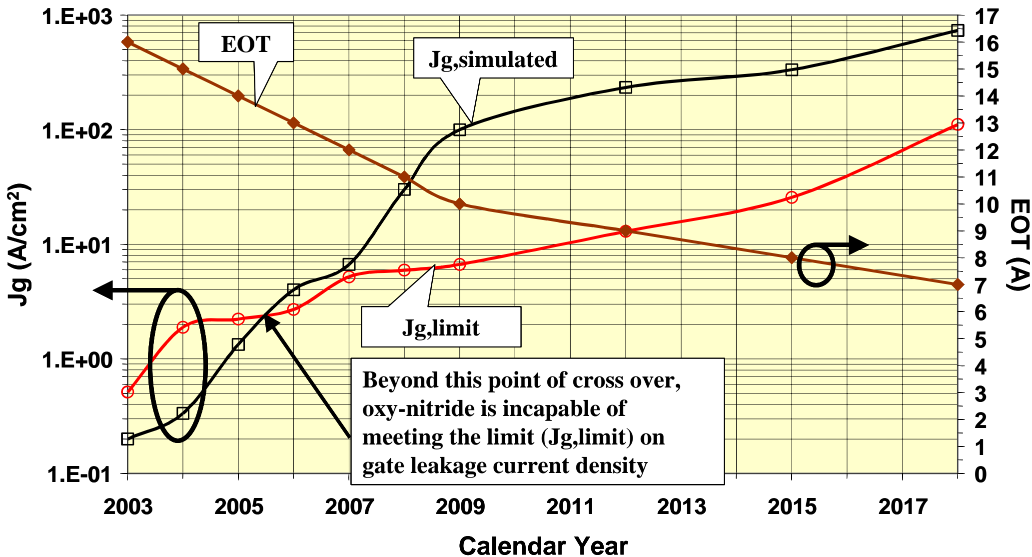


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

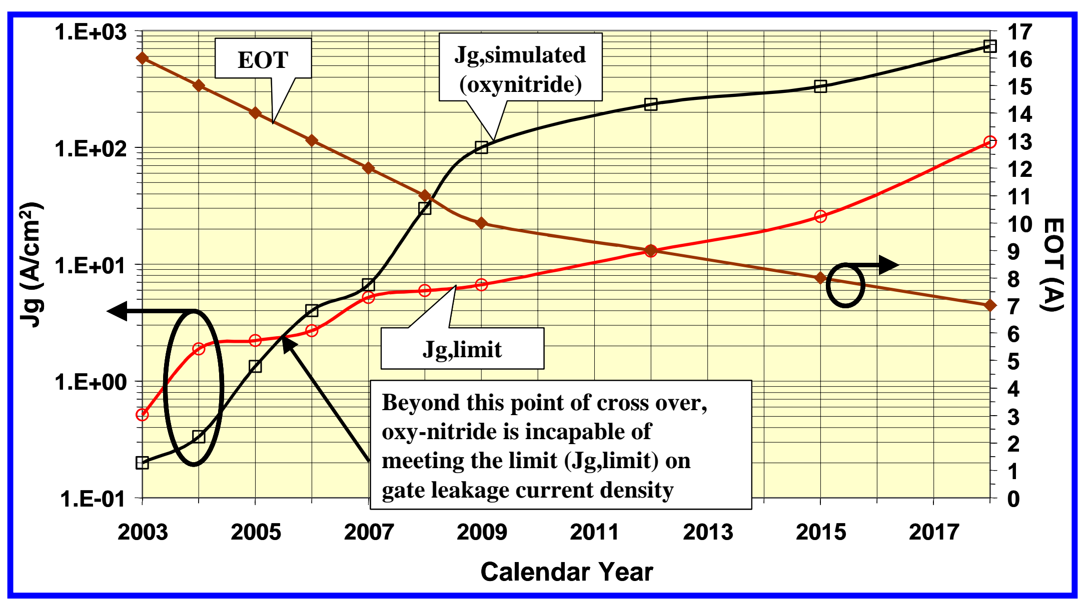


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

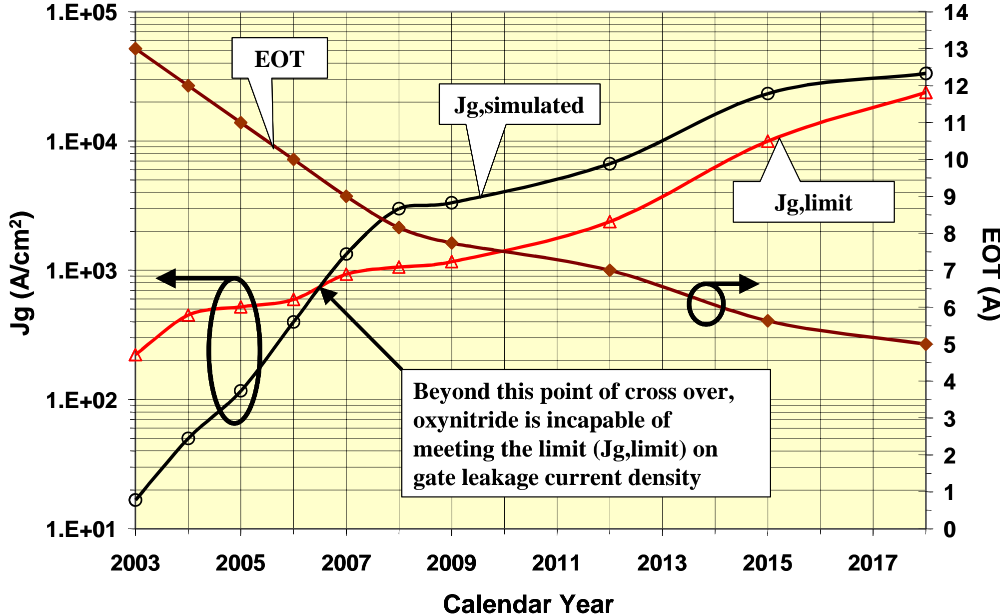


Figure 25 High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

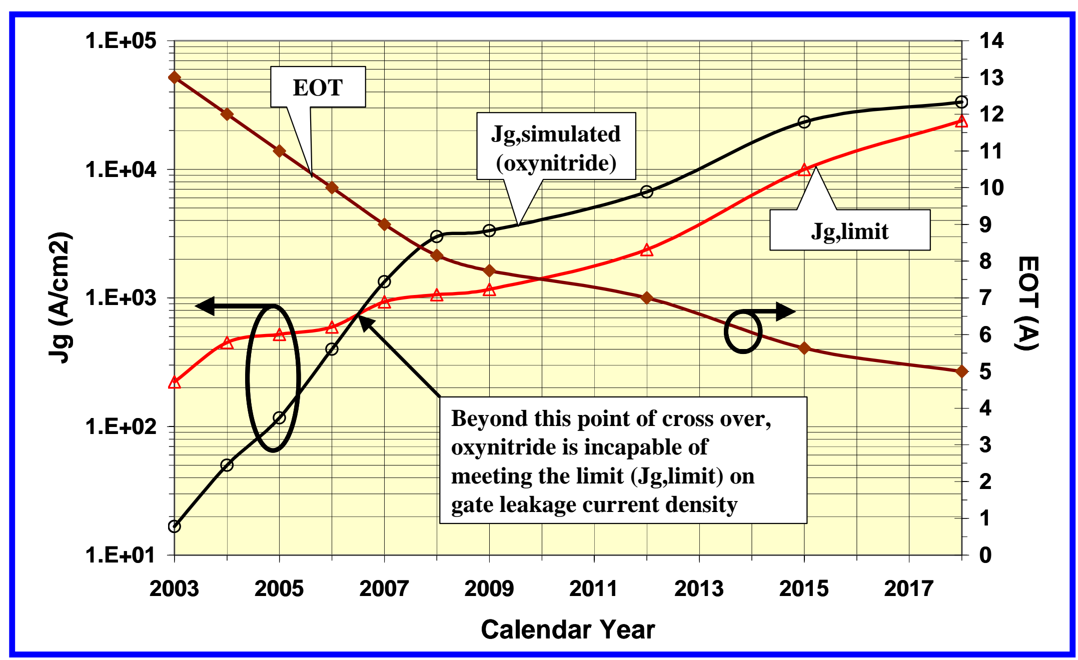


Figure 25 High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

Table 47a High-performance Logic Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Physical gate length high-performance (HP) (nm) [1]	**45**	**37**	**32**	**28**	**25**	**22**	**20**
EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	**1.3**	**1.2**	**1.1**	**1.0**	**0.9**	**0.8**	**0.8**
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	**0.8**	**0.8**	**0.7**	**0.7**	**0.4**	**0.4**	**0.4**
Equivalent electrical oxide thickness in inversion (nm) [4]	**2.1**	**2.0**	**1.8**	**1.7**	**1.3**	**1.2**	**1.2**
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	**2.2E+02**	**4.5E+02**	**5.2E+02**	**6.0E+02**	**9.3E+02**	**1.1E+03**	**1.2E+03**
Nominal power supply voltage (V_{dd}) (V) [6]	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**	**1.0**	**1.0**
Saturation threshold voltage (V) [7]	**0.21**	**0.20**	**0.20**	**0.21**	**0.18**	**0.17**	**0.16**
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (µA/µm) [8]	**0.03**	**0.05**	**0.05**	**0.05**	**0.07**	**0.07**	**0.07**
Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (mA/mm) [9]	◆ **980**	**1110**	**1090**	**1170**	**1510**	**1530**	**1590**
Required "mobility/transconductance improvement" factor [10]	**1.0**	**1.3**	**1.3**	**1.4**	**2.0**	**2.0**	**2.0**
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**0.8**	**0.7**
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	◆ **180**	**180**	**180**	**171**	**162**	**153**	**144**
Ideal NMOS device gate capacitance (F/µm) [14]	**7.40E-16**	**6.39E-16**	**6.14E-16**	**5.69E-16**	**6.64E-16**	**6.33E-16**	**5.76E-16**
Parasitic fringe/overlap capacitance (F/µm) [15]	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.30E-16**	**2.20E-16**	**2.00E-16**	**1.90E-16**
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	◆ **1.20**	**0.95**	**0.86**	**0.75**	**0.64**	**0.54**	**0.48**
Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	◆ **1.00**	**1.26**	**1.39**	**1.60**	**1.86**	**2.20**	**2.49**
Nominal logic gate delay (NAND Gate) (ps) [18]	◆ **30.24**	**23.94**	**21.72**	**18.92**	**16.23**	**13.72**	**12.13**
NMOSFET power-delay product (J/µm) [19]	**1.41E-15**	**1.27E-15**	**1.03E-15**	**9.66E-16**	**1.07E-15**	**8.33E-16**	**7.66E-16**
NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	**3.96E-07**	**6.60E-07**	**6.05E-07**	**6.05E-07**	**8.47E-07**	**7.70E-07**	**7.70E-07**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

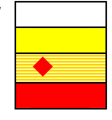


Table 47b High-performance Logic Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length high-performance (HP) (nm) [1]	18		14	13		10	9		7
IS	Physical gate length high-performance (HP) (nm) [1]	18	16	14	13	11	10	9	8	7
WAS	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7		0.7	0.6		0.6	0.5		0.5
IS	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4		0.4	0.4		0.4	0.4		0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.1		1.1	1		1	0.9		0.9
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.1	1.1	1.1	1	1	1	0.9	0.9	0.9
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	1.90E+03		2.40E+03	7.70E+03		1.00E+04	1.90E+04		2.40E+04
IS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	1.90E+03	2.08E+03	2.40E+03	7.70E+03	9.09E+03	1.00E+04	1.90E+04	2.08E+04	2.40E+04
WAS	Nominal power supply voltage (V_{dd}) (V) [6]	1		0.9	0.9		0.8	0.8		0.7
IS	Nominal power supply voltage (V_{dd}) (V) [6]	1	1	0.9	0.9	0.9	0.8	0.8	0.7	0.7
WAS	Saturation threshold voltage (V) [7]	0.15		0.14	0.11		0.12	0.1		0.11
IS	Saturation threshold voltage (V) [7]	0.15	0.15	0.14	0.11	0.11	0.12	0.1	0.1	0.11
WAS	Nominal high-performance NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	0.1		0.1	0.3		0.3	0.5		0.5
IS	Nominal high-performance NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	0.1	0.1	0.1	0.3	0.3	0.3	0.5	0.5	0.5

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

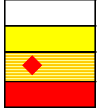


Table 47b High-performance Logic Technology Requirements—Long-term UPDATED (continued)

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
	DRAM ½ Pitch (nm)	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at Vdd, at 25°C) (mA/µm) [9]*	1900		1790	2050		2110	2400		2190
IS	*Nominal high-performance NMOS saturation drive current, Id,sat (at Vdd, at 25°C) (µA/µm) [9]*	1900	1940	1790	2050	2230	2110	2400	2120	2190
WAS	*Required "mobility/transconductance improvement" factor [10]*	2		2	2		2	2		2
IS	*Required "mobility/transconductance improvement" factor [10]*	2	2	2	2	2	2	2	2	2
WAS	*Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]*	0.6		0.5	0.5		0.5	0.5		0.5
IS	*Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]*	0.6	0.6	0.5	0.5	0.5	0.5	0.5	0.5	0.5
WAS	*Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]*	1.1		1.1	1.1		1.3	1.3		1.3
IS	*Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]*	1.1	1.1	1.1	1.1	1.2	1.3	1.3	1.3	1.3
WAS	*Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]*	135		116	107		88	79		60
IS	*Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]*	135	125	116	107	98	88	79	70	60
WAS	*Ideal NMOS device gate capacitance (F/µm) [14]*	5.65E-16		4.39E-16	4.49E-16		3.45E-16	3.45E-16		2.69E-16
IS	*Ideal NMOS device gate capacitance (F/µm) [14]*	5.65E-16	5.02E-16	4.39E-16	4.49E-16	3.76E-16	3.45E-16	3.45E-16	3.07E-16	2.69E-16
WAS	*Parasitic fringe/overlap capacitance (F/µm) [15]*	1.80E-16		1.50E-16	1.40E-16		1.20E-16	1.00E-16		8.00E-17
IS	*Parasitic fringe/overlap capacitance (F/µm) [15]*	1.80E-16	1.65E-16	1.50E-16	1.40E-16	1.30E-16	1.20E-16	1.00E-16	9.00E-17	8.00E-17
WAS	*High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]*	0.39		0.3	0.26		0.18	0.15		0.11
IS	*High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]*	0.39	0.34	0.3	0.26	0.21	0.18	0.15	0.13	0.11

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 47b High-performance Logic Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.06		4.05	4.64		6.8	8.08		10.77
IS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.1	3.5	4.1	4.6	5.7	6.8	8.1	9.2	10.8
WAS	Nominal logic gate delay (NAND gate) (ps) [18]	9.88		7.47	6.52		4.45	3.74		2.81
IS	Nominal logic gate delay (NAND gate) (ps) [18]	9.88	8.67	7.47	6.52	5.19	4.45	3.74	3.30	2.81
WAS	NMOSFET power-delay product (J/µm) [19]	7.45E-16		4.77E-16	4.77E-16		2.98E-16	2.85E-16		1.71E-16
IS	NMOSFET power-delay product (J/µm) [19]	7.45E-16	6.67E-16	4.77E-16	4.77E-16	4.10E-16	2.98E-16	2.85E-16	1.95E-16	1.71E-16
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	1.10E-06		9.90E-07	2.97E-06		2.64E-06	4.40E-06		3.85E-06
IS	NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	1.1E-06	1.1E-06	9.9E-07	3.0E-06	3.0E-06	2.6E-06	4.4E-06	3.9E-06	3.9E-06

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 47a and 47b:

A Microsoft Excel file containing the worksheet in which the details of the model-based scaling are described is located in the electronic version of this chapter at http://public.itrs.net, including the formulas used in the MOSFET modeling. All the entries in this High-performance Logic Technology Requirements Table are from the worksheet. Please refer to this Excel file for detailed questions about the table.

WAS *The scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed (see Note [16]), while delaying as long as feasible the projected need for major innovations. These include innovations such as metal gate electrode, high-κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters (see text for more detail on this point).*

IS *The scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed (see Note [~~16~~ 17]), while delaying as long as feasible the projected need for major innovations. These include innovations such as metal gate electrode, high-κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters (see text for more detail on this point).*

[1] This is the final, as-etched length of the bottom of the gate electrode. Values set by ORTC. Gate dimensional control is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of ± 10% × L_g. It is expected that meeting this 10% requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation.

[2] For a gate dielectric of thickness T_d and relative dielectric constant κ, EOT is defined by: EOT = T_d / (κ/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d, the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. Yellow coloring in 2006 is set by FEP TWG projections of difficulties in achieving adequate thickness control and reliability capability for thin silicon oxy-nitride gate dielectrics. Red coloring for 2007 and beyond is due to projected inability of oxy-nitride gate dielectric to meet the gate leakage current density limits (see Note [5], and see text as well as Figure 25 for detail). Utilization of high-κ gate dielectric is a potential solution. Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.

[3] Accounts (approximately) for gate electrode depletion and inversion-layer effects, including quantum effects. The portion of the electrical thickness adjustment due to inversion-layer effects is assumed to remain constant at 0.4 nm. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. The yellow coloring for 2005 and 2006 reflects the FEP TWG assessment of difficulty in adequately doping polysilicon (particularly

for the P^+, boron-doped electrodes) to meet the gate depletion thickness adjustment requirements. The red coloring for 2007 and beyond reflects the projected inability to adequately dope polysilicon gate electrodes to meet the gate depletion thickness adjustment requirements. Introduction of metal-gate electrodes, which reduce the gate depletion effect to zero, is a potential solution.

[4] Sum of EOT and electrical thickness adjustment (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [14]) is ε_{ox} / (equivalent electrical oxide thickness), where ε_{ox} is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the CV/I intrinsic delay (see Note [16]) and of the CV^2 dynamic switching energy (see Note [19]). Red/yellow coloring follows that of EOT and Electrical Thickness Adjustment (see Notes [2] and [3] above).

[5] This is the maximum allowed gate leakage at 25°C, and is related to $I_{sd,leak}$, the nominal subthreshold leakage current per micron device width (see Note [8] below). Specifically, gate leakage current density limit = [$I_{sd,leak}$ / (physical gate length)] × [temp. factor] / [stack and overlap factor]. "Temp factor" = 10, and it accounts for the high operating temperature expected for high-performance logic, by adjusting for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. Stack and overlap factor=3, and accounts for the different effects on $I_{sd,leak}$ and gate leakage current of stacked transistors in logic gates and of transistor gate overlap. The values of both temp factor and stack and overlap factor are rough order of magnitude estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] Nominal power supply voltage has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note 7)] in order to meet the required saturation current drive values (see Note 9), while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary ± 10% (or more) from the values in this table, depending on the particular circuit design application or technology optimization.

[7] Calculated threshold voltage for minimum nominal gate length transistor with drain bias set equal to V_{dd} (see Note [6]). The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). Since control of short-channel effects for scaled MOSFETs is a key issue here, the yellow/red coloring follows that of the subthreshold slope adjustment factor (see Note [11] below).

[8] Nominal subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} (see Note [6]) and with the gate, source, and substrate biases set to zero volts. All MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current components. The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between $I_{sd,leak}$ and gate leakage current density. Yellow and red coloring follows that of the subthreshold slope adjustment factor, which takes account of the impact of using advanced devices: ultra-thin body, fully depleted MOSFETs and multiple-gate MOSFETs (see Note [11] below). The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices. Note that subthreshold current values here apply to the fastest MOSFETs only; slower/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

WAS

[9] Nominal saturation current drive, $I_{d,sat}$, is defined as the NMOSFET drain current per micron device width, at 25°C, with the gate bias and the drain bias set equal to V_{dd} (see Note [6]) and the source and substrate biases set to zero; all MOSFET device dimensions are assumed to be at their nominal/target values. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note [17] below). Nominal PMOS saturation current-drive value is assumed to be (40–50)% of the nominal NMOS saturation current-drive value. Yellow/red coloring follows that of three items: the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), and the required mobility/transconductance improvement factor (see Note [10]). Note that saturation current drive values here apply to the fastest MOSFETs only; lower saturation current drive/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

IS

[9] Nominal saturation current drive, $I_{d,sat}$, is defined as the NMOSFET drain current per micron device width, at 25°C, with the gate bias and the drain bias set equal to V_{dd} (see Note [6]) and the source and substrate biases set to zero; all MOSFET device dimensions are assumed to be at their nominal/target values. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note [17] below). Nominal PMOS saturation current-drive value is assumed to be (40–50)% of the nominal NMOS saturation current-drive value. Yellow/red ***and striped*** *coloring follows that of three items: the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), and the required mobility/transconductance improvement factor (see Note [10]). Note that saturation current drive values here apply to the fastest MOSFETs only; lower saturation current drive/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).*

[10] Fundamental device mobility/transconductance improvement (strained Si channel is the current implementation choice) is captured by a factor multiplying the carrier mobility. Such improvement is projected to be needed by 2004 in order to meet the required saturation current drive values (see Note [9]). Yellow coloring in 2004 and beyond reflects projected implementation of strained Si channel devices. Red coloring in 2007 and beyond reflects the difficulty in optimizing this mobility enhancement to a factor of 2.0, and the difficulty of implementing enhanced mobility channels for advanced, ultra-thin body devices.

[11] Subthreshold slope adjustment factor takes account of the impact of using advanced, single-gate, ultra-thin body, fully depleted SOI MOSFETs and eventually, ultra-thin body, multiple-gate MOSFETs, which are needed to control short-channel effects for highly scaled transistors. Specifically, this is a multiplying factor for the subthreshold slope, reducing it towards its minimum ideal value of 60 mV/decade. The factor ranges from 1.0 for classical, planar bulk MOSFETs, to 0.7 to 0.8 for single-gate, ultra-thin body MOSFETs, to 0.6 to 0.5 for ultra-thin body, multiple-gate MOSFETs. These numbers are rough estimates of the impact of these advanced devices. (See Non-Classical CMOS tables in the Emerging Research Devices section for further discussion of the ultra-thin body MOSFETs.) The yellow coloring reflects the projected introduction of the single-gate, ultra-thin body MOSFET in 2008, and the red coloring reflects the projected introduction of the multiple-gate MOSFET in 2010.

[12] This is a multiplying factor for carrier saturation velocity, reflecting quasi-ballistic transport in highly scaled, ultra-thin body MOSFETs, particularly multi-gate MOSFETs. The red coloring in 2010 and beyond reflects the projected need for saturation velocity enhancement in order to meet the required saturation current drive values (see Note [9]).

WAS *[13] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.*

IS *[13] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red **and striped** coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.*

[14] This is $C_{g,ideal}$, the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal} = [\varepsilon_{ox}/(EOT_{inv})] \times L_g$, where ε_{ox} is the dielectric constant of thermal silicon dioxide, EOT_{inv} is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red/yellow coloring follows that of EOT_{inv} (see Note [4]).

[15] This is the parasitic gate overlap/fringing capacitance per micron device width [3× the overlap/fringing capacitance value per side, including the Miller effect]. These values are assumed to be independent of bias conditions.

WAS *[16] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{gate} \times V_{dd}) / I_{d,sat}$, where C_{gate} is the sum of the ideal device gate capacitance per micron device width (Note 14) and the parasitic gate overlap/fringing capacitance per micron device width (see Note [15]). τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat}$ ~ (0.4–0.5) × (NMOS $I_{d,sat}$) (see Note [9]). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow coloring follows that of both saturation current-drive (see Note [9]) and ideal gate capacitance (see Note [14]).*

IS *[16] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{gate} \times V_{dd}) / I_{d,sat}$, where C_{gate} is the sum of the ideal device gate capacitance per micron device width (Note 14) and the parasitic gate overlap/fringing capacitance per micron device width (see Note [15]). τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat}$ ~ (0.4–0.5) × (NMOS $I_{d,sat}$) (see Note [9]). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow **and striped** coloring follows that of both saturation current-drive (see Note [9]) and ideal gate capacitance (see Note [14]).*

WAS *[17] NMOS performance metric ($1/\tau$, NMOS intrinsic switching speed--see Note [16]), normalized to the year 2003. Maintenance of the historical approximate 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red/yellow coloring follows that of τ (see Note [16]).*

IS *[17] NMOS performance metric ($1/\tau$, NMOS intrinsic switching speed--see Note [16]), normalized to the year 2003. Maintenance of the historical approximate 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red/yellow **and striped** coloring follows that of τ (see Note [16]).*

WAS *[18] This is the calculated nominal delay for a 2-input, fan-out of 3, NAND gate, which is chosen to represent a typical logic gate (for details of the calculation, see link provided in the electronic version, online at http://public.itrs.net.). Red/yellow coloring follows that of τ (see Note [16]).*

IS *[18] This is the calculated nominal delay for a 2-input, fan-out of 3, NAND gate, which is chosen to represent a typical logic gate (for details of the calculation, see link provided in the electronic version, online at http://public.itrs.net.). Red/yellow **and striped** coloring follows that of τ (see Note [16]).*

[19] This is the energy dissipated per micron of MOSFET width during a full switching cycle, defined as $C_{gate} \times V_{dd}^2$, where C_{gate} is the sum of the ideal device gate capacitance per micron width (Note [14]) and the parasitic gate overlap/fringing capacitance per micron width (see Note [15]). (This is the same C_{gate} used in calculating τ [see Note [16]). The dynamic power dissipation is directly related to this power-delay product. Red/yellow coloring follows that of $C_{g,ideal}$ (see Note [14]).

[20] This is the static power dissipation per micron of MOSFET width, defined as $V_{dd} \times [\{I_{sd,leak}$ (see Note 8)} + { maximum gate leakage current per micron device width (defined as L_g × gate leakage current density limit, from Note 5)}]. (The junction leakage current is assumed to be much smaller than either the source/drain subthreshold leakage current or the gate leakage current). Yellow/red coloring follows that of nominal gate leakage current density limit (see Note [5]).

Table 48a Low Operating Power (LOP) Logic Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Physical gate length low operating power (LOP) (nm) [1]	**65**	**53**	**45**	**37**	**32**	**28**	**25**
EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	**1.6**	**1.5**	**1.4**	**1.3**	**1.2**	**1.1**	**1.0**
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.4**	**0.4**
Equivalent electrical oxide thickness in inversion (nm) [4]	**2.4**	**2.3**	**2.1**	**2.0**	**1.9**	**1.5**	**1.4**
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	**0.51**	**1.89**	**2.22**	**2.70**	**5.21**	**5.95**	**6.67**
Nominal LOP power supply voltage (V_{dd}) (V) [6]	**1.0**	**0.9**	**0.9**	**0.9**	**0.8**	**0.8**	**0.8**
Saturation threshold voltage (V) [7]	**0.31**	**0.26**	**0.27**	**0.28**	**0.26**	**0.25**	**0.25**
Nominal LOP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (μA/μm) [8]	**1.0E-03**	**3.0E-03**	**3.0E-03**	**3.0E-03**	**5.0E-03**	**5.0E-03**	**5.0E-03**
Nominal LOP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (μA/μm) [9]	**520**	**530**	**580**	**610**	**570**	**730**	**770**
Required "mobility/transconductance improvement" factor [10]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.3**	**1.3**
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	**180**	**180**	**180**	**180**	**180**	**180**	**180**
Ideal NMOS device gate capacitance (F/μm) [14]	**9.35E-16**	**7.96E-16**	**7.40E-16**	**6.39E-16**	**5.82E-16**	**6.45E-16**	**6.17E-16**
Parasitic fringe/overlap capacitance (F/μm) [15]	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**
LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	**2.26**	**1.76**	**1.52**	**1.30**	**1.15**	**0.97**	**0.89**
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	**1.00**	**1.29**	**1.49**	**1.74**	**1.96**	**2.33**	**2.54**
Nominal logic gate delay (NAND gate) (ps) [18]	**57.0**	**44.3**	**38.3**	**32.7**	**29.1**	**24.4**	**22.4**
NMOSFET power-delay product (J/μm) [19]	**1.18E-15**	**8.39E-16**	**7.94E-16**	**7.12E-16**	**5.26E-16**	**5.66E-16**	**5.48E-16**
NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	**2.0E-09**	**5.4E-09**	**5.4E-09**	**5.4E-09**	**8.0E-09**	**8.0E-09**	**8.0E-09**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 48b Low Operating Power (LOP) Logic Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length low operating power (LOP) (nm) [1]	22		18	16		13	11		9
IS	Physical gate length low operating power (LOP) (nm) [1]	22	20	18	16	14	13	11	10	9
WAS	EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	0.9	-	0.9	0.8	-	0.8	0.7	-	0.7
IS	EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	0.9	0.9	0.9	0.8	0.8	0.8	0.7	0.7	0.7
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	-	0.4	0.4	-	0.4	0.4	-	0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.3	-	1.3	1.2	-	1.2	1.1	-	1.1
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.3	1.3	1.3	1.2	1.2	1.2	1.1	1.1	1.1
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	11	-	13	21	-	26	91	-	111
IS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	11	12	13	21	24	26	91	100	111
WAS	Nominal LOP power supply voltage (V_{dd}) (V) [6]	0.7	-	0.7	0.6	-	0.6	0.5	-	0.5
IS	Nominal LOP power supply voltage (V_{dd}) (V) [6]	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
WAS	Saturation threshold voltage (V) [7]	0.22	-	0.23	0.21	-	0.19	0.16	-	0.17
IS	Saturation threshold voltage (V) [7]	0.22	0.22	0.23	0.21	0.2	0.19	0.16	0.16	0.17
WAS	Nominal LOP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (μA/μm) [8]	0.007	-	0.007	0.01	-	0.01	0.03	-	0.03
IS	Nominal LOP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (μA/μm) [8]	0.007	0.007	0.007	0.01	0.01	0.01	0.03	0.03	0.03
WAS	Nominal LOP NMOS saturation drive current, Id,sat (at V_{dd}, at 25°C) (μA/μm) [9]	770	-	830	780	-	900	920	-	950
IS	Nominal LOP NMOS saturation drive current, Id,sat (at V_{dd}, at 25°C) (μA/μm) [9]	770	800	830	780	840	900	920	935	950

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

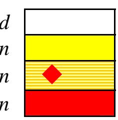


Table 48b Low Operating Power (LOP) Logic Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Required "mobility/transconductance improvement" factor [10]	1.3	-	2	2	-	2	2	-	2
IS	Required "mobility/transconductance improvement" factor [10]	1.3	1.3	2	2	2	2	2	2	2
WAS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	-	0.8	0.8	-	0.5	0.5	-	0.5
IS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	0.8	0.8	0.8	0.8	0.5	0.5	0.5	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	-	1	1.1	-	1.1	1.3	-	1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	1	1	1.1	1.1	1.1	1.3	1.3	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	160	-	135	126	-	107	98	-	80
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	160	148	135	126	117	107	98	89	80
WAS	Ideal NMOS device gate capacitance (F/μm) [14]	5.84E-16	-	4.78E-16	4.60E-16	-	3.74E-16	3.45E-16	-	2.83E-16
IS	Ideal NMOS device gate capacitance (F/μm) [14]	5.84E-16	5.31E-16	4.78E-16	4.60E-16	4.03E-16	3.74E-16	3.45E-16	3.14E-16	2.83E-16
WAS	Parasitic fringe/overlap capacitance (F/μm) [15]	2.20E-16	-	1.80E-16	1.60E-16	-	1.40E-16	1.30E-16	-	1.10E-16
IS	Parasitic fringe/overlap capacitance (F/μm) [15]	2.20E-16	2.00E-16	1.80E-16	1.60E-16	1.50E-16	1.40E-16	1.30E-16	1.20E-16	1.10E-16
WAS	LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.73	-	0.56	0.48	-	0.34	0.26	-	0.21
IS	LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.73	0.64	0.56	0.48	0.39	0.34	0.26	0.23	0.21
WAS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.1	-	4.1	4.7	-	6.6	8.7	-	10.9
IS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.1	3.54	4.1	4.7	5.72	6.6	8.7	9.75	10.9
WAS	Nominal logic gate delay (NAND Gate) (ps) [18]	18.4	-	14	12	-	8.6	6.5	-	5.2
IS	Nominal logic gate delay (NAND Gate) (ps) [18]	18.4	16.1	14	12	9.9	8.6	6.5	5.8	5.2
WAS	NMOSFET power-delay product (J/μm) [19]	3.94E-16	-	3.22E-16	2.23E-16	-	1.85E-16	1.19E-16	-	9.81E-17
IS	NMOSFET power-delay product (J/μm) [19]	3.94E-16	3.58E-16	3.22E-16	2.23E-16	1.99E-16	1.85E-16	1.19E-16	1.08E-16	9.81E-17
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	9.80E-09	-	9.80E-09	1.20E-08	-	1.20E-08	3.00E-08	-	3.00E-08
IS	NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	9.80E-09	9.80E-09	9.80E-09	1.20E-08	1.20E-08	1.20E-08	3.00E-08	3.00E-08	3.00E-08

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 48c Low Standby Power (LSTP) Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Physical gate length low standby power (LSTP) (nm) [1]	**75**	**65**	**53**	**45**	**37**	**32**	**28**
EOT: equivalent oxide thickness (physical) for LSTP (nm) [2]	**2.2**	**2.1**	**2.1**	**1.9**	**1.6**	**1.5**	**1.4**
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.4**	**0.4**
Equivalent electrical oxide thickness in inversion (nm) [4]	**3**	**2.9**	**2.8**	**2.6**	**2.3**	**1.9**	**1.8**
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	**4.4E-03**	**5.1E-03**	**9.4E-03**	**1.5E-02**	**2.3E-02**	**3.1E-02**	**4.8E-02**
Nominal LSTP power supply voltage (V_{dd}) (V) [6]	**1.2**	**1.2**	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**
Saturation threshold voltage (V) [7]	**0.50**	**0.50**	**0.51**	**0.52**	**0.50**	**0.47**	**0.47**
Nominal LSTP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (µA/µm) [8]	**1.0E-05**	**1.0E-05**	**1.5E-05**	**2.0E-05**	**2.5E-05**	**3.0E-05**	**4.0E-05**
Nominal LSTP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (µA/µm) [9]	**410**	**440**	**470**	**510**	**510**	**670**	**700**
Required "mobility/transconductance improvement" factor [10]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.3**	**1.3**
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	**180**	**180**	**180**	**180**	**180**	**180**	**180**
Ideal NMOS device gate capacitance (F/µm) [14]	**8.63E-16**	**7.74E-16**	**6.54E-16**	**5.98E-16**	**5.55E-16**	**5.82E-16**	**5.37E-16**
Parasitic fringe/overlap capacitance (F/µm) [15]	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**
LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	**3.23**	**2.77**	**2.28**	**1.97**	**1.72**	**1.35**	**1.22**
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	**1.00**	**1.17**	**1.42**	**1.64**	**1.88**	**2.39**	**2.64**
Nominal logic gate delay (NAND Gate) (ps) [18]	**81.4**	**69.7**	**57.5**	**49.7**	**43.2**	**34.0**	**30.8**
NMOSFET power-delay product (J/µm) [19]	**1.6E-15**	**1.5E-15**	**1.3E-15**	**1.2E-15**	**9.6E-16**	**9.9E-16**	**9.4E-16**
NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	**2.4E-11**	**2.4E-11**	**3.6E-11**	**4.8E-11**	**5.5E-11**	**6.6E-11**	**8.8E-11**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

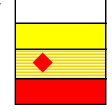


Table 48d Low Standby Power (LSTP) Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length low standby power (LSTP) (nm) [1]	25		20	18		14	13		10
IS	Physical gate length low standby power (LSTP) (nm) [1]	25	23	20	18	16	14	13	12	10
WAS	EOT: equivalent oxide thickness (physical) for LSTP (nm) [2]	1.3		1.2	1.1		1.1	1		0.9
IS	EOT: equivalent oxide thickness (physical) for LSTP (nm) [2]	1.3	1.3	1.2	1.1	1.1	1.1	1	1	0.9
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4		0.4	0.4		0.4	0.4		0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.7		1.6	1.5		1.5	1.4		1.3
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.7	1.7	1.6	1.5	1.5	1.5	1.4	1.4	1.3
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	8.00E-02		1.00E-01	1.48E-01		1.90E-01	2.56E-01		3.33E-01
IS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	0.08	0.09	0.10	0.15	0.17	0.19	0.26	0.28	0.33
WAS	Nominal LSTP power supply voltage (V_{dd}) (V) [6]	1		1	0.9		0.9	0.8		0.8
IS	Nominal LSTP power supply voltage (V_{dd}) (V) [6]	1	1	1	0.9	0.9	0.9	0.8	0.8	0.8
WAS	Saturation threshold voltage (V) [7]	0.39		0.43	0.34		0.38	0.36		0.4
IS	Saturation threshold voltage (V) [7]	0.39	0.42	0.43	0.34	0.36	0.38	0.36	0.39	0.4
WAS	Nominal LSTP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (μA/μm) [8]	6.00E-05		6.00E-05	8.00E-05		8.00E-05	1.00E-04		1.00E-04
IS	Nominal LSTP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (μA/μm) [8]	6.00E-05	6.00E-05	6.00E-05	8.00E-05	8.00E-05	8.00E-05	1.00E-04	1.00E-04	1.00E-04
WAS	Nominal LSTP NMOS saturation drive current, Id,sat (at V_{dd}, at 25°C) (μA/μm) [9]	760		790	880		870	860		990
IS	Nominal LSTP NMOS saturation drive current, Id,sat (at V_{dd}, at 25°C) (μA/μm) [9]	760	750	790	880	870	870	860	880	990

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 48d Low Standby Power (LSTP) Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Required "mobility/transconductance improvement" factor [10]	1.3		1.3	1.3		1.3	2		2
IS	Required "mobility/transconductance improvement" factor [10]	1.3	1.3	1.3	1.3	1.3	1.3	2	2	2
WAS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8		0.8	0.5		0.5	0.5		0.5
IS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	0.8	0.8	0.5	0.5	0.5	0.5	0.5	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1		1	1		1	1.1		1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	1	1	1	1	1	1.1	1.2	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	180		144	135		116	107		88
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	180	160	144	135	125	116	107	97	88
WAS	Ideal NMOS device gate capacitance (F/μm) [14]	5.08E-16		4.32E-16	4.14E-16		3.22E-16	3.21E-16		2.66E-16
IS	Ideal NMOS device gate capacitance (F/μm) [14]	5.08E-16	4.67E-16	4.32E-16	4.14E-16	3.68E-16	3.22E-16	3.21E-16	2.96E-16	2.66E-16
WAS	Parasitic fringe/overlap capacitance (F/μm) [15]	2.40E-16		1.90E-16	1.70E-16		1.50E-16	1.40E-16		1.20E-16
IS	Parasitic fringe/overlap capacitance (F/μm) [15]	2.40E-16	2.15E-16	1.90E-16	1.70E-16	1.60E-16	1.50E-16	1.40E-16	1.30E-16	1.20E-16
WAS	LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.98		0.79	0.6		0.49	0.43		0.31
IS	LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.98	0.90	0.79	0.6	0.55	0.49	0.43	0.39	0.31
WAS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.28		4.1	5.4		6.61	7.54		10.36
IS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.28	3.58	4.1	5.4	5.91	6.61	7.54	8.34	10.36
WAS	Nominal logic gate delay (NAND gate) (ps) [18]	24.8		19.83	15.06		12.31	10.8		7.85
IS	Nominal logic gate delay (NAND gate) (ps) [18]	24.8	22.78	19.83	15.06	13.71	12.31	10.8	9.73	7.85
WAS	NMOSFET power-delay product (J/μm) [19]	7.48E-16		6.22E-16	4.73E-16		3.83E-16	2.95E-16		2.47E-16
IS	NMOSFET power-delay product (J/μm) [19]	7.48E-16	6.82E-16	6.22E-16	4.73E-16	4.28E-16	3.83E-16	2.95E-16	2.73E-16	2.47E-16
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	1.20E-10		1.20E-10	1.44E-10		1.44E-10	1.60E-10		1.60E-10
IS	NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	1.20E-10	1.20E-10	1.20E-10	1.44E-10	1.44E-10	1.44E-10	1.60E-10	1.60E-10	1.60E-10

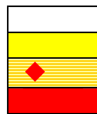
Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known

Manufacturable solutions are NOT known

Table 49a DRAM Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm) [1]	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm)	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
DRAM cell size (μm^2) [2]	**0.082**	**0.065**	**0.048**	**0.036**	**0.028**	**0.019**	**0.015**
DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	**3.5**	**2.3**	**1.8**	**1.3**	**0.8**	**0.8**	**0.8**
Minimum DRAM retention time (ms) [4]	**64**	**64**	**64**	**64**	**64**	**64**	**64**
DRAM soft error rate (FITs) [5]	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**

Table 49b DRAM Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm) [1]	45		35	32		25	22		18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	DRAM cell size (μm^2) [2]	**0.0122**		**0.0077**	**0.0061**		**0.0038**	**0.0025**		**0.0016**
IS	DRAM cell size (μm^2) [2]	**0.0122**	**0.0096**	**0.0077**	**0.0061**	**0.0048**	**0.0038**	**0.0025**	**0.0020**	**0.0016**
WAS	DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	**0.70**		**0.58**	**0.53**		**0.42**	**0.37**		**0.25**
IS	DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	**0.70**	**0.64**	**0.58**	**0.53**	**0.48**	**0.42**	**0.37**	**0.31**	**0.25**
WAS	Minimum DRAM retention time (ms) [4]	**64**		**64**	**64**		**64**	**64**		**64**
IS	Minimum DRAM retention time (ms) [4]	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**
WAS	DRAM soft error rate (FITs) [5]	**1000**		**1000**	**1000**		**1000**	**1000**		**1000**
IS	DRAM soft error rate (FITs) [5]	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 49a and 49b:

[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are the same as those in the 2002 ITRS due to no further speed up in the pace of DRAM half pitch scaling during 2002 and the early part of 2003.

[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC Tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F^2). and F is the DRAM half pitch. The required values of "a" are 8 for the 90 nm node, real 6 for the 55 nm DRAM half pitch in 2008, and 5 (need $4F^2$ layout) for the 32 nm node. The reason for the introduction delay of "a" value of 6 is due to no clear solutions, as illustrated with yellow zone in this line. The "a" value of 5 has no known solution for 32 nm node and beyond, as illustrated with red zone.

[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. Up to the 90 nm nodes, the dielectric material is based on Al_2O_3 or Ta_2O_5 with MIS structure, and hence the color is white. Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65 nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.

[4] Retention time is defined at 85ºC, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

[5] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
WAS	Flash technology node – F (nm) [1]	107	90	80	70	65	55	50
IS	Flash technology node – F (nm) [1]	107	90	80	70	65	57	50
	Flash NOR cell size – area factor a in multiples of F^2 [2]	10–12	11–14	11–14	11–14	11–14	12–14	12–15
	Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [3]	5.5	5.5	5.5	5.5	4.5	4.5	4.5
WAS	Flash NOR typical cell size (μm^2) [4]	0.135	0.101	0.08	0.061	0.053	0.039	0.034
IS	Flash NOR typical cell size (μm^2) [4]	0.135	0.101	0.08	0.061	0.053	0.042	0.034
	Flash NOR L_g-stack (physical – μm) [5]	0.22–0.24	0.2–0.22	0.2–0.22	0.19–0.21	0.19–0.21	0.18–0.20	0.18–0.20
	Flash NOR highest W/E voltage (V) [6]	8–10	7–9	7–9	7–9	7–9	7–9	7–9
	Flash NAND highest W/E voltage (V) [7]	18–20	17–19	17–19	17–19	15–17	15–17	15–17
	Flash NOR I_{read} (μA) [8]	34–42	31–39	29–37	28–36	27–35	26–34	25–33
	Flash coupling ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
WAS	Flash NOR tunnel oxide thickness (nm) [10]	9–10	8.5–9.5	8.5–9.5	8.5–9.5	8–9	8–9	8–9
IS	Flash NOR tunnel oxide thickness EOT (nm) [10]	9–10	8.5–9.5	8.5–9.5	8-9	8–9	8–9	8–9
WAS	Flash NAND tunnel oxide thickness (nm) [11]	7–8	7–8	7–8	7–8	6–7	6–7	6–7
IS	Flash NAND tunnel oxide thickness EOT (nm) [11]	7–8	7–8	7–8	6–7	6–7	6–7	6–7
WAS	Flash NOR interpoly dielectric thickness (nm) [12]	11–13	10–12	9–11	9–11	8.5–10.5	8.5–10.5	8.5–10.5
IS	Flash NOR interpoly dielectric thickness EOT (nm) [12]	13-15	11-13	11-13	11-13	10-12	10-12	10-12
	Flash NAND interpoly dielectric thickness (nm) [13]	13–15	13–15	13–15	13–15	10–13	10–13	10–13
	Flash endurance (erase/write cycles) [14]	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05
	Flash nonvolatile data retention (years) [15]	10–20	10–20	10–20	10–20	10–20	10–20	10–20
	Flash maximum number of bits per cell (MLC) [16]	2	2	4	4	4	4	4

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

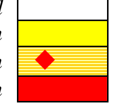


Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED (continued)

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
WAS	FeRAM technology node – F (nm) [17]	250	180	180	150	130	120	110
IS	FeRAM technology node – F (nm) [17]	250	180	130	130	120	110	110
WAS	FeRAM cell size – area factor a in multiples of F^2 [18]	24	16	12	12	12	10	10
IS	FeRAM cell size – area factor a in multiples of F^2 [18]	15	15	12	12	12	10	10
WAS	FeRAM cell size (μm^2) [19]	1.5	0.518	0.389	0.27	0.203	0.144	0.121
IS	FeRAM cell size (μm^2) [19]	0.937	0.486	0.203	0.203	0.173	0.121	0.121
WAS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
IS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
WAS	FeRAM capacitor structure [21]	stack	stack	stack	stack	3D	3D	3D
IS	FeRAM capacitor structure [21]	stack	stack	stack	stack	3D	3D	3D
WAS	FeRAM capacitor footprint (μm^2) [22]	0.5	0.26	0.13	0.09	0.07	0.06	0.05
IS	FeRAM capacitor footprint (μm^2) [22]	0.44	0.23	0.12	0.12	0.086	0.081	0.076
WAS	FeRAM capacitor active area (μm^2) [23]	0.5	0.26	0.13	0.09	0.09	0.09	0.08
IS	FeRAM capacitor active area (μm^2) [23]	0.44	0.23	0.12	0.12	0.058	0.048	0.04
WAS	FeRAM cap active area/footprint ratio [24]	1	1	1	1	1.29	1.5	1.6
IS	FeRAM cap active area/footprint ratio [24]	1	1	1	1	1.48	1.67	1.89
WAS	Ferro capacitor voltage (V) [25]	2.5	1.8	1.5	1.5	1.2	1.2	1.2
IS	Ferro capacitor voltage (V) [25]	2.5-3	1.8	1.5	1.5	1.2	1.2	1.2
WAS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	11.2	17.2	34.5	34.5	40	40	40
IS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	12.8	19.8	30.5	30.5	40	40	40
	FeRAM endurance (read/write cycles) [27]	1.00E+13	1.00E+14	1.00E+15	>1E16	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [28]	10	10	10	10	10	10	10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

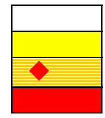


Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED (continued)

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
SONOS/NROM technology node – F (nm) [29]	**130**	**115**	**100**	**90**	**70**	**65**	**55**
SONOS/NROM cell size – area factor a in multiples of F^2 [30]	**5**	**5**	**5.5**	**5.5**	**6**	**6**	**6**
SONOS/NROM typical cell size (mm^2) [31]	**0.085**	**0.066**	**0.055**	**0.045**	**0.029**	**0.025**	**0.018**
SONOS/NROM maximum number of bits per cell (MLC) [32]	**2**	**2**	**2**	**2**	**2**	**2**	**2**
SONOS/NROM area per bit (mm^2) [33]	**0.042**	**0.033**	**0.028**	**0.022**	**0.015**	**0.013**	**0.009**
SONOS L_g-stack (physical – μm) [34]	**0.18**	**0.18**	**0.17**	**0.17**	**0.16**	**0.16**	**0.16**
SONOS highest W/E voltage (V) [35]	**6.0–7.0**	**6.0–7.0**	**5.0–6.0**	**5.0–6.0**	**5.0–5.5**	**5.0–5.5**	**5.0–5.5**
SONOS/NROM I_{read} (μA) [36]	**35–45**	**33–43**	**31–41**	**29–39**	**27–37**	**25–35**	**25–35**
SONOS/NROM tunnel oxide thickness (nm) [37]	**5**	**5**	**4.5**	**4**	**3.5**	**3.5**	**3.5**
SONOS/NROM nitride dielectric thickness (nm) [38]	**6**	**5**	**5**	**4.5**	**4**	**4**	**4**
SONOS/NROM blocking (top) oxide thickness (nm) [39]	**5**	**5**	**4.5**	**4.5**	**4**	**4**	**4**
SONOS/NROM endurance (erase/write cycles) [40]	**1.00E+06**	**1.00E+06**	**1.00E+07**	**1.00E+07**	**1.00E+07**	**1.00E+07**	**1.00E+07**
SONOS/NROM nonvolatile data retention (years) [41]	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**
MRAM technology node F (nm) [42]	**180**	**130**	**90**	**90**	**65**	**55**	**50**
MRAM cell size area factor a in multiples of F^2 [43]	**24.7**	**23.7**	**24.7**	**22.2**	**22.2**	**22.2**	**22.2**
MRAM typical cell size (μm^2) [44]	**0.8**	**0.4**	**0.2**	**0.18**	**0.09**	**0.07**	**0.06**
MRAM switching field (Oe) [45]	**50**	**60**	**80**	**70**	**90**	**100**	**110**
MRAM write energy (pJ) [46]	**150**	**100**	**70**	**70**	**50**	**45**	**40**
MRAM active area per cell (μm^2) [47]	**0.28**	**0.2**	**0.11**	**0.1**	**0.05**	**0.04**	**0.03**
MRAM resistance-area product (Kohm-μm^2) [48]	**3**	**2.5**	**2**	**1.7**	**1.5**	**1.3**	**1.2**
MRAM magnetoresistance ratio(%) [49]	**45**	**45**	**50**	**50**	**60**	**60**	**60**
MRAM nonvolatile data retention (years) [50]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**
MRAM write endurance (read/write cycles) [51]	**>1e15**	**>1e15**	**>1e15**	**>1e15**	**>1e15**	**>1e15**	**>1e15**
MRAM endurance – tunnel junction reliability (years at bias) [52]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

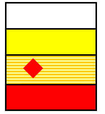


Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED

	Year of Production	2010	**2011**	2012	2013	**2014**	2015	2016	**2017**	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	**40**	35	32	**28**	25	22	**20**	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Flash technology node – F (nm) [1]	50		39	35		28	25		20
IS	Flash technology node – F (nm) [1]	45	40	35	32	28	25	22	20	18
WAS	Flash NOR cell size – area factor a in multiples of F^2 [2]	12–15		12–15	13–16		14–17	14–17		15–18
IS	Flash NOR cell size – area factor a in multiples of F^2 [2]	12–15	12–15	12–15	13–16	13-16	14–17	14–17	15-18	15–18
WAS	Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [3]	4.5/2.3		4.5/2.3	4.5/2.3		4.5/2.3	4.5/2.3		4.5/2.3
IS	Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [3]	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3
WAS	Flash NOR typical cell size (μm^2) [4]	0.034		0.021	0.018		0.012	0.01		0.007
IS	Flash NOR typical cell size (μm^2) [4]	0.027	0.022	0.017	0.017	0.011	0.01	0.008	0.007	0.005
WAS	Flash NOR L_g-stack (physical – μm) [5]	0.17–0.19		0.15–0.17	0.14–0.16		0.13–0.15	0.12–0.14		0.11–0.13
IS	Flash NOR L_g-stack (physical – μm) [5]	0.17–0.19	0.16-0.18	0.15–0.17	0.14–0.16	0.14-0.16	0.13–0.15	0.12–0.14	0.12-0.14	0.11–0.13
WAS	Flash NOR highest W/E voltage (V) [6]	7–9		7–9	7–9		7–9	7–9		7–9
IS	Flash NOR highest W/E voltage (V) [6]	7–9	7-9	7–9	7–9	7-9	7–9	7–9	7-9	7–9
WAS	Flash NAND highest W/E voltage (V) [7]	15–17		15–17	15–17		15–17	15–17		15–17
IS	Flash NAND highest W/E voltage (V) [7]	15–17	15-17	15–17	15–17	15-17	15–17	15–17	15-17	15–17
WAS	Flash NOR I_{read} (μA) [8]	27–33		26–32	25–31		23–29	22–28		20–26
IS	Flash NOR I_{read} (μA) [8]	27–33	27–33	26–32	25–31	24-30	23–29	22–28	21-27	20–26
WAS	Flash Coupling Ratio [9]	0.6–0.7		0.6–0.7	0.6–0.7		0.6–0.7	0.6–0.7		0.6–0.7
IS	Flash Coupling Ratio [9]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
WAS	Flash NOR tunnel oxide thickness (nm) [10]	8–9		8–9	8		8	8		8
IS	Flash NOR tunnel oxide thickness (nm) [10]	8–9	8–9	8–9	8–9	8	8	8	8	8
WAS	Flash NAND tunnel oxide thickness (nm) [11]	6–7		6–7	6–7		6–7	6–7		6–7
IS	Flash NAND tunnel oxide thickness (nm) [11]	6–7	6–7	6–7	6–7	6–7	6–7	6–7	6–7	6–7
WAS	Flash NOR interpoly dielectric thickness (nm) [12]	8–10		7–9	6–8		5–7	4–6		3–5
IS	Flash NOR interpoly dielectric thickness (nm) [12]	8–10	8–10	8–10	8–10	7-9	6-8	6-8	6-8	6-8
WAS	Flash NAND interpoly dielectric thickness (nm) [13]	10–13		10–13	9–10		9–10	9–10		9–10
IS	Flash NAND interpoly dielectric thickness (nm) [13]	10–13	10–13	10–13	9–10	9–10	9–10	9–10	9–10	9–10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

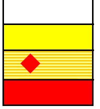


Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	**2011**	2012	2013	**2014**	2015	2016	**2017**	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	**40**	35	32	**28**	25	22	**20**	18
WAS	Flash endurance (erase/write cycles) [14]	1.00E+06		1.00E+06	1.00E+06		1.00E+06	1.00E+07		1.00E+07
IS	Flash endurance (erase/write cycles) [14]	1.E+06	1.E+06	1.E+06	1.E+06	1.E+06	1.E+06	1.E+07	1.E+07	1.E+07
WAS	Flash nonvolatile data retention (years) [15]	10–20		10–20	20		20	20		20
IS	Flash nonvolatile data retention (years) [15]	10–20	10–20	10–20	20	20	20	20	20	20
WAS	Flash maximum number of bits per cell (MLC) [16]	8		8	8		8	8		8
IS	Flash maximum number of bits per cell (MLC) [16]	8	8	8	8	8	8	8	8	8
WAS	FeRAM technology node – F (nm) [17]	100		80	70		57	50		45
IS	FeRAM technology node – F (nm) [17]	100	90	80	70	64	57	50	48	45
WAS	FeRAM cell size – area factor a in multiples of F^2 [18]	8		8	8		8	8		8
IS	FeRAM cell size – area factor a in multiples of F^2 [18]	8	8	8	8	8	8	8	8	8
WAS	FeRAM cell size (μm^2) [19]	0.08		0.051	0.039		0.026	0.02		0.016
IS	FeRAM cell size (μm^2) [19]	0.08	0.065	0.051	0.039	0.033	0.026	0.02	0.018	0.016
WAS	FeRAM cell structure [20]	1T1C		1T1C	1T1C		1T1C	1T1C		1T1C
IS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
WAS	FeRAM capacitor structure [21]	3D		3D	3D		3D	3D		3D
IS	FeRAM capacitor structure [21]	3D	3D	3D	3D	3D	3D	3D	3D	3D
WAS	FeRAM capacitor footprint (μm^2) [22]	0.03		0.019	0.015		0.01	0.0075		0.0061
IS	FeRAM capacitor footprint (μm^2) [22]	0.071	0.065	0.06	0.057	0.052	0.048	0.045	0.042	0.038
WAS	FeRAM capacitor active area (μm^2) [23]	0.076		0.065	0.06		0.052	0.048		0.045
IS	FeRAM capacitor active area (μm^2) [23]	0.024	0.02	0.015	0.013	0.01	0.008	0.0061	0.005	0.0037
WAS	FeRAM cap active area/footprint ratio [24]	2.53		3.42	4		5.2	6.4		7.38
IS	FeRAM cap active area/footprint ratio [24]	2.9	3.25	4	4.4	5.2	6	7.4	8.4	10.3
WAS	Ferro capacitor voltage (V) [25]	1		1	0.7		0.7	0.7		0.7
IS	Ferro capacitor voltage (V) [25]	1	1	1	0.7	0.7	0.7	0.7	0.7	0.7
WAS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	40		40	40		40	40		40
IS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	40	40	40	40	40	40	40	40	40

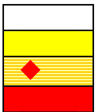
Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known

Manufacturable solutions are NOT known

Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	FeRAM endurance (read/write cycles) [27]	>1E16		>1E16	>1E16		>1E16	>1E16		>1E16
IS	FeRAM endurance (read/write cycles) [27]	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16
WAS	FeRAM nonvolatile data retention (years) [28]	10		10	10		10	10		10
IS	FeRAM nonvolatile data retention (years) [28]	10	10	10	10	10	10	10	10	10
WAS	SONOS/NROM technology node – F (nm) [29]	50		40	35		28	25		20
IS	SONOS/NROM technology node – F (nm) [29]	50	45	40	35	32	28	25	23	20
WAS	SONOS/NROM cell size – area factor a in multiples of F^2 [30]	6		6	6.5		6.5	7		7
IS	SONOS/NROM cell size – area factor a in multiples of F^2 [30]	6	6	6	6.5	6.5	6.5	7	7	7
WAS	SONOS/NROM typical cell size (mm^2) [31]	0.015		0.01	0.008		0.005	0.004		0.003
IS	SONOS/NROM typical cell size (mm^2) [31]	0.015	0.012	0.01	0.008	0.007	0.005	0.004	0.0037	0.003
WAS	SONOS/NROM maximum number of bits per cell (MLC) [32]	4		4	4		4	4		4
IS	SONOS/NROM maximum number of bits per cell (MLC) [32]	4	4	4	4	4	4	4	4	4
WAS	SONOS/NROM area per bit (mm^2) [33]	0.0038		0.0024	0.002		0.0013	0.0011		0.0007
IS	SONOS/NROM area per bit (mm^2) [33]	0.0038	0.003	0.0024	0.002	0.0018	0.0013	0.0011	0.0009	0.0007
WAS	SONOS L_g-stack (physical – µm) [34]	0.16		0.16	0.15		0.15	0.14		0.14
IS	SONOS L_g-stack (physical – µm) [34]	0.16	0.16	0.16	0.15	0.15	0.15	0.14	0.14	0.14
WAS	SONOS highest W/E voltage (V) [35]	5.0–5.5		5.0–5.5	5.0–5.5		5.0–5.5	4.5–5.0		4.0–4.5
IS	SONOS highest W/E voltage (V) [35]	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	4.5.–5.0	4.5.–5.0	4.0–4.5
WAS	SONOS/NROM I_{read} (µA) [36]	25–35		24–34	23–33		22–32	21–31		20–30
IS	SONOS/NROM I_{read} (µA) [36]	25–35	25–35	24–34	23–33	23–33	22–32	21–31	21–31	20–30

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

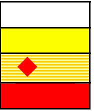


Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	**2011**	2012	2013	**2014**	2015	2016	**2017**	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	**40**	35	32	**28**	25	22	**20**	18
WAS	SONOS/NROM tunnel oxide thickness (nm) [37]	3		3	2.5		2.5	2		2
IS	SONOS/NROM tunnel oxide thickness (nm) [37]	3	3	3	2.5	2.5	2.5	2	2	2
WAS	SONOS/NROM nitride dielectric thickness (nm) [38]	4		4	4		4	3.5		3.5
IS	SONOS/NROM nitride dielectric thickness (nm) [38]	4	4	4	4	4	4	3.5	3.5	3.5
WAS	SONOS/NROM blocking (top) oxide thickness (nm) [39]	4		4	4		4	4		4
IS	SONOS/NROM blocking (top) oxide thickness (nm) [39]	4	4	4	4	4	4	4	4	4
WAS	SONOS/NROM endurance (erase/write cycles) [40]	1.00E+08		1.00E+08	1.00E+08		1.00E+08	1.00E+09		1.00E+09
IS	SONOS/NROM endurance (erase/write cycles) [40]	1.E+08	1.E+08	1.E+08	1.E+08	1.E+08	1.E+08	1.E+09	1.E+09	1.E+09
WAS	SONOS/NROM nonvolatile data retention (years) [41]	10–20		10–20	10–20		10–20	10–20		10–20
IS	SONOS/NROM nonvolatile data retention (years) [41]	10–20	10–20	10–20	10–20	10–20	10–20	10–20	10–20	10–20
WAS	MRAM technology node – F (nm) [42]	45		35	32		25	22		18
IS	MRAM technology node – F (nm) [42]	45	40	35	32	28	25	22	20	18
WAS	MRAM cell size – area factor a in multiples of F^2 [43]	22.2		22.2	22.2		22.2	22.2		22.2
IS	MRAM cell size – area factor a in multiples of F^2 [43]	22.2	22.2	22.2	22.2	22.2	22.2	22.2	22.2	22.2
WAS	MRAM typical cell size (μm^2) [44]	0.04		0.03	0.02		0.01	0.01		0.01
IS	MRAM typical cell size (μm^2) [44]	0.045	0.036	0.027	0.023	0.017	0.014	0.01	0.009	0.007
WAS	MRAM switching field (Oe) [45]	120		120	120		120	120		120
IS	MRAM switching field (Oe) [45]	120	120	120	120	120	120	120	120	120
WAS	MRAM write energy (pJ) [46]	35		30	25		23	20		18
IS	MRAM write energy (pJ) [46]	35	33	30	25	24	23	20	19	18
WAS	MRAM active area per cell (μm^2) [47]	0.03		0.02	0.01		0.01	0.01		0.01
IS	MRAM active area per cell (μm^2) [47]	0.03	0.025	0.02	0.01	0.01	0.01	0.01	0.01	0.01

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

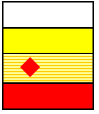


Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	**2011**	2012	2013	**2014**	2015	2016	**2017**	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	**40**	35	32	**28**	25	22	**20**	18
WAS	MRAM resistance-area product (Kohm-μm^2) [48]	1.1		0.95	0.8		0.7	0.6		0.55
IS	MRAM resistance-area product (Kohm-μm^2) [48]	1.1	1	0.95	0.8	0.75	0.7	0.6	0.6	0.55
WAS	MRAM magnetoresistance ratio(%) [49]	60		65	70		70	70		70
IS	MRAM magnetoresistance ratio(%) [49]	60	65	65	70	70	70	70	70	70
WAS	MRAM nonvolatile data retention (years) [50]	>10		>10	>10		>10	>10		>10
IS	MRAM nonvolatile data retention (years) [50]	>10	>10	>10	>10	>10	>10	>10	>10	>10
WAS	MRAM write endurance (read/write cycles) [51]	>1e15		>1e15	>1e15		>1e15	>1e15		>1e15
IS	MRAM write endurance (read/write cycles) [51]	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15
WAS	MRAM endurance – tunnel junction reliability (years at bias) [52]	>10		>10	>10		>10	>10		>10
IS	MRAM endurance – tunnel junction reliability (years at bias) [52]	>10	>10	>10	>10	>10	>10	>10	>10	>10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 50a and 50b:

[1] In the past Flash devices tended to lag behind the current CMOS technology node, but that delay no longer exists. This entry provides the F value for designs in the indicated time period.

[2] The area factor "a" = cell area/F^2, so this entry presents the expected range for Flash NOR cell area in multiples of the implementation technology node F^2. Note the lack of long term scaling.

[3] The area factor "a" = cell area/F^2, so this entry presents the Flash NAND cell area in multiples of F^2 the implementation technology node. Flash NAND enjoys a small cell size because much of the cell structure is shared among a group of cells. (SLC single level cell, MLC multilevel cell.)

[4] A typical Flash NOR cell size in micrometers squared is estimated using the midrange area factor "a."

[5] This is the physical length of the control gate of Flash NOR devices.

[6, 7] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.

*[8]The current reduces with scaling at a rate higher than W/(L*Cox) to reduce the voltage overdrive factor.*

[9]The coupling ratio is the (control gate to floating gate capacitance)/(total floating gate to source, drain and substrate capacitance).

[10, 11] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade off problem hinders scaling.

[12, 13] Interpoly dielectric must be thick enough to assure retention but thin enough to assure an almost constant coupling ratio. Charge retention when the dielectric is scaled downward is the major issue.

[14] E/W endurance requirements vary with the specifics of an application, but 1E5 cycles have been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.

[15] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.

[16] Cell read out distinguishes between four levels of charge storage to provide two storage bits. Progression to 16 and 256 levels is anticipated. (MLC multilevel cell).

[17]This entry is the critical dimension "F" within the FeRAM cell for stand-alone memory devices (not embedded devices).

[18] This is the area factor "a" = cell size/F^2. FeRAM cell size is presented in terms of F^2 multiples of the FeRAM implementation technology node.

[19] FeRAM cell size is presented in terms of micrometers squared. It is the product $a \times F^2$.

[20]FeRAM cell structures have migrated to one transistor, one capacitor (1T1C) formats. Other alternative configurations are under investigation such as Chain-FeRAM.

[21] The geometry of the capacitor is a key factor in determining cell size. Stacked planar films are expected to be replaced by more efficient 3D structures.

[22] This is the footprint of the capacitor in micrometers squared. It is this area that constitutes the capacitor area contribution to the cell size. For 2003–2004 $8F^2$, for 2005–2009 $4F^2$, and for 2010–2018 F^2 are assumed.

[23] This is the actual effective area of the capacitor. It can be larger than the footprint because of the utilization of area in the third dimension.

[24] This ratio of the effective area to the footprint gives a measure of the impact of utilization of the third dimension.

[25] This is the operating voltage (V_{op}) applied to the capacitor. Low voltage operation is a difficult key design issue.

[26] The minimum switching charge density in $\mu C/cm^2$ is a useful design parameter. It is equal to the cell minimum switching charge divided by the capacitor actual effective area. The capacitor voltage is taken as V_{op}.

[27] FeRAM is a destructive read-out technology, so every read is accompanied by a write to restore the data. Endurance cycles are taken as the sum of all read and all write cycles. For FeRAM to compete with DRAM and SRAM the cycle endurance should be about 1E15. Test time is a serious concern. Note that operation at 100 MHz for 10 years would accumulate 1E16 cycles.

[28] This is the data retention requirement while the device is disconnected from power. It is usually specified at 85ºC.

[29] SONOS/NROM devices have recently been introduced into the commercial market and will tend to lag the current CMOS technology node by one year; however, similar to Flash floating-gate technology, this gap will close rapidly due to low programming voltages combined with CMOS compatibility (i.e. single-level polysilicon). This entry provides the F value for designs in the indicated time period.

[30] The area factor "a" = cell area/F^2. This entry depicts the expected SONOS/NROM NOR cell area in multiples of the implementation technology node F^2. The reduced ONO gate stack thickness and low programming voltages should permit long range scaling of this technology.

[31] The expected "typical" SONOS/NROM NOR cell size is presented in terms of micrometers squared.

[32] MBC signifies "multiple bit storage," while MLC signifies "multiple level storage." The SONOS/NROM cell stores charge in two distinct locations – in the nitride over the source and drain junctions. Thus, in the simplest case there are two distinct bits within each cell; however, each charge location may be partitioned into multiple levels, thereby, increasing the bit storage per cell.

[33] The expected "typical" SONOS/NROM NOR area per bit is presented in terms of micrometers squared.

[34] This is the physical length of the gate of SONOS/NROM devices in micrometers as there is only a single gate, similar to a MOSFET.

[35] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.

*[36] Reduction rate is higher than (W/L)*Cox) to reduce the voltage overdrive factor.*

[37] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This offers a challenge to scaling.

[38] The nitride dielectric provides the charge storage medium and its thickness is a compromise between program/erase voltages, erase/write window, retention, process control and endurance. This offers a challenge to scaling.

[39] The blocking (top) oxide thickness isolates the charge storage region (nitride) from the gate electrode. Its thickness is a compromise between program/erase voltages and retention. This offers a challenge to scaling.

[40] E/W endurance (erase/write cycles) requirements vary with the specifics of an application, but 1E5cycles has been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.

[41] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.

[42] MRAM devices are expected to lag the CMOS current technology node up until the 65 nm node in 2007. This entry provides the F value for designs in the indicated time period.

[43] The area factor "a" = cell area/F^2. This entry is the expected MRAM cell area in multiples of the implementation technology node F^2.

[44] The expected "typical" MRAM cell size is presented in micrometers squared.

[45] The MRAM switching field is the magnetic intensity H required to change the direction of magnetization of the cell.

*[46] MRAM switching energy per bit is calculated as (write current * power supply voltage * write time). It is preferred to use the median value of switching energy measured on a multi-megabit array. A good estimate of power drain is (switching energy * number of writes per second).*

*[47] MRAM active bit area is the area of the magnetic material stack within the cell. It represents the "A" in the R*A product.*

*[48] MRAM resistance-area product (i.e., the R*A product) is an intrinsic property of the magnetic material stack that provides a convenient basis for comparing cells of different sizes. The R*A product can be computed by measuring the effective low state resistance (R_{low}) of the magnetic tunnel junction and multiply it by the active bit area of the magnetic stack.*

[49] MRAM magnetoresistive ratio is calculated as $100*(R_{high} – R_{low})/R_{low}$. This ratio summarizes the difference between a logic ONE and a logic ZERO, and as such it represents the intrinsic capability of the magnetic stack. The magnetic tunnel junction resistance values are to be measured at low currents.

[50] MRAM devices are required to retain data while unpowered. This entry states the retention requirement in years.

[51] This entry is the required number of read/write cycles that an MRAM device must be able to endure without degradation that impacts the ability of the device to pass all operating specifications.

[52] An MRAM device is required to meet this minimum life requirement when the magnetic material stack is continuously under bias.

Table 51 Reliability Difficult Challenges

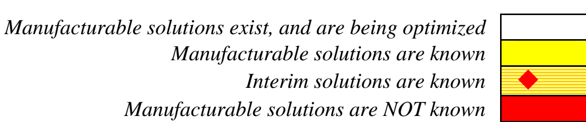
Difficult Challenges ≥45 nm/ Through 2010	*Summary of Issues*
High-κ Gate Dielectrics	Dielectric breakdown characteristics (hard and soft breakdown) Influence of charge trapping and NBTI on threshold voltage stability Stability and number of fixed charges
Metal Gate	Impact of metal-ion drift and/or diffusion on gate dielectric reliability Work function control and stability Metal susceptibility to oxidation Thermo-mechanical issues due to large thermal expansion mismatch Impact of implantation
Copper/Low-κ Interconnects	Stress migration of Cu vias and lines Cu via and line electromigration performance Thermal-mechanical stability of the interfaces between metals, barriers and interlevel dielectrics and resulting line-to-line leakage Time Dependent Dielectric Breakdown (TDDB) of the Cu/low-κ system Reliability impact of lower thermal conductivity of low-κ dielectric Reliability issues due to the porous nature of the low-κ dielectrics and moisture Reliability impact of the lower mechanical strength in the Cu/low-κ system, including the impact of packaging
Packaging	Ability of bumps to withstand thermal and mechanical stresses while providing sufficient current carrying capability Solder joints fracture at 1st and 2nd level interconnects Electromigration in package traces, vias and bumps Impact of increasing Coefficient of Thermal Expansion (CTE) mismatch between low-κ, silicon and organic packages
Design and Test for Reliability	Simulation tools for concurrent optimization of circuit performance and reliability Tools to simulate electromigration, thermal-mechanical stress and process induced charging Soft error detection and correction at chip and system level, including random logic faults Screens for resistive and capacitively coupled interconnect defects Alternative screens for decreasing burn-in effectiveness

Table 52a Reliability Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	
*Early failures (ppm) (First 4000 operating hours)** [1]*	**50–2000**	**50–2000**	**50–2000**	**50–2000**	**◆50–2000**	**◆50–2000**	**◆50–2000**	*Customer needs; new materials (High κ in 2004)*
Long term reliability (FITS = failures in 1E9 hours) [2]	**10–100**	**10–100**	**10–100**	**10–100**	**◆10–100**	**◆10–100**	**◆10–100**	*Customer needs; new materials (High κ in 2004)*
Soft error rate (FITs)	**1000**	**1000**	**1000**	**1000**	**◆1000**	**◆1000**	**◆1000**	*Scaling*
Relative failure rate per transistor (normalized to 130 nm) [3]	**1**	**0.8**	**0.63**	**0.5**	**◆ 0.4**	**TBD**	**TBD**	*Number of transistors*
Relative failure rate per m of interconnect (normalized to 130 nm node) [4]	**1**	**0.84**	**0.64**	**0.58**	**◆ 0.52**	**◆ 0.41**	**◆ 0.37**	*Customer needs; J11 length of interconnect*

Table 52b Reliability Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
*Early failures (ppm) (First 4000 operating hours)**[1]*	**◆50–2000**	**50–2000**	**50–2000**	**50–2000**	**50–2000**	**50–2000**
Long term reliability (FITS = failures in 1E9 hours) [2]	**◆10–100**	**10–100**	**10–100**	**10–100**	**10–100**	**10–100**
Soft error rate (FITs)	**◆ 1000**	**1000**	**1000**	**1000**	**1000**	**1000**
Relative failure rate per transistor (normalized to 130 nm) [3]	**◆ 0.2**		**0.1**		**0.04**	
Relative failure rate per m of interconnect (normalized to 130 nm) [4]	**◆ 0.36**	**0.26**	**0.25**	**0.16**	**0.17**	**0.11**



Notes for Tables 52a and 52b:
Reliability requirements vary with different applications. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to be improved. Degradation of current reliability levels is not acceptable. Reliability requirements are for the packaged device and include both chip and package related failure modes.
A reliability qualification can always be attempted with available knowledge. The better the knowledge the less risk in the qualification and vice versa. Yellow coloring indicates some risk. Striped indicates a greater risk (due to changed and possible new failure mode 0. Finally, red indicates an unspecified solution (e.g., what technology will be used for post-CU) for which the reliability risk cannot be assessed until details about the solution are provided.
[1] Failures during the first 4000 hours of operation (~1 year's use at 50% duty cycle). Early failures are associated with defects.
[2] Long term reliability rate applies for the specified lifetime of the IC.
[3] While the overall IC failure rate does not change with time, as the number of transistors increase [from ORTC], the relative failure rate per transistor must decrease.
[4] As the length of interconnect increases [from Interconnect Technology Requirements Tables], the failure rate per m of interconnect must decrease. Even more important for reliability is the increase in the number of vias.