

METROLOGY

Table 96 Metrology Difficult Challenges

<i>Five Difficult Challenges ≥ 65 nm, Through 2007</i>	<i>Summary of Issues</i>
Factory level and company wide metrology integration for real time <i>in situ</i> , integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during RTA.
Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. Key requirements are void detection in copper lines and pore size distribution in patterned low κ dielectrics.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers. High frequency dielectric constant measurements advances need to continue.
Measurement test structures and reference materials.	Scribe lines are shrinking and correlation to variation of chip properties is difficult. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between scribe line measurement and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate stable reference materials.
<i>Five Difficult Challenges < 65 nm, Beyond 2007</i>	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for Damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	The wearout mechanism for new, high κ gate and capacitor dielectric materials is unknown.
Statistical limits of sub-65 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
3D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

Table 97a Metrology Technology Requirements—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007	Driver
DRAM ½ Pitch (nm)		130	115	100	90	80	70	65	
MPU / ASIC ½ Pitch (nm)		150	130	107	90	80	70	65	
MPU Printed Gate Length (nm)		90	75	65	53	45	40	35	
MPU Physical Gate Length (nm)		65	53	45	37	32	28	25	
<i>Microscopy</i>									
Was	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.65	0.53	0.45	0.37	0.32	0.3	0.25	MPU Gate
Is	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	<u>0.5</u>	<u>0.4</u>	<u>0.4</u>	<u>0.3</u>	<u>0.3</u>	<u>0.2</u>	<u>0.2</u>	MPU Gate
Was	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	11.4	11.9	12.4	13	13.6	14.3	15.2	
Is	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	<u>11.4</u> 150	<u>11.9</u> 130	<u>12.4</u> 110	<u>13</u> 90	<u>13.6</u> 80	<u>14.3</u> 70	<u>15.2</u> 65	D1/2
<i>Materials and Contamination Characterization</i>									
	Real particle detection limit (nm) [B]	65	53	45	37	32	30	25	D1/2
	Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	43	35	30	24	21	20	17	D1/2
	Specification limit of total surface contamination for critical COI surface materials (atoms/cm ²) [C]	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	MPU Gate
	Surface detection limits for individual elements for critical GOI elements (atoms/cm ²) with signal-to-noise ratio of 3:1 for each element	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	MPU Gate

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Table 97b Metrology Technology Requirements—Long-term

Year of Production		2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	
	MPU / ASIC ½ Pitch (nm)	45	32	22	
	MPU Printed Gate Length (nm)	25	18	13	
	MPU Physical Gate Length (nm)	18	13	9	
<i>Microscopy</i>					
Was	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.18	0.13	0.09	MPU
Is	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.15	0.11	0.07	MPU
Was	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	16.1	19.3	23.2	D1/2
Is	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	16.1 45	19.3 32	23.2 22	D1/2
<i>Materials and Contamination Characterization</i>					
	Real particle detection limit (nm) [B]	18	13	9	D1/2
	Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	12	9	6	D1/2
	Specification limit of total surface contamination for critical COI surface materials (atoms/cm ²) [C]	5.00E+09	5.00E+09	5.00E+09	D1/2
	Surface detection limits for individual elements for critical GOI elements (atoms/cm ²) with signal-to-noise ratio of 3:1 for each element	5.00E+08	5.00E+08	5.00E+08	D1/2

















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Table 98a Lithography Wafer Metrology Technology Requirements—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Add	Printed Gate CD Control (nm) Allowed Litho Variance = 2/3 Total Variance of physical gate length	 5.3	 4.3	3.7	3.0	2.6	2.3	2.0
Was	Wafer gate CD control*	6.5	5.3	4.5	3.7	3.2	2.8	2.5
Delete	Wafer Gate CD Control (nm) total allowed range for physical gate length*	6.5	5.3	4.5	3.7	3.2	2.8	2.5
	Wafer dense line CD control*	13	11.5	10	9	8	7	6.5
Was	Wafer contact CD control*	15	13	11.5	10	9	8	7
Is	Wafer contact CD control (nm)*	 15	 13	 11	9	8	7	6.5
Was	Line Edge Roughness control*	4.5	3.9	3.3	2.7	2.4	2.1	1.8
Is	Line Edge Roughness control (nm)*	4.5	3.9	3.3	2.7	2.4	2.1	1.8
Was	Wafer CD metrology tool precision* (P/T=.2 for isolated lines**)	1.3	1.1	0.9	0.75	0.65	0.56	0.5
Is	Wafer CD metrology tool precision (nm)* 3σ at P/T = 0.2 for printed and physical lines [A]	 1.1	 0.86	 0.73	0.60	0.52	0.46	0.41
Was	Wafer CD metrology tool precision* (P/T=.2 for dense lines**)	2.6	2.3	2	1.8	1.6	1.4	1.3
Is	Wafer CD metrology tool precision (nm)* (P/T=.2 for dense lines**)	 2.6	 2.3	 2	1.8	1.6	1.4	1.3
Was	Wafer CD metrology tool precision* (P/T=.2 for contacts**)	3	2.6	2.3	2	1.8	1.6	1.4
Is	Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)	3	2.6	2.2	1.8	1.6	1.4	1.3
Was	Wafer CD metrology tool precision* (P/T=.2 for LER**)	0.9	0.78	0.66	0.54	0.48	0.42	0.36
Is	Wafer CD metrology tool precision (nm) * (P/T=.2 for LER**)	 0.9	 0.78	 0.66	0.54	0.48	0.42	0.36
	Maximum CD measurement bias (%)	10	10	10	10	10	10	10
Was	Wafer overlay control (nm)	65	58	52	45	42	38	35
Is	Wafer overlay control (nm)	46	40	35	32	28	25	23
Was	Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	6.5	5.8	5.2	4.5	4.2	3.8	3.5
Is	Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	4.6	 4.0	 3.5	3.2	2.8	2.5	2.3

* All precision values are 3 Sigma in nm and include metrology tool to tool matching

** Measurement tool performance needs to be independent of target shape, material, and density

LER—Local linewidth variation (3 Sigma total, all frequency components included, both edges) evaluated along a distance equal to four technology nodes"

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Table 98b Lithography Metrology Technology Requirements—Long-term

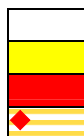
Year of Production		2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	45	32	22
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
Add	Printed Gate CD Control (nm) Allowed Litho Variance = 2/3 Total Variance of physical gate length	1.5	1.1	0.7
Was	Wafer gate CD control*	1.8	1.3	0.9
Delete	Wafer Gate CD Control (nm) total allowed range for physical gate length*	4.8	4.3	0.9
Was	Wafer dense line CD control*	4.5	3.2	2.2
Is	Wafer dense line CD control (nm) *	4.5	3.2	2.2
Was	Wafer contact CD control*	5	3.5	2.5
Is	Wafer contact CD control (nm) *	4.5	3.2	2.2
	Line Edge Roughness control*	1.3	0.9	0.65
Was	Wafer CD metrology tool precision* (P/T=.2 for isolated lines**)	0.36	0.26	0.18
Is	Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for printed and physical lines [A]	0.29	0.21	0.15
Was	Wafer CD metrology tool precision* (P/T=.2 for dense lines**)	0.9	0.64	0.44
Is	Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	0.9	0.64	0.44
Was	Wafer CD metrology tool precision* (P/T=.2 for contacts**)	1	0.7	0.5
Is	Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)	0.9	0.64	0.44
Was	Wafer CD metrology tool precision* (P/T=.2 for LER**)	0.26	0.18	0.13
Is	Wafer CD metrology tool precision (nm) * (P/T=.2 for LER**)	0.26	0.18	0.13
	Maximum CD measurement bias (%)	10	10	10
Was	Wafer overlay control (nm)	18	13	9
Is	Wafer overlay control (nm)	15.8	11.2	7.7
Was	Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	1.8	1.3	0.9
Is	Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	1.6	1.1	0.77

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[A] The red designation for CD measurement for isolated lines in the near term is a result of roadmap process range and need for tool matching in the precision requirement also makes this requirement very difficult to achieve.

Precision values are based on need to control to Litho allowed range in printed lines.

Long term, CD measurement for 25 nm linewidths requires a technology breakthrough because extension of known methods may not be possible.

Table 100a Front End Processes Metrology Technology Requirements—Near-term

Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	
MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm ³)	1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	*
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm ³)	1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	*
High-performance logic EOT equivalent oxide thickness (EOT) nm	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	
Low operating power logic EOT	2	1.8	1.6	1.4	1.2	1.1	1	
± 3σ dielectric process range (EOT) (nm)	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	M Gate
EOT measurement precision 3σ (nm) [B]	0.0052	0.0048	0.0044	0.0036	0.0032	0.0028	0.0024	MPU High-performance
DRAM capacitor structure	Cyl.	Pedestal	Pedestal	Pedestal	Pedestal	Pedestal	Pedestal	
DRAM capacitor electrodes	MIS	MIM	MIM	MIM	MIM	MIM	MIM	
Was DRAM capacitor dielectric material	Ta ₂ O ₅	Ta ₂ O ₅	bb	Ta ₂ O ₅	Not BST??	BST	Epi-BST	D½
Is DRAM capacitor dielectric material	Ta ₂ O ₅	Ta ₂ O ₅	Ta ₂ O ₅	Ta ₂ O ₅	BST	BST	Epi-BST	
Was DRAM capacitor dielectric constant	>22	>50	>50	>50	>250	>250	>700	
Is DRAM capacitor dielectric constant	22	22	50	50	250	300	450	
Equivalent oxide thickness (EOT) (nm)	3	0.95	0.95	0.95	0.45	0.45	0.15	
Was DRAM capacitor dielectric physical thickness (nm) ± 3σ process range	11.5 ±4%	12.2 ±4%	12.2 ±4%	12.2 ±4%	28.7 ±4%	28.7 ±4%	27.2 ±4%	D½
Is DRAM capacitor dielectric physical thickness (nm) ± 3σ process range	5.9 ±4%	4.5 ±4%	15.3 ±4%	12.8 ±4%	28.7 ±4%	24.7 ±4%	25 ±4%	D½
Was DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.046	0.049	0.049	0.049	0.11	0.11	0.11	D½
Is DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.02	0.02	0.06	0.05	0.11	0.10	0.10	D½
Dopant concentration (atoms/cm ³)	3 × 10 ¹⁸	4 × 10 ¹⁸	4 × 10 ¹⁸	5 × 10 ¹⁸	6 × 10 ¹⁸	7 × 10 ¹⁸	8 × 10 ¹⁸	D½
Dopant atom	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	MPU
Metrology for junction depth of (nm)	27	22	19	15	13	12	10	
Lateral Steepness of dopant profile (nm/decade)	5.1	4.7	4.25	4	3.8	3.5	3.3	
Was Lateral/depth spatial resolution for 2D / 3D dopant profile (nm)	4.1 / 5.2	2	2	3.9 / 4.0	1.5	1.5	2.6 / 2.0	
Is Lateral/depth spatial resolution for 2D / 3D dopant profile (nm)	4.1 / 5.2	2	2	3.9 / 4.0	1.5	1.5	2.6 / 2.0	*
At-line dopant concentration precision (across concentration range) [D]	5%	4%	4%	4%	3%	3%	2%	*

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Table 100b Front End Processes Metrology Technology Requirements—Long-term

Year of Production		2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	
	MPU / ASIC ½ Pitch (nm)	45	32	22	
	MPU Printed Gate Length (nm)	25	18	13	
	MPU Physical Gate Length (nm)	18	13	9	
	Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm ³)	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	
	Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm ³)	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	
	High-performance logic EOT [A] equivalent oxide thickness (EOT) nm	0.5–0.8	0.4–0.6	0.4–0.5	
	Low operating power logic EOT	0.9	0.8	0.6	
	± 3σ process range (EOT) (nm)	± 4%	± 4%	± 4%	
	Logic dielectric measurement precision 3σ (nm) [B]	0.002	0.0016	0.0016	MPU high - performance
Was	DRAM capacitor structure dielectric material process control requirements	Pedestal MIM epi-BST	Pedestal MIM ???	Pedestal MIM ???	
Is	DRAM capacitor structure dielectric material process control requirements	Pedestal MIM	Pedestal MIM	Pedestal MIM	
Was	(Dielectric constant)	>700	>1500	>1500	D ½
Is	(Dielectric constant)	800	1500	3000	
Was	Equivalent oxide thickness (nm)	0.15	0.06	0.043	
Is	Equivalent oxide thickness (nm)	0.08	0.028	0.01	
	DRAM capacitor dielectric physical thickness (nm) ±3σ process range [C]	27.2 ± 4%	23 4%	16.4 4%	D ½
	DRAM capacitor dielectric physical thickness measurement precision (nm 3σ)	0.11	0.092	0.066	D ½
	Dopant concentration (atoms/cm ³)	1.4 × 10 ¹⁹	2.0 × 10 ¹⁹	? × 10 ¹⁹	
	Dopant atom	P, As, B	P, As, B	P, As, B	MPU
	Metrology for junction depth of (nm)	7	5	4	
	Lateral Steepness of dopant profile (nm/decade)	2.7	1.9	1.6	
	Lateral/depth spatial resolution for 2D / 3D dopant profile (nm)	2.2 / 2.0	1.5 / 1.4	1.0 / 1.2	
	At-line dopant profile concentration precision (across concentration range) [E]	2%	2%	2%	

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Table 101a Interconnect Metrology Technology Requirements—Near Term

Year of Production		2001	2002	2003	2004	2005	2006	2007	Driver
DRAM ½ Pitch (nm)		130	115	100	90	80	70	65	Driver
MPU / ASIC ½ Pitch (nm)		150	130	107	90	80	70	65	
MPU Printed Gate Length (nm)		90	75	65	53	45	40	35	
MPU Physical Gate Length (nm)		65	53	45	37	32	28	25	
Planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm)		25 × 32	250	250	25 × 36	200	200	25 × 40	
Measurement precision (nm)		250 ± 25			200 ± 20			175 ± 17	
Was	Measurement of deposited barrier layer at thickness (nm) /	18	15	13	11	10	9	8	MPU
	Process range ($\pm 3\sigma$) precision 1σ (nm) for P/T=0.1	10%	10%	10%	10%	10%	10%	10%	
	Require profile characterization on patterned wafers [A]	0.06	0.05	0.043	0.037	0.033	0.03	0.026	
Is	Measurement of deposited barrier layer at thickness (nm) /	18	15	13	11	10	9	8	MPU
	<u>Process range ($\pm 3\sigma$)</u>	10%	10%	10%	10%	10%	10%	10%	
	<u>precision 1s (nm) for P/T=0.1 [A]</u>	0.06	0.05	0.043	0.037	0.033	0.03	0.026	
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 μm square array		28	24	20	18	16	14	13	MPU
Was	Void size for 1 % voiding in copper lines	32.5	28.75	25	22.5	20	17.5	16.25	MPU
Is	<u>Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1 % or more of total metal level conductor volume of copper line and 5% of vias. [B]</u>	87	73	61	52	46	42	37	MPU
Was	Detection of killer pore at (nm) size	6.5	5.75	5	4.5	4	3.5	3.25	MPU
Is	<u>Detection of killer pore in ILD at (nm) size</u>	7.5	6.5	5.35	4.5	4	3.5	3.25	MPU
Measure interlevel metal insulator bulk / effective dielectric constant (k) and anisotropy on patterned structures at 5 × to 10 × local clock frequency (GHz) [B]		2.7 3.0–3.7 1.7	2.7 3.0–3.7 2.3	2.7 2.9–3.5 3.1	2.2 2.5–3.0 4	2.2 2.5–3.0 5.2	2.2 2.5–3.0 5.6	1.7 2.0–2.5 6.7	MPU

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Table 101b Interconnect Metrology Technology Requirements—Long-term

	Year of Production	2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	
	MPU / ASIC ½ Pitch (nm)	45	32	22	
	MPU Printed Gate Length (nm)	25	18	13	
	MPU Physical Gate Length (nm)	18	13	9	
	Planarity requirements: lithography field (mm × mm) / planarity for minimum interconnect CD (nm) / measurement precision	25 × 44 175 ±17	25 × 52 175 ±17	175 ±17	
Was	Measurement of deposited barrier layer at Thickness (nm) / process range (± 3σ) Precision 1σ (nm) for P/T=0.1 [A]	7 10% 0.023	5 10% 0.017	4 10% 0.013	MPU
Is	Measurement of deposited barrier layer at Thickness (nm) / process range (± 3σ) Precision 1σ (nm) for P/T=0.1 <i>Require profile characterization on patterned wafers—[A]</i>	7 10% 0.023	5 10% 0.017	4 10% 0.013	MPU
	Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% X height, 50% areal density, 500 μm square array	5	4	3	MPU
Was	Void size for 1 % voiding in copper lines	11.25	8	5.5	MPU
Is	<i>Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1 % or more of total metal level conductor volume of copper line and 5% of vias. [B]</i>	26	18	12	MPU
Was	Detection of killer pore at (nm) size	2.25	1.6	1.1	MPU
Is	<i>Detection of killer pore in ILD at (nm) size</i>	2.25	1.6	1.1	MPU
	Measure interlevel metal insulator bulk / effective dielectric constant (k) and anisotropy on patterned structures at 5 × to 10 × clock frequency (GHz) [B]	1.6 2 11.5	<1.6 1.9 19.3	1.5 1.7 28.7	MPU

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