LITHOGRAPHY

Table 56 Lithography Difficult Challenges

Five Difficult Challenges ≥ 65 nm, Through 2007	*Summary of Issues*
Optical mask fabrication with resolution enhancement techniques for ≤ 90 nm and development of post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as registration, CD control, defectivity, and 157 nm films; defect free multi-layer substrates or membranes). Development of equipment infrastructure (writers, inspection, repair, metrology) for a relatively small market.
Cost control and return on investment (ROI)	Achieving constant/improved ratio of tool cost to throughput over time Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, such as low cost masks. Achieving ROI for all segments of the industry (chipmakers, equipment and material suppliers, and infrastructure) with sufficient lifetimes for the technologies, especially single node solutions at 90 nm and below.
Process control	Development of processes to control gate linewidths to nearly 3nm, 3 σ Development of new and improved alignment and overlay control methods independent of technology option for < 25 nm overlay.
Resists for ArF and F_2	Outgassing, LER, SEM induced CD changes, etch resistance, and defects as small as 40 nm.
CaF_2	Yield, cost, quality.
Five Difficult Challenges < 65 nm, Beyond 2007	
Mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (defect-free NGL masks, such as EUV multi-layer masks or EPL membranes and stencil masks). Development of equipment infrastructure (writers, inspection of substrates, blanks and patterned masks, repair, metrology) for a relatively small market. Development of mask process control methods to achieve critical dimensions, image placement, and defect density control below the 65 nm node.
Metrology and defect inspection	Capability for measuring critical dimensions down to 9 nm and metrology for overlay down to 9 nm, and patterned wafer defect inspection for defects < 40nm.
Cost control and ROI	Achieving constant/improved ratio of tool cost to throughput over time. Development of cost-effective post-optical masks including an affordable ASIC solution, such as low cost masks. Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) with sufficient lifetimes for the technologies, especially single node solutions at 45 nm and below.
Gate CD control improvements; process control; resist materials	Development of processes to control gate CDs < 1nm (3 sigma) with appropriate line-edge roughness. Development of new and improved alignment and overlay control methods independent of technology option to < 9 nm overlay.
Tools for mass production	Post optical exposure tools capable of meeting requirements of the Roadmap.

Table 57a Lithography Technology Requirements—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM							
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
Contact in resist (nm)	**165**	**140**	**130**	**110**	**100**	**90**	**80**
Contact after etch (nm)	**150**	**130**	**115**	**100**	**90**	**80**	**70**
Overlay	**46**	**40**	**35**	**32**	**28**	**25**	**23**
CD control (3 sigma) (nm)	**15.9**	**14.1**	**12.2**	**11**	**9.8**	**8.6**	**8**
MPU							
MPU ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU gate in resist (nm)	**90**	**70**	**65**	**53**	**45**	**40**	**35**
MPU gate length after etch (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Contact in resist (nm)	**165**	**140**	**122**	**100**	**90**	**80**	**75**
Contact after etch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
Gate CD control (3 sigma) (nm)	**5.3**	**4.3**	**3.7**	**3**	**2.6**	**2.4**	**2**
ASIC/LP							
ASIC/LP ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
ASIC/LP gate in resist (nm)	**130**	**107**	**90**	**75**	**65**	**53**	**45**
ASIC/LP gate length after etch (nm)	**90**	**80**	**65**	**53**	**45**	**37**	**32**
Contact in resist (nm)	**165**	**140**	**122**	**100**	**90**	**80**	**75**
Contact after etch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
CD control (3 sigma) (nm)	**7.3**	**6.5**	**5.3**	**4.3**	**3.7**	**3**	**2.6**
Chip size (mm^2)							
DRAM, introduction	**390**	**308**	**364**	**287**	**454**	**359**	**568**
DRAM, production	**127**	**100**	**118**	**93**	**147**	**116**	**183**
MPU, high volume at introduction	**280**	**280**	**280**	**280**	**280**	**280**	**280**
MPU, high volume at production	**140**	**140**	**140**	**140**	**140**	**140**	**140**
MPU, high performance	**310**	**310**	**310**	**310**	**310**	**310**	**310**
ASIC	**800**	**800**	**572**	**572**	**572**	**572**	**572**
Minimum field area	**800**	**800**	**572**	**572**	**572**	**572**	**572**
Wafer size (diameter, mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

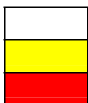


Table 57b Lithography Technology Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM			
DRAM ½ Pitch (nm)	**45**	**32**	**22**
Contact in resist (nm)	**55**	**40**	**30**
Contact after etch (m)	**50**	**35**	**25**
Overlay	**18**	**13**	**9**
CD control (3 sigma) (nm)	**5.5**	**3.9**	**2.7**
MPU			
MPU ½ Pitch (nm)	**45**	**32**	**22**
MPU gate in resist (nm)	**25**	**18**	**13**
MPU gate length after etch (nm)	**18**	**13**	**9**
Contact in resist (nm)	**50**	**37**	**27**
Contact after etch (nm)	**45**	**32**	**22**
CD control (3 sigma) (nm)	**1.5**	**1.1**	**0.7**
ASIC/LP			
ASIC/LP ½ Pitch (nm)	**45**	**32**	**22**
ASIC/LP gate in resist (nm)	**32**	**22**	**16**
ASIC/LP gate length after etch (nm)	**22**	**16**	**11**
Contact in resist (nm)	**50**	**37**	**27**
Contact after etch (nm)	**45**	**32**	**22**
CD control (3 sigma) (nm)	**1.8**	**1.3**	**0.9**
Chip size (mm^2)			
DRAM, introduction	**563**	**373**	**186**
DRAM, production	**181**	**239**	**238**
MPU, high volume at introduction	**280**	**280**	**280**
MPU, high volume at production	**140**	**140**	**140**
MPU, high performance	**310**	**310**	**310**
ASIC	**572**	**572**	**572**
Minimum field area	**572**	**572**	**572**
Wafer size (diameter, mm)	**300**	**450**	**450**

Note: The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists and masks for manufacturing must be available one year earlier. Development capability must be available 2–3 years earlier.

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 59a Optical Mask Requirements

	Year of Production	*2001*	*2002*	*2003*	*2004*		*2005*		*2006*		*2007*	
		130nm	*115nm*	*100nm*	*90nm*		*80nm*		*70nm*		*65nm*	
Was	Wafer minimum half pitch (nm) [A]	130	115	100	90	90	80	80	70	70	65	65
Is	Wafer minimum half pitch (nm) [A]	Linked to Table 57a values and cell colors										
Was	Wafer minimum line (nm, in resist)	90	75	65	53	53	45	45	40	40	35	35
Is	Wafer minimum line (nm, in resist)	Linked to Table 57a values and cell colors										
Was	Wafer minimum line (nm, Post Etch)	65	53	45	37	37	32	32	30	30	25	25
Is	Wafer minimum line (nm, Post Etch)	Linked to Table 57a values and cell colors										
Was	Overlay	45	40	35	32	32	28	28	25	25	23	23
Is	Overlay	Linked to Table 57a values and cell colors										
Was	Wafer minimum contact hole (nm, Post Etch) [A]	150	130	115	100	100	90	90	80	80	70	70
Is	Wafer minimum contact hole (nm, Post Etch) [A]	Linked to Table 57a values and cell colors										
	Magnification [B]	4	4	4	4	5	4	5	4	5	4	5
Was	Mask minimum image size (nm) [C]	360	300	260	212	265	180	225	160	200	140	175
Is	Mask minimum image size (nm) [C]	360	300	260	212	265	180	225	160	200	140	175
Was	Mask OPC feature size (nm) Clear [D]	260	230	200	180	225	160	200	140	175	130	163
Is	Mask OPC feature size (nm) Clear [D]	260	230	200	180	225	160	200	140	175	130	163
Was	Mask OPC feature size (nm) Opaque [D]	180	150	130	106	133	90	113	80	100	70	88
Is	Mask OPC feature size (nm) Opaque [D]	180	150	130	106	133	90	113	80	100	70	88

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

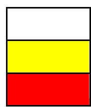
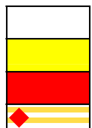


Table 59a Optical Mask Requirements (continued)

	Year of Production	*2001*	*2002*	*2003*	*2004*		*2005*		*2006*		*2007*	
		130nm	*115nm*	*100nm*	*90nm*		*80nm*		*70nm*		*65nm*	
	Image placement (nm, multi-point) [E]	27	24	21	19	24	17	21	15	19	14	17
	CD uniformity (nm, 3 sigma) [F] @	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Was	Isolated lines (MPU gates) Binary	7.4	6.1	5.1	4.2	5.3	3.7	4.6	3.4	4.3	2.5	3.1
Is	Isolated lines (MPU gates) Binary	7.4	6.1	5.1	4.2	5.3	3.7	4.6	3.4	4.3	2.5	3.1
Was	Isolated lines (MPU gates) ALT	10.4	8.5	7.2	5.9	7.4	5.1	6.4	4.8	6	4	5
Is	Isolated lines (MPU gates) ALT	10.4	8.5	7.2	5.9	7.4	5.1	6.4	4.8	6	4	5
Was	Dense lines DRAM half pitch)	10.4	9.2	8	7.2	9	6.4	8	5.6	7	4.2	5.2
Is	Dense lines DRAM half pitch)	10.4	9.2	8	7.2	9	6.4	8	5.6	7	4.2	5.2
Was	Contact/vias	8	6.9	6.1	5.3	6.7	4.8	6	4.3	5.3	3.2	4
Is	Contact/vias	8	6.9	6.1	5.3	6.7	4.8	6	4.3	5.3	3.2	4
Was	Linearity (nm) [G]	19.8	17.5	15.2	13.7	17.1	12.2	15.2	10.6	13.3	9.9	12.4
Is	Linearity (nm) [G]	19.8	17.5	15.2	13.7	17.1	12.2	15.2	10.6	13.3	9.9	12.4
	CD mean to target (nm) [H]	10.4	9.2	8	7.2	9	6.4	8	5.6	7	5.2	6.5
Was	Defect size (nm) [I] *	104	92	80	72	90	64	80	56	70	52	65
Is	Defect size (nm) [I] *	104	92	80	72	90	64	80	56	70	52	65
	Substrate form factor	152 x 152 x 6.35 mm										
	Blank Flatness (nm)	250	250	200	180	280	160	250	140	220	130	200

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known
Interim Solutions are Known



A definition of interim solutions is included in the Glossary.

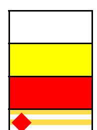
Table 59a Optical Mask Requirements (continued)

	Year of Production	2001	2002	2003	2004		2005		2006		2007	
		130nm	115nm	100nm	90nm		80nm		70nm		65nm	
	Transmission uniformity to mask(pellicle and clear feature) (+-% 3sigma)	1	1	1	1	1	1	1	1	1	1	1
Was	Data volume (GB) [J]	64	96	144	216	216	324	324	486	486	729	729
Is	Data volume (GB) [J]	64	96	144	216	216	324	324	486	486	729	729
	Mask design grid (nm) [K]	8	8	4	4	5	4	5	4	5	4	5
	Attenuated PSM transmission mean deviation from target (+/- % of target) [L]	5	5	5	5	5	5	5	4	4	4	4
	Attenuated PSM transmission uniformity (+/-% of target) [M]	4	4	4	4	4	4	4	4	4	4	4
	Attenuated PSM phase mean deviation from 180o (+/- degree)	4	4	3	3	3	3	3	3	3	3	3
Was	Alternating PSM phase mean deviation from 180o (+/- degree)	2	2	2	2	2	2	2	1	1	1	1
Is	Alternating PSM phase mean deviation from 180o (+/- degree)	2	2	2	2	2	2	2	1	1	1	1
Was	Alternating PSM phase uniformity (+/- degree)	2	2	2	2	2	2	2	1	1	1	1
Is	Alternating PSM phase uniformity (+/- degree)	2	2	2	2	2	2	2	1	1	1	1
Was	Mask materials and substrates	**Absorber on fused silica, except for 157nm optical which will be absorber on modified fused silica square with pellicles** ***157nm has no known cost-effective pellicle solution***										
Is	Mask materials and substrates	**Absorber on fused silica, except for 157nm optical which will be absorber on modified fused silica square**										
Is	*Strategy for protecting mask from defects*	***Pellicle for optical masks down to 193nm.***					***Modified fused silica pellicles might be feasible for 157-nm scanners, and removable pellicles might be useful for small lot production. Organic membrane pellicles are under research.***					
	(Exposure tool dependent)	**Primary PSM choices are attenuated shifter and alternating aperture**										

The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.

**180 degree phase defects are 70% of number shown*

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known
Interim Solutions are Known

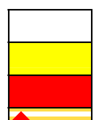


A definition of interim solutions is included in the Glossary.

Table 59b EUVL Mask Requirements

	Year of Production	*2006 70nm*	*2007 65nm*	*2010 45nm*	***2013 32nm***	*2016 22nm*
Was	Wafer minimum half pitch (nm) [A]	70	65	45	32	22
Is	Wafer minimum half pitch (nm) [A]	Linked to Table 57b values and cell colors				
Was	Wafer minimum line (nm, in resist)	40	35	25	18	13
Is	Wafer minimum line (nm, in resist)	Linked to Table 57b values and cell colors				
Was	Wafer minimum line (nm, Post Etch)	30	25	18	13	9
Is	Wafer minimum line (nm, Post Etch)	Linked to Table 57b values and cell colors				
Was	Overlay	25	23	18	13	9
Is	Overlay	Linked to Table 57b values and cell colors				
Was	Wafer minimum contact hole (nm, after etch)	80	70	50	35	25
Is	Wafer minimum contact hole (nm, after etch)	Linked to Table 57b values and cell colors				
	Generic Mask Requirements					
	Magnification [B]	4	4	4	4	4
	Mask minimum image size (nm) [C]	160	140	100	72	52
	Image placement (nm, multi-point) [D]	15	14	11	8	6
	CD Uniformity (nm, 3 sigma) [E]					
	Isolated lines (MPU gates)	4.5	4	2.5	2	1
Was	Dense lines DRAM (half pitch)	11	10	7	5	3.5
Is	Dense lines DRAM (half pitch)	11	10	7	5	3.5
Was	Contact/vias	12.5	11	8	5.5	4
Is	Contact/vias	12.5	11	8	5.5	4
Was	Linearity (nm) [F]	11	10	7	5	3.5
Is	Linearity (nm) [F]	11	10	7	5	3.5
	CD mean to target (nm) [G]	5.5	5	3.5	2.5	1.5
	Defect size (nm) [H]	55	50	35	25	15
	Data volume (GB) [I]	324	486	1644	5550	18736
	Mask design grid (nm) [J]	4	4	4	4	4

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known
Interim Solutions are Known

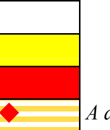


A definition of interim solutions is included in the Glossary.

Table 59b EUVL Mask Requirements (continued)

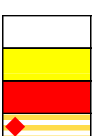
	Year of Production	*2006 70nm*	*2007 65nm*	*2010 45nm*	***2013 32nm***	*2016 22nm*
	EUVL-specific Mask Requirements					
	Substrate defect size (nm) [K]	39	37	32	27	23
Was	Mean peak reflectivity	65%	65%	66%	67%	67%
Is	Mean peak reflectivity	65%	65%	66%	67%	67%
	Relative reflectivity uniformity of the mask (% 3sigma) [L]	1.50%	1.30%	0.90%	0.70%	0.50%
	Peak reflectivity uniformity (% 3sigma absolute)	0.69%	0.61%	0.42%	0.33%	0.24%
Was	Reflected centroid wavelength uniformity (nm 3sigma) [M]	0.06	0.05	0.05	0.04	0.03
Is	Reflected centroid wavelength uniformity (nm 3sigma) [M]	0.06	0.05	0.05	0.04	0.03
	Minimum absorber sidewall angle (degrees)	85	85	85	85	85
	Absorber sidewall angle tolerance (± degrees)	1	1	0.75	0.5	0.5
	Absorber LER (3sigma nm) [N]	5	4	3	3	3
	Mask substrate flatness (nm peak-to-valley) [O]	80	75	50	45	30
Was	Maximum aspect ratio of absorber stack	1	1.1	1.3	1.5	1.7
Is	Maximum aspect ratio of absorber stack	1	1.1	1.3	1.5	1.7
	Substrate form factor	152 × 152 × 6.35 mm				
	Strategy for protecting mask from defects	Removable pellicle and thermophoresis during exposure				

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known
Interim Solutions are Known



A definition of interim solutions is included in the Glossary.

Table 59c EPL Mask Requirements

	Year of Production	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
	Wafer minimum half pitch (nm) [A]	70	65	45	32	22
	Wafer minimum line (nm, in resist)	40	35	25	18	13
	Wafer minimum line (nm, Post Etch)	30	25	18	13	9
	Overlay	25	23	18	13	9
	Wafer minimum contact hole (nm, after etch)	80	70	50	35	25
	Magnification [B]	4	4	4	4	4
	Mask minimum image size (nm) [C]	112	98	70	50	36
	Non-linear image placement error in sub-field (nm, multi-point) [D]	11	10	7	5	3
	Generic mask requirements					
Add	CD Uniformity (nm, 3 sigma) [E]					
	Isolated lines (MPU gates) [E]	4.5	4	2.5	2	1
Was	Dense lines DRAM half pitch) [E]	11.5	10.5	7.5	5	3.5
Is	Dense lines DRAM half pitch) [E]	11.5	10.5	7.5	5	3.5
Was	Contact/vias [E]	13	11.5	8	5.5	4
Is	Contact/vias [E]	13	11.5	8	5.5	4
Was	Linearity (nm) [F]	11	10	7	5	3.5
Is	Linearity (nm) [F]	11	 10	7	5	3.5
	CD mean to target (nm) [G]	6	5.5	4	2.5	1.5
	Pattern corner rounding (nm)	45	40	28	18	15
	Defect size (nm) [H]	55	50	35	25	15
	Data volume (GB) [I]	324	486	1644	5550	18736
	Mask design grid (nm) [J]	4	4	4	4	4

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known
Interim Solutions are Known — *A definition of interim solutions is included in the Glossary.*

Table 59c EPL Mask Requirements (continued)

Year of Production	*2006 70nm*		*2007 65nm*		*2010 45nm*		*2013 32nm*		*2016 22nm*	
EPL-specific mask requirements										
Mask type	***Membrane [N]***	***Stencil [O]***	***Membrane***	***Stencil***	***Membrane***	***Stencil***	***Membrane***	***Stencil***	***Membrane***	***Stencil***
Clear area transmission factor [K]	**50%**	**100%**	**50%**	**100%**	**50%**	**100%**	**70%**	**100%**	**70%**	**100%**
Membrane thickness uniformity (3 sigma %) [L]	**1.00%**	**N/A**	**1.00%**	**N/A**	**1.00%**	**N/A**	**1.00%**	**N/A**	**1.00%**	**N/A**
Pattern sidewall angle (degrees)	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**
Pattern sidewall angle tolerance (+ degrees)	**0.2**		**0.2**		**0.2**		**0.2**		**0.2**	
Scatterer/stencil LER (3sigma nm) [M]	**5**		**4**		**3**		**3**		**3**	
Mask substrate flatness (micron peak-to-valley)	**10**		**10**		**5**		**5**		**4**	
Mask flatness within a sub-field (micron peak-to-valley)	**1**		**1**		**1**		**1**		**1**	
Maximum mask resistivity (ohm-cm)	**20**									
Substrate form factor	**200 mm diameter, 0.725 mm thick**									
Strategy for protecting mask from defects	**Periodic inspection and cleaning as needed**									

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
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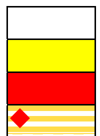
Interim Solutions are Known



A definition of interim solutions is included in the Glossary.

Notes for Table 59b—EUV Mask requirements:

	EUVL masks are patterned absorber layers on top of multilayers that are deposited on low thermal expansion material substrates.
	[A] Wafer Minimum Feature Size-Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)
	[B] Magnification-Lithography tool reduction ratio, N:1
	[C] Mask Minimum Image Size-The nominal mask size of the smallest primary feature to be transferred to the wafer (Commonly equivalent to wafer minimum feature size times the reduction ratio.)
	[D] Image Placement-The maximum component deviation (x or y) of the array of the images centerline relative to a defined reference grid.
	[E] CD Uniformity-The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the Mask Feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt(AREA) - sqrt(TARGET AREA)
	[F] Linearity-Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than half the primary feature size and less than five times the primary feature size
	[G] CD Mean to Target-The maximum difference between the average of the measured feature sizes and the intended feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.
	[H] Defect Size-A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The Mask Defect Size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
	[I] Date Volume-This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.
	[J] Mask Design Grid-Wafer design grid times the mask magnification.
	[K] Substrate Defect Size-the minimum diameter spherical defect on the substrate beneath the multilayers that causes an unacceptable linewidth change in the printed image. Substrate defects might cause phase errors in the printed image and are the smallest mask blank defects that would unacceptably change the printed image.
	[L] Relative reflectivity uniformity includes errors in effective reflectivity due to peak reflectivity uniformity, centroid wavelength uniformity, and centered wavelength accuracy.
	[M] Includes variation in centroid wavelength over the mask area and mismatching of the average wavelength to the wavelength of the exposure tool optics.
	[N] Line edge roughness (LER) is defined a roughness 3sigma one-sided for spatial period < minimum linewidth
Was	*[O] Mask Substrate Flatness-Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge and or bow that are compensable by the mask mounting and leveling method in the exposure tool.*
Is	*[O] Mask Substrate Flatness-Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge and or bow that are compensable by the mask mounting and leveling method in the exposure tool.* ***This flatness requirement applies to each of the front and backsides individually.***