FRONT END PROCESSES

Table 48 Front End Processes Difficult Challenges

	MPU/ASIC Physical Gate Length ≥ 25 nm, Through 2007	*Summary of Issues*
	New gate stack processes and materials	Extension of oxy-nitride gate dielectric materials to < 1.0nm E.O.T for high performance MOSFETs, consistent with device reliability requirements Introduction and process integration of high κ gate stack materials and processes for low operating and low standby power MOSFETs Control of boron penetration from doped polysilicon gate electrode Minimized depletion of dual-doped polysilicon electrodes Possible introduction of dual-metal gate electrodes with appropriate work function (toward end of period) Metrology issues associated with gate dielectric film thickness and stack electrical and materials characterization
Was	Critical dimension and effective channel length (L_{eff}) control	Control of gate etch process that yield a physical gate length that is smaller than the feature size printed in the resist, while maintaining <10% overall 3-sigma control of the combined lithography and etch processes Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns Control of self-aligned doping processes and thermal activation budgets to achieve ~15% 3σ L_{eff} control Maintenance of CD and profile Control throughout the transition to new gate stack materials and processes CD and etch metrology
Is	Critical dimension and effective channel length (L_{eff}) control	Control of gate etch process that yield a physical gate length that is smaller than the feature size printed in the resist, while maintaining <10% overall 3-sigma control of the combined lithography and etch processes Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns Control of self-aligned doping processes and thermal activation budgets to achieve ~~~15% 3σ~~ L_{eff} control Maintenance of CD and profile Control throughout the transition to new gate stack materials and processes CD and etch metrology
	CMOS integration of new memory materials and processes	Development and introduction of very high κ DRAM capacitor dielectric layers Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal Integration and scaling of FeRAM ferroelectric materials Scaling of Flash inter-poly and tunnel dielectric layers may require high κ Limited temperature stability of high κ and ferroelectric materials challenges CMOS integration
	Surfaces and interfaces: structure, composition and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface Interface control for DRAM capacitor structures Maintenance of surface and interface integrity through full-flow CMOS processing Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces
	Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~16–20% of ideal channel resistance ($=V_{dd}/I_{on}$) Control of parasitic capacitance to achieve less than ~19–27% of gate capacitance, consistent with acceptable Ion and minimum short channel effect Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes Formation of continuous self-aligned silicide contacts over shallow source and drain regions Metrology issues associated with 2D dopant profiling

Table 48 Front End Processes Difficult Challenges(continued)

MPU/ASIC physical Gate Length <25 nm, Beyond 2007	*Issues*
Continued scaling of planar CMOS devices	Higher κ gate dielectric materials including temperature constraints Metal gate electrodes with appropriate work function Sheet resistance of clad junctions Enhanced channel mobility, e.g., strained layers CD and L_{eff} control Chemical, electrical and structural characterization
Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices may be needed as early as 2007 Selection and characterization of optimum device types CMOS integration with other devices, including planar MOSFETs Introduction, characterization and production hardening of new FEP unit processes Device and FEP process metrology Increased funding of long term research
Starting silicon material alternatives beyond 300 mm	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm Economies of the incumbent Czochralski crystal pulling, wafer slicing and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon
New memory storage cells, storage devices, and memory architectures	Scaling of DRAM storage capacitor beyond $6F^2$ and ultimately beyond $4F^2$ Further scaling of Flash memory interpoly and tunnel oxide thickness FeRAM storage cell scaling Introduction of new memory types and storage concepts
Surface and interface structural, contamination, and compositional control	Achievement and maintenance of structural, chemical and contamination control of surfaces and interfaces, that may be horizontally or vertically oriented relative to the chip surface Metrology and characterization of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface

Corrected Starting Materials Requirements Cell Key for Table 49a and b

Starting Materials Requirements Cell Key

Technology requirements value and supplier manufacturing capability	
Criticality of requirement to IC wafer user	Metrology readiness capability

Color-Code Key

Technology requirements value and supplier manufacturing capability cells and metrology readiness capability cells		Criticality of requirement to IC wafer user cells
White-Manufacturable Solutions Exist and Are Being Optimized	(white)	White-Maintenance Item
Yellow-Manufacturable Solutions are Known	(yellow)	Yellow-Process Margin Iimprovement
Red-Manufacturable Solutions are NOT Known	(red)	Red-"Showstopper"

Strained Si:Ge on SOI

Recommend addition of comment below to 2002 ITRS update as follows:

Strained silicon films to enhance carrier mobility typically are formed on relaxed Si_xGe_{1-x} for NMOSFETS. However, for PMOSFET applications, strained Si may be fabricated on strained Si_xGe_{1-x} or strained Si_xGe_{1-x} may be utilized in place of the strained Si on strained Si_xGe_{1-x} for the channel region. Both SOI-like structures and bulk silicon may be utilized, although the former appears to be preferred for enhanced device performance.

Starting Materials sub TWG will address strained Si:Ge in further detail in the 2003 ITRS revision.

Table 49a Starting Materials Technology Requirements—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*DRIVER*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*D ½*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*M*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*M*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*M*
DRAM Total Chip Area (mm^2)	**127**	**100**	**118**	**93**	**147**	**116**	**183**	*D ½*
DRAM Active Transistor Area (mm^2)	**55.3**	**36.9**	**59.0**	**42.3**	**73.1**	**53.2**	**89.9**	*D ½*
MPU High-Performance Total Chip Area (mm^2)	**310**	**310**	**310**	**310**	**310**	**310**	**310**	*M*
MPU High-Performance Active Transistor Area (mm^2)	**28.7**	**28.2**	**27.7**	**27.2**	**26.8**	**26.8**	**26.8**	*M*
*General Characteristics * (99% Chip Yield) [A,B,C]*								
Wafer diameter (mm) **	**300*** **	**300*** **	**300*** **	**300**	**300**	**300**	**300**	*D ½, M*
Edge exclusion (mm) ****	**3**	**3**	**2**	**2**	**2**	**2**	**2**	*D ½, M*
Front surface particle size (nm), latex sphere equivalent [D]	**≥ 90**	**≥ 90**	**≥ 90**	**≥45**	**≥40**	**≥35**	**≥33**	*D ½, M*
Particles (cm^{-2}) [E]	**≤ 0.18**	**≤ 0.27**	**≤ 0.17**	**≤ 0.24**	**≤ 0.14**	**≤ 0.19**	**≤ 0.11**	*D ½*
Particles (#/wf)	**≤ 123**	**≤ 185**	**≤ 117**	**≤ 164**	**≤ 95**	**≤ 130**	**≤ 77**	*D ½*
Critical surface metals (at/cm^2) [F]	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	*D ½, M*
Site flatness (nm) [G]	**≤ 130**	**≤ 115**	**≤ 100**	**≤ 90**	**≤ 80**	**≤ 70**	**≤ 65**	*D ½, M*
*Polished Wafer * (99% Chip Yield)*								
The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D,E]								
Total bulk Fe (at/cm^3) [H]	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	*D ½, M*
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [I]	**≤ 2.8**	**≤ 2.3**	**≤ 1.9**	**≤ 1.6**	**≤ 1.4**	**≤1.1**	**≤ 1.0**	*D ½*
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [I]	**≤ 1.0**	**≤ 0.8**	**≤ 0.6**	**≤ 0.5**	**≤ 0.4**	**≤ 0.3**	**≤ 0.3**	*M*
*Epitaxial Wafer * (99% Chip Yield)*								
Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Structural Defects, Small Structural Defects and Particles (see General Characteristics) [J,K]								
Large structural epi defects (DRAM) (cm^{-2}) [L]	**≤ 0.008**	**≤ 0.010**	**≤ 0.009**	**≤ 0.011**	**≤ 0.007**	**≤ 0.009**	**≤ 0.005**	*D ½*
Large structural epi defects (MPU) (cm^{-2}) [L]	**≤ 0.003**	**≤ 0.003**	**≤ 0.003**	**≤ 0.003**	**≤ 0.003**	**≤ 0.003**	**≤ 0.003**	*M*
Small structural epi defects (DRAM) (cm^{-2}) [M]	**≤ 0.016**	**≤ 0.020**	**≤ 0.017**	**≤ 0.022**	**≤ 0.014**	**≤ 0.017**	**≤ 0.011**	*D ½*
Small structural epi defects (MPU) (cm^{-2}) [M]	**≤ 0.006**	**≤ 0.006**	**≤ 0.006**	**≤ 0.006**	**≤ 0.006**	**≤ 0.006**	**≤ 0.006**	*M*

Table Cell Key Legend

Technology requirements value and supplier manufacturing capability	
Criticality of requirement to IC wafer user	**Metrology readiness capability**

Color-Code Key

Technology requirements value and supplier manufacturing capability cells and metrology readiness capability cells		*Criticality of requirement to IC wafer user cells*
White-Manufacturable Solutions Exist and Are Being Optimized		*White-Maintenance Item*
Yellow-Manufacturable Solutions are Known		*Yellow-Process Margin Iimprovement*
Red-Manufacturable Solutions are NOT Known		*Red-"Showstopper"*

Table 49a Starting Materials Technology Requirement—-Near-term (continued)

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*DRIVER*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*D ½*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*M*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*M*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*M*
DRAM Total Chip Area (mm^2)	**127**	**100**	**118**	**93**	**147**	**116**	**183**	***D ½***
DRAM Active Transistor Area (mm^2)	**55.3**	**36.9**	**59.0**	**42.3**	**73.1**	**53.2**	**89.9**	***D ½***
MPU High-Performance Total Chip Area (mm^2)	**310**	**310**	**310**	**310**	**310**	**310**	**310**	***M***
MPU High-Performance Active Transistor Area (mm^2)	**28.7**	**28.2**	**27.7**	**27.2**	**26.8**	**26.8**	**26.8**	***M***
Silicon-On-Insulator Wafer (95% Chip Yield)*								
Wafer diameter (mm) **	**200**	**300*****	**300*****	**300**	**300**	**300**	**300**	*D ½, M*
Silicon final device layer thickness (Partially Depleted) (tolerance ± 5%) (nm) [N]	**98–163**	**80–133**	**68–113**	**56–93**	**48–80**	**42–70**	**38–63**	*M*
Silicon final device layer thickness (Fully Depleted) (tolerance ± 5%) (nm) [O]	**20–33**	**16–27**	**14–23**	**11–19**	**10–16**	**8–14**	**8–13**	*M*
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%) (nm) [P]	**49–81**	**40–66**	**34–56**	**28–46**	**24–40**	**21–35**	**19–31**	*M*
D_{LASOI}, Large area SOI wafer defects (DRAM) (cm^{-2}) [Q]	**≤ 0.040**	**≤ 0.051**	**≤ 0.043**	**≤ 0.055**	**≤ 0.035**	**≤ 0.044**	**≤ 0.028**	*D ½*
D_{LASOI}, Large area SOI wafer defects (MPU) (cm^{-2}) [Q]	**≤ 0.017**	**≤ 0.017**	**≤ 0.017**	**≤ 0.017**	**≤ 0.017**	**≤ 0.017**	**≤ 0.017**	*M*
D_{SASOI}, Small area SOI wafer defects (DRAM) (cm^{-2}) [R]	**≤ 0.464**	**≤ 0.695**	**≤ 0.434**	**≤ 0.607**	**≤ 0.351**	**≤ 0.482**	**≤ 0.285**	*D ½*
D_{SASOI}, Small area SOI wafer defects (MPU) (cm^{-2}) [R]	**≤ 0.894**	**≤ 0.910**	**≤ 0.926**	**≤ 0.942**	**≤ 0.956**	**≤ 0.956**	**≤ 0.956**	*M*
D_{EC}, Extended Crystal Defects (MPU) (cm^{-2}) [S]	**1.8 E5**	**1.8 E5**	**1.9 E5**	**1.9 E5**	**1.9 E5**	**1.9 E5**	**1.9 E5**	*M*

Table Cell Key Legend

Technology requirements value and supplier manufacturing capability	
Criticality of requirement to IC wafer user	***Metrology readiness capability***

Color-Code Key

Technology requirements value and supplier manufacturing capability cells and metrology readiness capability cells		*Criticality of requirement to IC wafer user cells*
White-Manufacturable Solutions Exist and Are Being Optimized		*White-Maintenance Item*
Yellow-Manufacturable Solutions are Known		*Yellow-Process Margin Iimprovement*
Red-Manufacturable Solutions are NOT Known		*Red-"Showstopper"*

Table 49b Starting Materials Technology Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*	*Driver*
DRAM ½ Pitch (nm)	*45*	*32*	*22*	*D ½*
MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*	*M*
MPU Printed Gate Length (nm)	*25*	*18*	*13*	*M*
MPU Physical Gate Length (nm)	*18*	*13*	*9*	*M*
DRAM Total Chip Area (mm^2)	**181**	**239**	**238**	*D ½*
DRAM Active Transistor Area (mm^2)	**89.5**	**146.9**	**166.1**	*D ½*
MPU High-Performance Total Chip Area (mm^2)	**310**	**310**	**310**	*M*
MPU High-Performance Active Transistor Area (mm^2)	**26.8**	**26.8**	**26.8**	*M*
*General Characteristics * (99% Chip Yield) [A,B,C]*				
Wafer diameter (mm) **	**300**	**300*******	**450**	*D ½,M*
Edge exclusion (mm) ****	**2**	**2**	**2**	*D ½,M*
Front surface particle size (nm), latex sphere equivalent [D]	**≥ 23**	**≥ 16**	**≥ 11**	*D ½*
Particles (cm^{-2})[E]	**≤ 0.11**	**≤ 0.07**	**≤ 0.06**	*D ½*
Particles (#/wf)	**≤ 77**	**≤ 47**	**≤ 95**	*D ½*
Critical surface metals (at/cm^2) [F]	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	*D ½,M*
Site flatness (nm) [G]	**≤ 45**	**≤ 32**	**≤ 22**	*D ½,M*
*Polished Wafer * (99% Chip Yield)*				
The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D,E]				
Total bulk Fe (at/cm^3) [H]	**≤ 1 E10**	**≤ 1 E10**	**≤ 1 E10**	*D ½,M*
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [I]	**≤0.6**	**≤ 0.4**	**≤ 0.2**	*D ½*
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [I]	**≤ 0.2**	**≤ 0.1**	**≤ 0.1**	*M*
*Epitaxial Wafer * (99% Chip Yield)*				
Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Structural Defects, Small Structural Defects and Particles (see General Characteristics) [J,K]				
Large structural epi defects (DRAM) (cm^{-2}) [L]	**≤ 0.006**	**≤ 0.004**	**≤ 0.004**	*D ½*
Large structural epi defects (MPU) (cm^{-2}) [L]	**≤ 0.003**	**≤ 0.003**	**≤ 0.003**	*M*
Small structural epi defects (DRAM) (cm^{-2}) [M]	**≤ 0.011**	**≤ 0.008**	**≤ 0.008**	*D ½*
Small structural epi defects (MPU) (cm^{-2}) [M]	**≤ 0.006**	**≤ 0.006**	**≤ 0.006**	*M*

Table Cell Key Legend

Technology requirements value and supplier manufacturing capability	
Criticality of requirement to IC wafer user	Metrology readiness capability

Color-Code Key

Technology requirements value and supplier manufacturing capability cells and metrology readiness capability cells		*Criticality of requirement to IC wafer user cells*
White-Manufacturable Solutions Exist and Are Being Optimized		*White-Maintenance Item*
Yellow-Manufacturable Solutions are Known		*Yellow-Process Margin Iimprovement*
Red-Manufacturable Solutions are NOT Known		*Red-"Showstopper"*

Table 49b Starting Materials Technology Requirements—Long-term (continued)

Year of Production	*2010*	*2013*	*2016*	*Driver*
DRAM ½ Pitch (nm)	*45*	*32*	*22*	*D ½*
MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*	*M*
MPU Printed Gate Length (nm)	*25*	*18*	*13*	*M*
MPU Physical Gate Length (nm)	*18*	*13*	*9*	*M*
DRAM Total Chip Area (mm^2)	**181**	**239**	**238**	*D ½*
DRAM Active Transistor Area (mm^2)	**89.5**	**146.9**	**166.1**	*D ½*
MPU High-Performance Total Chip Area (mm^2)	**310**	**310**	**310**	*M*
MPU High-Performance Active Transistor Area (mm^2)	**26.8**	**26.8**	**26.8**	*M*
Silicon-On-Insulator Wafer (95% Chip Yield)*				
Wafer diameter (mm)	**300**	**300*******	**450**	*D ½, M*
Silicon final device layer thickness (Partially Depleted) (tolerance ± 5%) (nm) [N]	**27–45**	**20–33**	**14–23**	*M*
Silicon final device layer thickness (Fully Depleted) (tolerance ± 5%) (nm) [O]	**5–9**	**4–7**	**3–5**	*M*
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%) (nm) [P]	**14–23**	**10–16**	**7–11**	*M*
D_{LASOI}, Large area SOI wafer defects (DRAM) (cm^{-2}) [Q]	**≤ 0.028**	**≤ 0.021**	**≤ 0.022**	*D ½*
D_{LASOI}, Large area SOI wafer defects (MPU) (cm^{-2}) [Q]	**≤ 0.017**	**≤ 0.017**	**≤ 0.017**	*M*
D_{SASOI}, Small area SOI wafer defects (DRAM) (cm^{-2}) [R]	**≤ 0.287**	**≤ 0.175**	**≤ 0.154**	*D ½*
D_{SASOI}, Small area SOI wafer defects (MPU) (cm^{-2}) [R]	**≤ 0.956**	**≤ 0.956**	**≤ 0.956**	*M*
D_{EC}, Extended Crystal Defects (MPU) (cm^{-2}) [S]	**1.9 E5**	**1.9 E5**	**1.9 E5**	*M*

Table Cell Key Legend

Technology requirements value and supplier manufacturing capability	
Criticality of requirement to IC wafer user	**Metrology readiness capability**

Color-Code Key

Technology requirements value and supplier manufacturing capability cells and metrology readiness capability cells		*Criticality of requirement to IC wafer user cells*
White-Manufacturable Solutions Exist and Are Being Optimized		*White-Maintenance Item*
Yellow-Manufacturable Solutions are Known		*Yellow-Process Margin Iimprovement*
Red-Manufacturable Solutions are NOT Known		*Red-"Showstopper"*

Table 50a Surface Preparation Technology Requirements—Near-term*

	Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	D ½
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	M
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	M
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	M
	Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**D ½, M**
Was	*Wafer edge exclusion (mm)*	**3**	**3**	**1**	**1**	**1**	**1**	**1**	**D ½, M**
Is	*Wafer edge exclusion (mm)*	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**D ½, M**
	Front surface particles								
	Critical Particle Size (nm) [A]	**65**	**58**	**50**	**45**	**40**	**35**	**33**	D ½
	Particles (cm^{-2}) [B]	**0.091**	**0.136**	**0.085**	**0.119**	**0.069**	**0.094**	**0.056**	D ½
Was	Particles (#/wafer) [C]	**63**	**94**	**60**	**83**	**48**	**66**	**39**	D ½
Is	Particles (#/wafer) [C]	**62**	**92**	**59**	**82**	**47**	**65**	**38**	D ½
	Back surface particle size (nm), latex sphere equivalent [D]	**250**	**200**	**200**	**200**	**200**	**200**	**200**	D ½, M
	Particles (cm^{-2}) [E]	**0.68**	**0.68**	**0.68**	**0.68**	**0.68**	**0.68**	**0.68**	MPU
	Particles (#/wafer) [C]	**468**	**468**	**468**	**468**	**468**	**468**	**468**	MPU
	Critical GOI surface metals (E+9 ions/cm^2) [F]	**5**	**5**	**5**	**5**	**5**	**5**	**5**	MPU
	Critical Other surface metals (E+10 ions/cm^2) [F]	**1**	**1**	**1**	**1**	**1**	**1**	**1**	MPU
	Mobile ions (E+10 ions/cm^2) [G]	**1.5**	**2.1**	**2.7**	**2.5**	**3.1**	**2.6**	**2.8**	D ½
	Residual interface carbon contamination (E+13 C at/cm^2) [H]	**2.6**	**2.1**	**1.8**	**1.5**	**1.3**	**1.1**	**1**	LOP
	AFM Surface Roughness nm [I]	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	D ½, M
	Water Marks (#/wafer) [J]	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	D ½
Was	*Residual interfacial oxygen (O at/cm^2) [K]*	**<1 E14**	**<1 E14**	**<1 E14**	**<1 E14**	**<1 E14**	**<1 E14**	**<1 E14**	D ½, M
Is	*Residual interfacial oxygen (O at/cm^2) [K]*	**<1 E14**	**<1 E13**	**<1 E13**	**<1 E13**	**<1 E13**	**<1 E13**	**<1 E13**	D ½, M

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

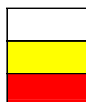
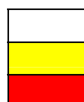


Table 50b Surface Preparation Technology Requirements—Long-term*

	Year of Production	2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	D ½
	MPU / ASIC ½ Pitch (nm)	50	35	25	M
	MPU Printed Gate Length (nm)	25	18	13	M
	MPU Physical Gate Length (nm)	18	13	9	M
	Wafer diameter (mm)	300	300	450	D ½, M
Was	Wafer edge exclusion (mm)	1	1	1	D ½, M
Is	Wafer edge exclusion (mm)	2	2	2	D ½, M
	Front surface particle				
	Critical Particle Size (nm) [A])	23	16	11	D ½
	Particles (cm^{-2}) [B]	0.056	0.034	0.03	D ½
	Particles (#/wafer) [C]	39	24	48	D ½
	Back surface particle size (nm), latex sphere equivalent [D]	200	200	200	D ½, M
	Particles (cm^{-2}) [E]	0.68	0.68	0.68	MPU
Was	Particles (#/wafer) [F]	468	468	468	D ½
Is	Particles (#/wafer) [C]	468	468	468	D ½
Was	Critical GOI surface metals (E+9 ions/cm^2) [G]	5	5	5	MPU
Is	Critical GOI surface metals (E+9 ions/cm^2) [F]	5	5	5	MPU
Was	Critical Other surface metals (E+10 ions/cm^2) [G])	5	5	5	MPU
Is	Critical Other surface metals (E+10 ions/cm^2) [F])	5	5	5	MPU
Was	Mobile ions (E+10 ions/cm^2) [H]	3.12	3.36	3.48	D ½
Is	Mobile ions (E+10 ions/cm^2) [G]	3.12	3.36	3.48	D ½
Was	Organic contamination (E+13 C at/cm^2)[I]	0.73	0.53	0.37	LOP
Is	Organic contamination (E+13 C at/cm^2)[H]	0.73	0.53	0.37	LOP
Was	Surface Roughness [J]	0.2	0.2	0.2	D ½, M
Is	Surface Roughness [I]	0.2	0.2	0.2	D ½, M
Was	Water Marks (#/wafer) [K]	<1	<1	<1	D ½
Is	Water Marks (#/wafer) [J]	<1	<1	<1	D ½
Was	Surface Oxygen (O at/cm^2) [L]	<1 E12	<1 E12	<1 E12	D ½, M
Is	Surface Oxygen (O at/cm^2) [K]	<1 E12	<1 E12	<1 E12	D ½, M

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



Notes for Tables 50a and b

(A) The critical particle size St = 1/2 DRAM 1/2 pitch.

Was	(B) $Y=0.99=\exp[-D_pR_pTA(CD)^2]$. For DRAM, this version replaces $TA(CD)^2$ with the effective chip area, $A_{eff}=2.5F^2T+(1-F^2T/A_{chip})*0.6A_{chip}$. The kill factor, R_p, is taken as 0.2. $D_p=-\ln(0.99)/[R_pTA(CD)^2]$ for DRAMs and $D_p= -\ln(0.99)/[R_pTA(GL)^2]$ for MPUs. If a different critical Particle size (Dx) is used for measurement purposes then D_p should be adjusted by $(Dx/.5CD)^2$.
Is	(B) $Y=0.99=\exp[-D_pR_pA_{eff}]$. For DRAM, $A_{eff}=2.5F^2T+(1-aF^2T/A_{chip})*0.6A_{chip}$. Where F is the minimum feature size (CD), a is the cell fill factor (see Table 52), T is the number of transistors per chip (see Table 1c) and A_{chip} is the chip size (see Table 1c). For MPUs, $A_{eff}=aT(GL)^2$, where GL is the gate length and a and T are specified for MPUs. The kill factor, R_p, is taken as 0.2. $D_p=-\ln(0.99)/[R_pA_{eff}]$. If a different critical Particle size (Dx) is used for measurement purposes then D_p should be adjusted by $(Dx/.5CD)^2$. Note that the year-to-year value for D_p does not always decrease because D_p is not only inversely proportional to T, which increases each year, but is also inversely proportional to a and F, which are decreasing year-to-year, and A_{chip} which moves up and down.
Was	(C) To obtain these values, the allowable particle density is multiplied by the fixed quality area $[DW=DP_p(R_{wafer}\text{-}ee)2]$, and rounded to the nearest whole number.
Is	(C) To obtain these values, the allowable particle density is multiplied by the fixed quality area $[D_W= D_p(3.14159)(R_{wafer}\text{-}ee)^2]$, and rounded to the nearest whole number.
Was	(D) The critical particle size is taken as the allowable step height which raises the surface out of the lithographic plane of focus. The critical size is based the budgeted portion of the total allowable DOP variation.
Is	(D) The critical particle size is taken as the allowable step height which raises the surface out of the lithographic plane of focus. The critical size is based the budgeted portion of the total allowable DOF variation.

(E) Backside particles are modeled for 99% Yield by $Y=\exp[-DpRpA_{eff}]$ (1), Rp = 1.0 and $A_{eff} = A_{chip} \times 0.03 \times 0.8$, where 0.03 corresponds to only 3% of the back side of the chip area touches the chuck and 0.8 corresponds to only 80% of the effective chip area is degraded by effects of the back-surface particle on the front-surface defocus effect. $Dp = -\ln(.99)/.03*.8*A_{chip}$.

(F) In past roadmaps, metal contamination targets have been based on an empirically derived model predicting failure due to metal contamination as a function of gate oxide thickness. However, the oxides used in the experiments from which this model was derived were far thicker than gate oxide thicknesses used today. More recent data suggest an updated approach is appropriate. The metals are empirically grouped into three classes [1], [2]: (a) Mobile metals which may be easily cleaned such as Na and K and may be modeled by taking the flat-band shift of a capacitance-voltage (CV) test less than or equal to 50 mV; (b) metals which dissolve in silicon or form silicides such as Fe, Ni, Cu, Cr, Co, and Pt; and (c) major gate-oxide-integrity (GOI) killers such as Ca. Targets for mobile ions are based on allowable threshold voltage shift from a CV test. Current targets for GOI "killers" and other metals are based on empirical data. For extrapolation to future years, there may be reason to predict less stringent targets because effects should scale with respect to physical dielectric thickness (not EOT) which will increase upon introduction of high-k gate dielectrics. However, in the absence of data to corroborate such a prediction, as well as predictions of physical dielectric thickness, the targets are left constant for future years.

Was	(G) Based on $Di=1/q*C_{gate}*DV*.10$, where C_{gate} is computed for electrically equivalent to SiO_2 gate dielectric thickness and DV is the allowable threshold voltage variability for this node. It is assumed that 10% of allowable shift is attributable to Di. $Di = ((3.9*8.85)/1.6)*(DV/EOT)*E+9$
Is	(G) Based on $Di=1/q*C_{gate}*DV*0.05$, where C_{gate} is computed for electrically equivalent to SiO_2 gate dielectric thickness and DV is the allowable threshold voltage variability for this node. It is assumed that 5% of allowable shift is attributable to Di. $Di = ((3.9*8.85)/1.6)*(0.05*DV/EOT)*10^9$, with DV is in mV and EOT is in nm, and the oxide dielectric constant is 3.9 Note that the year-to-year value for D_i does not always decrease because D_i is not only proportional to DV, which does not always decrease year to year, but is also inversely proportional to EOT, which decreases every year.

(H) Residual carbon in a gate stack resulting from organic contamination after surface preparation. Dc at the 180nm corresponded to 10% carbon atom coverage of a bare silicon wafer ($7.3E+13 atoms/cm^2$). Dc for subsequent nodes were scaled linearly with the ratio of CD to 180nm. $Dc = (CD/180)(7.3E+13)$

Was	(I) Device channel mobility cannot be degraded >10% due to surface preparation induced surface roughness. Current technologies are successfully manufactured with AFM based determination of 0.2 nm RMS of surface micro-roughness. This RMS value is an average over the range of spatial frequencies sampled by the AFM. The surface micro-roughness that affects carrier mobility occurs at smaller spatial frequencies than those that are sampled in the typical AFM micro-roughness measurement.
Is	(I) Device channel mobility cannot be degraded >5% due to surface preparation induced surface roughness. Current technologies are successfully manufactured with AFM based determination of 0.2 nm RMS of surface micro-roughness. This RMS value is an average over the range of spatial frequencies sampled by the AFM. The surface micro-roughness that affects carrier mobility occurs at smaller spatial frequencies than those that are sampled in the typical AFM micro-roughness measurement.

(J) Water marks are generally large enough to touch more than one die and they result in failure of each of the die they touch. Therefore a single water mark will exceed the allowable die loss of 1%. Hence the specification is <1 water mark per wafer.

Notes for Tables 50a and b (continued)

Was	*(K) Residual interfacial oxygen resulting from inadequate passivation after surface preparation. Oxygen concentrations up to <1E+14 atoms/cm^2 are acceptable for all processes until selective epitaxial for raised source/drains and high κ gates are implemented.*
Is	***(K) Residual interfacial oxygen resulting from inadequate passivation after surface preparation. Oxygen concentrations up to <1E+13 atoms/cm^2 are acceptable for processes such as pre-silicide cleaning. Current pre-gate cleaning does not require an oxide-free surface, but the pre-gate surface should be either fully passivated by a continuous oxide layer or have <1E+13/cm^2, as an intermediate level of oxygen will be unstable. It is unclear whether high κ gate dielectrics will require oxide-free or oxide-passivated surfaces prior to deposition. More stringent oxide levels will be required for selective epitaxy when raised source/drains are implemented, thus <1E+12 is specified in Table 50b.***

[1] Mertens, P. W., "Advanced Cleaning Technology," UCPSS 2000, Ostende, Belgium, invited tutorial, pp. 31-48 (2000).

[2] Mertens, P. W., et. al., "Recent Advances in Wafer Cleaning Technology," Semicon Europa Front End Technology Conference, Munich, 24 April (2001).

Table 51a Thermal & Thin Film, Doping and Etching Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	DRAM
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	MPU
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	MPU
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	MPU
Was	Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A]	1.3–16	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1	MPU
Is	Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A]	1.3–1.6	1.2–1.5	1.1–1.4	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1	MPU
	Gate dielectric leakage at 100°C (nA/µm) High-performance [B]	10	30	70	100	300	700	1000	MPU
Was	Physical gate length low power (nm)	90	80	65	53	45	37	32	Low Power
Is	Physical gate length low operating power (LOP) (nm)	90	75	65	53	45	37	32	Low Power
Add	Physical gate length low standby power (LSTP) (nm)	100	90	75	65	53	45	37	Low Power
	Equivalent physical oxide thickness for low operating power Tox (nm) [A]	2.0-24	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4	LOP
	Gate dielectric leakage (pA/µm) LOP [B]	100	100	100	300	300	300	700	LOP
	Equivalent physical oxide thickness for low standby power Tox (nm) [A]	2.4-2.8	2.2-2.6	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	LSTP
	Gate dielectric leakage (pA/µm) LSTP [B]	1	1	1	1	1	1	1	LSTP
	Equivalent physical oxide thickness for DRAM transfer device Tox (nm) [A]	5	4.5	4.1	3.6	3.3	3	2.7	DRAM
	Gate dielectric leakage at 100°C (fA/µm) DRAM transfer device [B]	4.1	4.6	2.6	2.4	1.4	1.6	1.4	DRAM
	Thickness control EOT (% 3σ) [C]	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4	MPU/ASIC
	Gate Etch Bias (nm) [D-1]	25.2	21.2	17.8	15	12.6	11.2	10	MPU/ASIC
	L_{gate} 3σ variation (nm) [D]	6.31	5.3	4.46	3.75	3.15	2.81	2.5	MPU/ASIC
	Total maximum allowable lithography 3σ (nm) [D-2]	5.15	4.33	3.64	3.06	2.57	2.29	2.04	MPU/ASIC
	Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [D-2]	3.64	3.06	2.57	2.17	1.82	1.62	1.44	MPU/ASIC
	Resist trim maximum allowable 3σ (nm) [D-3]	2.1	1.77	1.49	1.25	1.05	0.94	0.83	MPU/ASIC
	Gate etch maximum allowable 3σ (nm) [D-3]	2.5	2.1	1.77	1.48	1.32	1.18	1.05	MPU/ASIC
	CD bias between dense and isolated lines [E]	≤ 15%	≤ 15%	≤ 15%	≤ 15%	≤ 15%	≤ 15%	≤ 15%	MPU/ASIC
	Minimum measurable gate dielectric remaining (post gate etch clean) [F]	>0	>0	>0	>0	>0	>0	>0	MPU/ASIC
	Profile control (side wall angle) [FF]	>89	>89	>89	90	90	90	90	MPU/ASIC
Was	Drain extension Xj (nm) [G]	27-45	22-36	19-31	15-25	13-22	19-Dec	17-Oct	MPU/ASIC
Is	Drain extension Xj (nm) [G]	27-45	22-36	19-31	15-25	13-22	12-19	10-17	MPU/ASIC
	Maximum drain extension sheet resistance (PMOS) (Ω/sq) [H]	400	460	550	660	770	830	760	MPU/ASIC
Add	Maximum drain extension sheet resistance (NMOS) (Ω/sq) [H]	190	220	260	310	360	390	360	MPU/ASIC
	Extension lateral abruptness (nm/decade) [I]	7.2	5.8	5	4.1	3.5	3.1	2.8	MPU/ASIC
	Contact Xj (nm) [J]	48–95	39–78	33–66	27–45	24–47	21–42	18–37	MPU/ASIC
	Sidewall spacer thickness (nm) extension structure [K]	48–95	39–78	33–66	27–45	24–47	21–42	18–37	MPU/ASIC
	Spacer thickness, elevated contact [L]	—	—	—	15–25	13–22	12–19	10–17	MPU/ASIC
	Spacer thickness, single contact [M]	—	—	—	—	—	—	5-8.5	MPU/ASIC
	Maximum silicon consumption (nm) [N]	23–46	19–38	16–32	13–26	11–23	10–20	9–18	MPU/ASIC
	Silicide thickness (nm) [O]	35.8	29.2	24.8	20.4	17.6	15.4	13.8	MPU/ASIC
	Contact silicide sheet Rs (Ω/sq) [P]	4.2	5.1	6.1	7.4	8.5	9.7	10.9	MPU/ASIC
	Contact maximum resistivity ($\Omega\text{-cm}^2$) [Q]	4.10E-07	3.20E-07	2.70E-07	2.10E-07	1.80E-07	1.60E-07	1.10E-07	MPU/ASIC
	Gate electrode thickness [R]	65–130	53–106	45–90	37–74	32–64	30–60	25–50	MPU/ASIC
	Active poly doping for 25% depletion allowance (cm^{-3}) [S]	9.2 E19	9.2 E19	1.14 E20	1.50 E20	1.66 E20	1.66 E20	1.87 E20	MPU/ASIC

Table 51a Thermal & Thin Film, Doping and Etching Technology Requirements—Near-term (continued)

	Year of Production	2001	2002	2003	2004	2005	2006	2007	Driver
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	DRAM
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65	MPU
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35	MPU
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25	MPU
Was	Average gate electrode sheet Rs (Ω/sq) from table [T]	5	5	5	5	5	5	5	MPU/ASIC
Is	Average gate electrode sheet Rs (Ω/sq) [T]	5	5	5	5	5	5	5	MPU/ASIC
	Channel concentration for Wdepletion <1/4L_{eff} (cm^{-3}) [U]	4.0 E18	6.0 E18	8.0 E18	1.1E 19	1.4E 19	1.6 E19	2.3 E19	MPU/ASIC
	Uniform channel concentration (cm^{-3}), for V_t=0.4 [V]	0.8–1.5 E18	0.8–1.5 E18	1.5–2.5 E18	1.5–2.5 E18	1.5–2.5 E18	2.0–4.0 E18	2.5–5.0 E18	MPU/ASIC
Was	Retrograde channel depth (nm) [W]	21-30	19-27	16-23	15-21	13-19	16-Nov	15-Oct	MPU/ASIC
Is	Retrograde channel depth (nm) [W]	21-30	19-27	16-23	15-21	13-19	11-16	10-15	MPU/ASIC
	Undoped dielectric layer thickness (nm) [X]	500	465	435	400	365	335	300	MPU/ASIC
	Alkali diffusion barrier layer thickness (nm)	50	46	43	40	36	33	30	MPU/ASIC
	Undoped bit line dielectric layer thickness (nm) [Y]	200	193	187	180	174	168	162	DRAM
	Cell dielectric layer thickness (nm) [Z]	200	193	187	180	174	168	162	DRAM
	M-1 dielectric layer thickness (nm) [AA]	250	242	233	225	217	210	203	DRAM

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

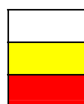


Table 51b Thermal & Thin Film, Doping and Etching Technology Requirements—Long-term

	Year of Production	2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	DRAM
	MPU / ASIC ½ Pitch (nm)	50	35	25	MPU
	MPU Printed Gate Length (nm)	25	18	13	MPU
	MPU Physical Gate Length (nm)	18	13	9	MPU
	Equivalent physical oxide thickness for MPU/ASIC Tox (nm) [A]	0.5–0.8	0.4–0.6	0.4–0.5	MPU/ASIC
	Gate dielectric leakage at 100°C (µA/µm) High-performance [B]	3	7	10	MPU/ASIC
Was	Physical gate length low power (nm)	22	16	11	Low Power
Is	Physical gate length operating low **operating** power (LOP) (nm)	22	16	11	Low Power
Add	Physical gate length low standby power (LSTP) (nm)	22	16	11	Low Power
	Equivalent physical oxide thickness for low operating power T_{ox} (nm) [A]	0.8-1.2	0.7-1.1	0.6-1.0	LOP
	Gate dielectric leakage (pA/µm) LOP [B]	1000	3000	10000	LOP
	Equivalent physical oxide thickness for low standby power T_{ox} (nm) [A]	0.9-1.3	0.8-1.2	07-1.1	LSP
	Gate dielectric leakage (pA/µm) LSTP [B]	3	7	10	LSTP
	Equivalent physical oxide thickness for DRAM transfer device T_{ox} (nm) [A]	1.55	1.05	0.55	DRAM
	Gate dielectric leakage at 100°C (nA/µm) DRAM transfer device [B]	0.7	0.3	0.2	DRAM
	Thickness control EOT (% 3σ) [C]	<± 4	<± 4	<± 4	MPU/ASIC
Delete	~~Leffective control~~	~~≤ 20%~~	~~≤ 20%~~	~~≤ 20%~~	~~MPU/ASIC~~
	Gate etch bias (nm) [D-1]	7.1	5	3.6	MPU/ASIC
	L_{gate} 3σ variation (nm) [D]	1.77	1.25	0.88	MPU/ASIC
	Total allowable lithography 3σ (nm) [D-2]	1.45	1.02	0.72	MPU/ASIC
	Total allowable etch 3σ (nm), including photoresist trim and gate etch [D-2]	1.02	0.72	0.51	MPU/ASIC
	Resist trim allowable 3σ (nm) [D-3]	0.59	0.42	0.29	MPU/ASIC
	Gate etch allowable 3σ (nm) [D-3]	0.83	0.59	0.41	MPU/ASIC
	CD bias between dense and isolated lines [E]	≤ 15%	≤ 15%	≤ 15%	MPU/ASIC
	Minimum measurable gate dielectric remaining (post gate etch clean) [F]	>0	>0	>0	MPU/ASIC
	Profile control (side wall angle) [FF]	90	90	90	MPU/ASIC
	Drain extension Xj (nm) [G]	7–12	5–9	4–6	MPU/ASIC
	Maximum drain extension sheet resistance (PMOS) (Ω/sq) [H]	830	940	1210	MPU/ASIC
Add	Maximum drain extension sheet resistance (NMOS) (Ω/sq) [H]	390	440	570	MPU/ASIC
	Extension lateral abruptness (nm/decade) [I]	2	1.4	1	MPU/ASIC
	Contact Xj (nm) [J]	13–26	10–19	7–13	MPU/ASIC
	Sidewall spacer thickness (nm) extension structure [K]	13–26	10–19	7–13	MPU/ASIC
	Spacer thickness, elevated contact [L]	7–12	5–9	4–6	MPU/ASIC
	Spacer thickness, single contact [M]	3.5–6	2.5–4.5	2–3	MPU/ASIC
	Maximum silicon consumption (nm) [N]	6–13	5–9	3–6	MPU/ASIC
	Silicide thickness (nm) [O]	9.9	7.2	5	MPU/ASIC
	Contact silicide sheet Rs (Ω/sq) [P]	15.2	21	30.3	MPU/ASIC
	Contact maximum resistivity (Ω-cm^2) [Q]	6.40E-08	3.80E-08	2.40E-08	MPU/ASIC
	Gate electrode thickness [R]	18–36	13–26	9–18	MPU/ASIC
Was	Active poly doping for 25% depletion allowance (cm^{-3}) [S]	1.80E+20	2.50E+20	2.99E+20	MPU/ASIC
Is	Active poly doping for 25% depletion allowance (cm^{-3}) [S]	2.50E+20	2.99E+20	3.74E+20	MPU/ASIC

Table 51b Thermal & Thin Film, Doping and Etching Technology Requirements—Long-term(continued)

	Year of Production	2010	2013	2016	Driver
	DRAM ½ Pitch (nm)	45	32	22	DRAM
	MPU / ASIC ½ Pitch (nm)	50	35	25	MPU
	MPU Printed Gate Length (nm)	25	18	13	MPU
	MPU Physical Gate Length (nm)	18	13	9	MPU
Was	Average gate electrode sheet Rs (Ω/sq) from Table [T]	5	6	7	MPU/ASIC
Is	Average gate electrode sheet Rs (Ω/sq) [T]	5	6	7	MPU/ASIC
	Channel concentration for Wdepletion <1/4L_{eff} (cm^{-3}) [U]	5.00E+19	1.30E+20	5.00E+20	MPU/ASIC
	Uniform channel concentration (cm^{-3}), for V_t=0.4 [V]	5.0–9.0 E18	0.9–1.8 E19	1.5–3.0 E19	MPU/ASIC
	Retrograde channel depth (nm) [W]	7–10	5–7	3–5	MPU/ASIC
	Undoped dielectric layer thickness (nm) [X]	300	250	200	MPU/ASIC
	Alkali diffusion barrier layer thickness (nm)	30	25	20	MPU/ASIC
	Undoped bit line dielectric layer thickness (nm) [Y]	146	131	118	DRAM
	Cell dielectric layer thickness (nm) [Z]	146	131	118	DRAM
	M-1 dielectric layer thickness (nm) [AA]	182	164	148	DRAM

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 53a DRAM Trench Capacitor Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Storage node area, top view [(DRAM 1/2 pitch)^2]	**2**	**2**	**2**	**<2**	**<2**	**<2**	**<2**
	Trench structure	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**	**bottled**
	Trench area enhancement factor	**1.3**	**1.5**	**1.5**	**1.7**	**1.7**	**1.7**	**1.7**
	Capacitor dielectric equivalent oxide thickness (nm)	**4.5**	**4.5**	**4.3**	**3.6**	**3.2**	**2.8**	**2.6**
	Trench depth [µm], (at 35fF)	**7.6**	**7.5**	**8.2**	**6.9**	**6.9**	**6.8**	**6.9**
	Aspect ratio (trench depth / trench width)	**43**	**48**	**61**	**64**	**72**	**81**	**88**
Was	*Upper electrode*	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Metal/Poly-Si**	**Metal/Poly-Si**
Is	*Upper electrode*	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**Poly-Silicon**	**1.Metal/Poly-Si 2. Metal**	**1.Metal/Poly-Si 2. Metal**
	Dielectric material	**NO**	**NO**	**NO**	**High-κ**	**High-κ**	**High-κ**	**High-κ**
	Bottom electrode	**Silicon**	**Silicon**	**Silicon**	**Silicon**	**Silicon**	**Silicon**	**Silicon**
Was	*Capacitor Structure / dielectric*	**Silicon-Insulator-Silicon / NO**			**Silicon-Insulator-Silicon / High-κ**		**Metal Silicon-Insulator-Silicon / High-κ**	
Is	*Capacitor Structure / dielectric*	**Silicon-Insulator-Silicon / NO**			**Silicon-Insulator-Silicon / High-κ**		**1. Metal Silicon-Insulator-Silicon / High-κ 2. Metal-Insulator-Silicon / High-κ**	

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

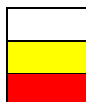


Table 54a FLASH Non-volatile Memory Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Was	*Flash technology node (nm) [A]*	**150**	**130**	**115**	**100**	**90**	**80**	**70**
Is	*Flash technology node (nm) [A]*	**150**	**130**	**107**	**90**	**80**	**70**	**65**
Was	*Flash NOR tunnel oxide thickness (EOT - nm) [B]*	**9.5–10.5**	**9.5–10**	**9–10**	**9–10**	**8.5–9.5**	**8.5–9.5**	**8.5–9.5**
Is	*Flash NOR tunnel oxide thickness (EOT - nm) [B]*	**9.5–10.5**	**9–10**	**9–10**	**8.5–9.5**	**8.5–9.5**	**8.5–9.5**	**8–9**
Was	*Flash NAND tunnel oxide thickness (EOT - nm) [B]*	**8.5–9.5**	**8.5–9**	**8–9**	**8–9**	**8–9**	**7.5–8**	**7.5–8**
Is	*Flash NAND tunnel oxide thickness (EOT - nm) [B]*	**8.5–9.5**	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**	**6–7**
Was	*Flash tunnel oxide thickness control EOT (% 3σ) [C]*	**<± 4**	**<± 4**	**<± 3.5**	**<± 3.5**	**<± 3**	**<± 3**	**<± 3**
Is	*Flash tunnel oxide thickness control EOT (% 3σ) [C]*	**<± 4**	**<± 4**	**<± 3.5**	**<± 3**	**<± 3**	**<± 3**	**<± 3**
	Flash tunnel oxide minimum Q_{BD} @ 1×10^{-2} A/cm^2 (C/cm^2) [D]	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
	Flash tunnel oxide defectivity @ minimum Q_{BD} (def/cm^2) [E]	**<0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**	**<0.01**
	Flash tunnel low field leakage (nA/5V) [F]	**100**	**100**	**100**	**100**	**100**	**100**	**100**
	Flash program/erase window ΔV_T (V) [G]	**>3**	**>3**	**>3**	**>3**	**>3**	**>3**	**>3**
	Flash erase time degradation t_{max}/t_0 [H]	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**
	Flash program time degradation t_{max}/t_0 [I]	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**
Was	*Flash NOR interpoly dielectric thickness (EOT-nm) [J]*	**13-15**	**12-14**	**11-13**	**11-13**	**10-12**	**9-11**	**9-11**
Is	*Flash NOR interpoly dielectric thickness (EOT-nm) [J]*	**13-15**	**12-14**	**11-13**	**10-12**	**9-11**	**9-11**	**8.5-10.5**
Was	*Flash NAND interpoly dielectric thickness (EOT-nm) [J]*	**14-16**	**13-15**	**12-14**	**12-14**	**12-14**	**11-13**	**10-12**
Is	*Flash NAND interpoly dielectric thickness (EOT-nm) [J]*	**14-16**	**13-15**	**13-15**	**13-15**	**13-15**	**13-15**	**10-13**
	Flash interpoly dielectric thickness control EOT (% 3σ) [K]	**<± 7**	**<± 7**	**<± 6**	**<± 6**	**<± 6**	**<± 6**	**<± 6**
Was	*Flash interpoly dielectric T_{max} of formation $t > 5' / < 5'$ (ºC) [L]*	**800 / 900**	**800 / 900**	**750 / 900**	**750 / 900**	**700 / 850**	**700 / 850**	**650 / 800**
Is	*Flash interpoly dielectric T_{max} of formation $t > 5' / < 5'$ (ºC) [L]*	**800 / 900**	**800 / 900**	**750 / 900**	**700 / 850**	**700 / 850**	**650 / 800**	**650 / 800**
Was	*Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [M]*	**>0.92**	**>0.95**	**>0.95**	**>0.95**	**>0.95**	**>0.98**	**>0.98**
Is	*Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [M]*	**>0.92**	**>0.95**	**>0.95**	**>0.95**	**>0.98**	**>0.98**	**>0.98**
	Flash maximum charge loss 10 years @Room Temp (V) – single/dual bit (%) [N]	**20 / 10**	**20 / 10**	**20 / 10**	**20 / 10**	**20 / 10**	**20 / 10**	**20 / 10**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

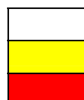


Table 54b FLASH Non-volatile Memory Technology Requirements—Long-term

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Flash technology node (nm) [A]	**50**	**35**	**25**
	Flash NOR tunnel oxide thickness (EOT - nm) [B]	**8-9**	**8**	**8**
	Flash NAND tunnel oxide thickness (EOT - nm) [B]	**6–7**	**6–7**	**6–7**
	Flash tunnel oxide thickness control EOT (% 3σ) [C]	**<± 2.5**	**<± 2.5**	**<± 2**
	Flash tunnel oxide minimum Q_{BD} @ 1×10^{-2} A/cm^2 (C/cm^2) [D]	**0.3**	**0.3**	**0.4**
	Flash tunnel oxide defectivity @ minimum Q_{BD} (def/cm^2) [E]	**<0.01**	**<0.01**	**<0.01**
	Flash tunnel low field leakage (nA/5V) [F]	**100**	**100**	**100**
	Flash program/erase window ΔV_T (V) [G]	**>3**	**>3**	**>3**
	Flash erase time degradation t_{max}/t_0 [H]	**<2**	**<2**	**<2**
	Flash program time degradation t_{max}/t_0 [I]	**<2**	**<2**	**<2**
	Flash NOR interpoly dielectric thickness (EOT-nm) [J]	**8-10**	**6-8**	**4-6**
Was	*Flash NAND interpoly dielectric thickness (EOT-nm) [J]*	**10-12**	**9-11**	**9-11**
Is	*Flash NAND interpoly dielectric thickness (EOT-nm) [J]*	**10-13**	**9-10**	**9-10**
	Flash interpoly dielectric thickness control EOT (% 3σ) [K]	**<± 5**	**<± 5**	**<± 5**
	Flash interpoly dielectric T_{max} of formation t >5′ / < 5′ (°C) [L]	**600 / 750**	**600 / 700**	**600 / 700**
	Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [M]	**>0.98**	**>0.98**	**>0.98**
	Flash maximum charge loss 10 years @Room Temp (V) – single/dual bit (%) [N]	**20 / 10**	**20 / 10**	**20 / 10**

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known