

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

Table 34 Process Integration Difficult Challenges [Update]

	Difficult Challenges $\geq 65\text{nm}$ / Through 2007	Summary of Issues
Was	1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs.	<ul style="list-style-type: none"> – Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage. – Implementation of metal gate electrode by about 2007. – Need to reduce series S/D parasitic resistance. – Controlling static power dissipation in the face of rapidly increasing leakage. – Architecture and circuit design improvement and innovation will be needed
Is	1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs.	<ul style="list-style-type: none"> – Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage. – Implementation of metal gate electrode and high κ gate dielectric by about 2007. – Need to reduce series S/D parasitic resistance. – Controlling static power dissipation in the face of rapidly increasing leakage. – Architecture and circuit design improvement and innovation will be needed
	2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs.	<ul style="list-style-type: none"> – Early availability of manufacturing-worthy high κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. – Very slow scaling of V_{dd} will make overall device scaling difficult.
	3. Implementation into manufacturing of non-classical MOSFET devices (for example, double-gate SOI).	<ul style="list-style-type: none"> – It is likely that these transistors will be necessary eventually to control short-channel and other effects in highly scaled devices. See Emerging Research Devices section, Non-classical CMOS, for more detail.
	4. Ensuring reliability of new materials and structures in a timely manner.	<ul style="list-style-type: none"> – Accelerated reliability ensurance of high κ material for gate stack will be needed for early insertion into manufacturing. – Ensuring reliability of new gate electrode materials will be a challenge. – Ensuring reliability of new, non-classical CMOS structures will be a challenge. – Ensuring reliability of very thin oxy-nitrides with very high leakage current will be critical for high-performance applications. – Difficulty of screening with high leakage currents
	5. Constructing DRAM, SRAM, and high density nonvolatile memory (NVM) for scaled technologies	<ul style="list-style-type: none"> – DRAM main issues: adequate storage capacitance for devices with reduced feature size; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. Also, the availability of manufacturing worthy 193 nm lithography and integrated DRAM etch capability for 100 nm half pitches in 2003. – SRAM: difficult lithography and etch as well as process integration issues. – NVM: very difficult scaling issues with tunnel and interpoly dielectrics.
	6. High-performance mixed-signal solutions for scaled technologies.	<ul style="list-style-type: none"> – Passive element scaling: embedded inductor densities and Q factor values. – Signal isolation. – Optimizing RF CMOS devices with scaled technologies: gate leakage is a particularly sensitive issue. – Transition to reduced analog supply voltages. – Difficulty and cost of integrating analog/RF and high-performance digital functions on a chip.

Table 34 Process Integration Difficult Challenges [[Update](#)](continued)

<i>Difficult Challenges < 65 nm, Beyond 2007</i>	<i>Summary of Issues</i>
7. Fundamental improvements in MOSFET device effective transconductance needed to maintain device performance scaling trend.	<ul style="list-style-type: none"> – With sharp reductions in V_{dd} and 17% annual increase in intrinsic transistor speed, basic MOSFET device performance will be inadequate to meet circuit speed requirements.
8. Dealing with atomic-level fluctuations and statistical process variations in sub-30 nm MOSFETs.	<ul style="list-style-type: none"> – Fundamental problems of atomic-level statistical fluctuations are not completely understood.
9. New interconnect schemes	<ul style="list-style-type: none"> – Eventually, copper/low κ performances will be inadequate. – Solutions (optical, microwave/RF, etc.) are currently unclear.
10 Toward the end of the Roadmap or beyond, implementation of advanced non-CMOS devices and architectures, including memory.	<ul style="list-style-type: none"> – Will drive major changes in process, materials, physics, design, etc. – Non-CMOS devices may coexist with CMOS: integration of the two will be difficult, especially for mixed signal. – See Emerging Research Devices sections for more discussion and detail.

Table 35a High-performance Logic Technology Requirements—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Physical gate length high-performance (HP) (nm) [1]	65	53	45	37	32	28	25
Was	Equivalent physical oxide thickness for high-performance T_{ox} (EOT) (nm) [2]	1.3–1.6	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1
Is	<u>EOT: equivalent oxide thickness (physical) for high-performance</u> (nm) [2]	1.3–1.6	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1
	Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Was	T_{ox} electrical equivalent (nm) [4]	2.3	2.1	2	2	1.9	1.9	1.4
Is	<u>Equivalent oxide thickness (electrical)</u> (nm) [4]	2.3	2.1	2	2	1.9	1.9	1.4
	Nominal power supply voltage (V_{dd}) (V) [5]	1.2	1.1	1	1	0.9	0.9	0.7
	Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25° C) ($\mu A/\mu m$) [6]	0.01	0.03	0.07	0.1	0.3	0.7	1
	Nominal high-performance NMOS saturation drive current, I_{dd} (at V_{dd} , at 25° C) ($\mu A/\mu m$) [7]	900	900	900	900	900	900	900
	Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
	Parasitic source/drain resistance (Rsd) (ohm- μm) [9]	190	180	180	180	180	170	140
	Parasitic source/drain resistance (Rsd) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	16%	16%	17%	18%	19%	19%	20%
	Parasitic capacitance percent of ideal gate capacitance [11]	19%	22%	24%	27%	29%	32%	27%
	High-performance NMOS device τ ($C_{gate} * V_{dd} / I_{dd}$ -NMOS)(ps) [12]	1.6	1.3	1.1	0.99	0.83	0.76	0.68
	Relative device performance [13]	1	1.2	1.5	1.6	2	2.1	2.5
Was	Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate} * (3 * L_{gate}) * V_{dd}^2$) (fJ/Device) [14]	0.347	0.212	0.137	0.099	0.065	0.052	0.032
Is	<u>Power-delay product for ($W/L_{gate}=3$) device [$C_{gate} * (3 * L_{gate}) * V_{dd}^2$]</u> (fJ/Device) [14]	0.347	0.212	0.137	0.099	0.065	0.052	0.032
	Static power dissipation per ($W/L_{gate}=3$) device (Watts/Device) [15]	5.60E-09	6.70E-09	1.00E-08	1.10E-08	2.60E-08	5.30E-08	5.30E-08

White—Manufacturable Solutions Exist, and Are Being Optimized
 Yellow—Manufacturable Solutions are Known
 Red—Manufacturable Solutions are NOT Known



Table 35b High-performance Logic Technology Requirements—Long-term

Year of Production		2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Physical gate length high-performance (HP) (nm) [1]	18	13	9
Was	Equivalent physical oxide thickness for high-performance T_{ox} (EOT) (nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
	Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.5	0.5	0.5
Was	T_{ox} electrical equivalent (nm) [4]	1.2	1	0.9
Is	Equivalent oxide thickness (electrical) (nm) [4]	1.2	1	0.9
	Nominal power supply voltage (V_{dd}) (V) [5]	0.6	0.5	0.4
	Nominal high-performance NMOS sub threshold leakage current, $I_{sd,leak}$ (at 25 °C) ($\mu A/\mu m$) [6]	3	7	10
	Nominal high-performance NMOS saturation drive current, I_{dd} (at V_{dd} , at 25 °C) ($\mu A/\mu m$) [7]	1200	1500	1500
	Required percent current-drive "mobility/transconductance improvement" [8]	30%	70%	100%
	Parasitic source/drain resistance (R_{sd}) (ohm- μm) [9]	110	90	80
	Parasitic source/drain resistance (R_{sd}) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	25%	30%	35%
	Parasitic capacitance percent of ideal gate capacitance [11]	31%	36%	42%
	High-performance NMOS device τ ($C_{gate} * V_{dd} / I_{dd}$ -NMOS)(ps) [12]	0.39	0.22	0.15
	Relative device performance [13]	4.3	7.2	10.7
Was	Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate} * (3 * L_{gate}) * V^2$) (fJ/Device) [14]	0.015	0.007	0.002
Is	Power-delay product for ($W/L_{gate}=3$) device [$C_{gate} * (3 * L_{gate}) * V_{dd}^2$] (fJ/Device) [14]	0.015	0.007	0.002
	Static power dissipation per ($W/L_{gate}=3$) device (Watts/Device) [15]	9.70E-08	1.40E-07	1.10E-07

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Notes for Table 35a and b:

	[1] Values set by ORTC. Gate dimensional control is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three sigma value of $\pm 10\%$. Gate dimension variation is assumed to be the primary factor responsible for driving device parameter variation.
Was	[2] EOT range set by FEP TWG. Yellow/red feasibility coloring set by FEP TWG projections on thickness control and reliability capability. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values.
Is	[2] EOT range set by FEP TWG. Yellow/red feasibility coloring set by FEP TWG projections on thickness control and reliability capability. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values. <u>For a gate dielectric of thickness T_d and relative dielectric constant k, EOT is defined by: $EOT = T_d / (k/3.9)$, where 3.9 is the relative dielectric constant of thermal silicon dioxide. The ideal gate capacitance per unit area of the gate dielectric of thickness T_d is the same as that of a gate dielectric made up of thermal silicon dioxide with a thickness of EOT.</u>
	[3] Accounts for gate electrode depletion and inversion-layer quantum effects. Yellow feasibility coloring reflects FEP assessment of polysilicon doping capability; red feasibility coloring reflects the introduction of metal-gate electrodes by 2007 (which reduces the gate depletion value).
	[4] Sum of midpoint EOT and Electrical Thickness Adjustment Factor. Used in CV/I performance metric and CV^2 dynamic power metric calculations. Red/yellow feasibility coloring determined by worst-case EOT and Electrical Thickness Adjustment Factor red/yellow feasibility coloring.
Was	[5] Nominal power supply voltage has been set to maintain sufficient voltage over-drive to continue historical approximate 17% per year device performance scaling while still enabling approximate 30% per year switching energy reduction and still maintaining reasonable vertical gate dielectric electric field strengths. Actual power supply voltage values may vary $\pm 10\%$, depending on the particular circuit design application or technology optimization.
Is	[5] Nominal power supply voltage has been set to maintain sufficient voltage over-drive to continue historical approximate 17% per year device performance scaling while still enabling approximate 30% per year switching energy reduction and still maintaining reasonable vertical gate dielectric electric field strengths. Actual target power supply voltage values may vary $\pm 10\%$, depending on the particular circuit design application or technology optimization.
	[6] Nominal sub-threshold leakage current is defined as the NMOSFET source current at room temperature with the drain bias set equal to the nominal power-supply voltage and with the gate, source and substrate biases set to zero volts; all MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current at room temperature, and is the sum of the NMOS sub-threshold, gate, and junction leakage current components. The sub-threshold leakage current is assumed to be larger than either the gate or junction leakage current components at either room or high-temperature conditions. The threshold voltage value (and the corresponding sub-threshold current) has been set to maintain sufficient voltage over-drive to continue historical approximate 17% per year device performance scaling. Yellow feasibility coloring by 2007 reflects the potential need for non-classical CMOS or ultra-shallow junction technology in order to control short-channel and/or high-field effects (See Emerging Research Devices section). The above sub-threshold, gate, and junction current scaling scenario also applies to PMOS devices. Note, sub-threshold current value applies to fastest MOS devices only; slower/lower-leakage MOS devices will also be available. Future systems will consist of a mix of both high and lower-leakage devices.
	[7] Nominal saturation current drive is defined as the MOSFET drain current at room temperature with the gate bias and the drain bias set equal to the nominal power-supply voltage; all MOSFET device dimensions are assumed to be at their nominal/target values. Nominal PMOS saturation current-drive value is assumed to be 40-50% of the nominal NMOS saturation current-drive value. Yellow/red feasibility coloring indicates the projected need for fundamental device current-drive (or transconductance/mobility) improvement by 2010 in order to continue historical approximate 17% per year device performance scaling. NMOS/PMOS current-drive targets are approximate with only 1.5 significant digits of accuracy.
	[8] Fundamental device mobility/transconductance improvement needed by 2010 in order to continue historical approximate 17% per year device performance scaling. Yellow/red feasibility coloring indicates the difficulty in implementing fundamental device current-drive (transconductance/mobility) improvement required in 2010 and later to continue historical approximate 17% per year device performance scaling.
Was	[9] Total parasitic device source/drain resistance R_{sd} (sum of the source and drain parasitic resistances). R_{sd} targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling. Similar R_{sd} values are assumed for the LOP and LSTP devices.
Is	[9] Maximum allowable parasitic device source/drain resistance R_{sd} (sum of the source and drain parasitic resistances). R_{sd} targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling. Similar R_{sd} values are assumed for the LOP and LSTP devices.
Was	[10] Maximum ratio of the parasitic device source/drain resistance (R_{sd}) to the ideal channel resistance (V_{dd}/I_{dd}). R_{sd} targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.
Is	[10] Maximum Ratio of the parasitic device source/drain resistance (R_{sd}) to the ideal channel resistance (V_{dd}/I_{dd}). R_{sd} targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

Notes for Table 35a and b(continued)

Was	[11] Maximum ratio of the parasitic gate overlap/fringing capacitance to the ideal gate capacitance. Assume constant C-parasitic value of 2.4E-16F/um. [3×the fringing capacitance value per side, including the Miller effect]; this value is assumed to be independent of bias conditions and/or technology. Parasitic capacitance factor is included in CV/I and CV ² performance and power metric calculations. Similar parasitic capacitance values are assumed for the LOP and LSTP devices.
Is	[11] Maximum ratio of the parasitic gate overlap/fringing capacitance to the ideal gate capacitance. Assume constant C-parasitic value of 2.4E-16F/um. [3×the fringing capacitance value per side, including the Miller effect]; this value is assumed to be independent of bias conditions and/or technology. Parasitic capacitance factor is included in CV/I and CV ² performance and power metric calculations. Similar parasitic capacitance values are assumed for the LOP and LSTP devices.
	[12] $\tau = CV/I$ intrinsic delay metric for NMOS device; PMOS CV/I metric assumed to scale proportionally. The CV/I metric provides an indication of the intrinsic switching delay of the device, while $1/\tau$, the reciprocal of CV/I, is a good metric for the intrinsic switching speed of the device. Red/yellow feasibility coloring determined by worst-case saturation current-drive feasibility coloring.
	[13] Improvement in $1/\tau$ NMOS performance metric normalized to the year 2001. Maintains historical approximate 17% per year device performance improvement scaling trend. Red/yellow feasibility coloring determined by worst-case, saturation current-drive feasibility coloring.
Was	[14] CV ² switching energy metric for an NMOS device with dimensions W/Lgate=3. The switching energy metric indicates the amount of dynamic power required to switch the device. Maintains approximate 30% per year device switching energy reduction scaling trend. Red/yellow feasibility coloring determined by worst-case saturation current-drive feasibility and mobility/transconductance improvement feasibility coloring.
Is	[14] CV ² switching energy metric for an NMOS device with dimensions W/Lgate=3. The power-delay product indicates the amount of dynamic energy required to switch the device through a full (up and down) transition . Maintains approximate 30% per year device switching energy reduction scaling trend. Red/yellow feasibility coloring determined by worst-case saturation current-drive feasibility and mobility/transconductance improvement feasibility coloring.
	[15] Static power dissipation for an NMOS device with dimensions W/Lgate=3. Assume that the device static power is primarily determined by the sub-threshold current (since the other junction and leakage current components are assumed to be lower). Yellow feasibility coloring by 2007 reflects the potential need for non-classical CMOS or ultra-shallow junction technology in order to control short-channel and/or high-field effects (See Emerging Research Devices section, Non-classical CMOS).

Table 36a Low Operating Power (LOP) Logic Technology Requirements—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Physical gate length low-operating power (LOP) (nm) [1]	90	75	65	53	45	37	32
Was	Equivalent physical oxide thickness for LOP T_{ox} (EOT) (nm) [2]	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4
Is	EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Was	T_{ox} electrical equivalent (nm) [4]	3	2.8	2.6	2.4	2.2	2.1	1.7
Is	Equivalent oxide thickness (electrical) (nm) [4]	3	2.8	2.6	2.4	2.2	2.1	1.7
	Nominal LOP power supply voltage (V_{dd}) (V) [5]	1.2	1.2	1.1	1.1	1	1	0.9
	Nominal LOP NMOS sub-threshold leakage current, $I_{sd,leak}$ (@25C) (pA/ μ m) [6]	100	100	100	300	300	300	700
	Nominal LOP NMOS Saturation drive current, I_{dd} (@ V_{dd} , @25C) (μ A/ μ m) [7]	600	600	600	600	600	600	700
	Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
	LOP NMOS Device τ ($C_{gate} * V_{dd} / I_d$ -NMOS) (ps) [9]	2.55	2.45	2.02	1.84	1.58	1.41	1.14
	LOP relative device performance [10]	1	1.04	1.3	1.4	1.6	1.8	2.2
Was	Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate} * (3 * L_{gate}) * V_{dd}^2$) (fJ/Device) [11]	0.496	0.424	0.26	0.193	0.128	0.094	0.069
Is	Power-delay product for ($W/L_{gate}=3$) device $[C_{gate} * (3 * L_{gate}) * V_{dd}^2]$ (fJ/Device) [14]	0.496	0.424	0.26	0.193	0.128	0.094	0.069
	Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	3.20E-11	2.90E-11	2.10E-11	5.20E-11	4.10E-11	3.30E-11	6.00E-11

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Table 36b Low Operating Power (LOP) Logic Technology Requirements—Long-term

Year of Production		2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Physical gate length low-operating power (LOP) (nm) [1]	22	16	11
Was	Equivalent physical oxide thickness for LOP T_{ox} (EOT) (nm) [2]	0.8-1.2	0.7-1.1	0.6-1.0
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.8-1.2	0.7-1.1	0.6-1.0
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.5	0.5	0.5
Was	T_{ox} electrical equivalent (nm) [4]	1.5	1.4	1.3
Is	Equivalent oxide thickness (electrical) (nm) [4]	1.5	1.4	1.3
	Nominal LOP power supply voltage (V_{dd}) (V) [5]	0.8	0.7	0.6
	Nominal LOP NMOS sub-threshold leakage current, $I_{sd,leak}$ (@25C) (pA/ μ m) [6]	1000	3000	10000
	Nominal LOP NMOS saturation drive current, I_{dd} (@ V_{dd} , @25C) (μ A/ μ m) [7]	700	800	900
	Required percent current-drive "mobility/transconductance improvement" [8]	10%	30%	70%
	LOP NMOS device τ ($C_{gate} * V_{dd} / I_{dd}$ -NMOS) (ps) [9]	0.85	0.56	0.35
	LOP relative device Performance [10]	3	4.6	7.2
Was	Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate} * (3 * L_{gate}) * V^2$) (fJ/Device) [11]	0.032	0.015	0.006
Is	Power-delay product for ($W/L_{gate}=3$) device [$C_{gate} * (3 * L_{gate}) * V_{dd}^2$] (fJ/Device) [14]	0.032	0.015	0.006
	Static power dissipation per ($W/L_{gate}=3$) device (Watts/Device) [12]	5.30E-11	1.00E-10	2.00E-10

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Red—Manufacturable Solutions are NOT Known



Table 36c Low Standby Power (LSTP) Technology Requirements—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was	Physical gate length low-standby power (LSTP) (nm) [1]	90	75	65	53	45	37	32
Is	Physical gate length low-standby power (LSTP) (nm) [1]	100	90	75	65	53	45	37
Was	Equivalent physical oxide thickness for LSTP T_{ox} (EOT) (nm) [2]	2.4–2.8	2.2–2.6	2.0–2.4	1.8–2.2	1.6–2.0	1.4–1.8	1.2–1.6
Is	EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	2.4–2.8	2.2–2.6	2.0–2.4	1.8–2.2	1.6–2.0	1.4–1.8	1.2–1.6
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Was	T_{ox} electrical equivalent (nm) [4]	3.4	3.2	3	2.8	2.6	2.4	1.9
Is	Equivalent oxide thickness (electrical) (nm) [4]	3.4	3.2	3	2.8	2.6	2.4	1.9
	Nominal LSTP power supply voltage (V_{dd}) (V) [5]	1.2	1.2	1.2	1.2	1.2	1.2	1.1
	Nominal LSTP NMOS sub-threshold current (at 25 °C) ($pA/\mu m$) [6]	1	1	1	1	1	1	1
	Nominal LSTP NMOS saturation current drive (I_{dd}) (at V_{dd} , at 25 °C) ($mA/\mu m$) [7]	300	300	400	400	400	400	500
	Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
Was	LSTP NMOS device τ ($C_{gate} * V_{dd} / I_d$ -NMOS) (ps) [9]	4.61	4.41	2.96	2.68	2.51	2.32	1.81
Is	LSTP NMOS device τ ($C_{gate} * V_{dd} / I_d$ -NMOS) (ps) [9]	5.02	4.84	3.31	3.12	2.83	2.66	2.01
Was	LSTP relative device performance [10]	1	1.05	1.6	1.7	1.8	2	2.6
Is	LSTP relative device performance [10]	1	1.04	1.52	1.61	1.77	1.89	2.50
Was	Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate} * (3 * L_{gate}) * V_{dd}^2$) (fJ/device) [11]	0.448	0.381	0.277	0.204	0.163	0.123	0.095
Is	Power-delay product for ($W/L_{gate}=3$) device $I_{C_{gate}} * (3 * L_{gate}) * V_{dd}^2 L$ (fJ/Device) [14]	0.542	0.471	0.357	0.292	0.216	0.172	0.122
Was	Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	3.20E-13	2.90E-13	2.30E-13	1.90E-13	1.60E-13	1.30E-13	1.10E-13
Is	Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	3.60E-13	3.24E-13	2.70E-13	2.34E-13	1.91E-13	1.62E-13	1.22E-13

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Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Table 36d Low Standby Power (LSTP) Technology Requirements—Long-term

Year of Production		2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
Was	Physical gate length low-standby power (LSTP) (nm) [1]	22	16	11
Is	Physical gate length low-standby power (LSTP) (nm) [1]	28	20	16
Was	Equivalent physical oxide thickness for LSTP T_{ox} (EOT) (nm) [2]	0.9-1.3	0.8-1.2	0.7-1.1
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.9-1.3	0.8-1.2	0.7-1.1
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.5	0.5	0.5
Was	T_{ox} electrical equivalent (nm) [4]	1.6	1.5	1.4
Is	Equivalent oxide thickness (electrical) (nm) [4]	1.6	1.5	1.4
	Nominal LSTP power supply voltage (V_{dd}) (V) [5]	1	0.9	0.9
	Nominal LSTP NMOS sub-threshold current (at 25°C) ($pA/\mu m$) [6]	3	7	10
	Nominal LSTP NMOS saturation current drive (I_{dd}) (at V_{dd} , at 25°C) ($\mu A/\mu m$) [7]	500	600	700
	Required percent current-drive "mobility/transconductance improvement" [8]	10%	30%	50%
Was	LSTP NMOS device τ ($C_{gate} * V_{dd} / I_{d-NMOS}$) (ps) [9]	1.43	0.91	0.66
Is	LSTP NMOS device τ ($C_{gate} * V_{dd} / I_{d-NMOS}$) (ps) [9]	1.69	1.05	0.82
Was	LSTP relative device performance [10]	3.2	5.1	7
Is	LSTP relative device performance [10]	2.97	4.78	6.15
Was	Energy per ($W/L_{gate}=3$) device switching transition ($C_{gate}*(3*L_{gate})*V^2$) (fJ/device) [11]	0.047	0.024	0.014
Is	Power-delay product for ($W/L_{gate}=3$) device [$C_{gate}*(3*L_{gate})*V_{dd}^2$] (fJ/Device) [14]	0.071	0.034	0.025
Was	Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	2.00E-13	3.00E-13	3.00E-13
Is	Static power dissipation per ($W/L_{gate}=3$) device (Watts/device) [12]	2.52E-13	3.78E-13	4.32E-13

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Notes for Table 36a through d:

[1] Values set by ORTC.

[1] Values set by ORTC. Assumed to lag high-performance scaling by 2 years. Gate dimensional control is set by the Lithography and FEP (Etch) ITWGs and is assumed to have a three sigma value of $\pm 10\%$. Gate dimension variation is assumed to be the primary factor responsible for driving device parameter variation. Gate length for the LOP and LSTP devices are assumed to be identical.

Was	[2] EOT value set by FEP ITWG in the Front End Processes chapter, Thermal and Thin Film, Doping, and Etching Technology Requirements tables Yellow/red feasibility coloring set by FEP ITWG projections on gate leakage, thickness control and reliability capability (high κ gate dielectrics will be required around 2005 in order to suppress gate leakage for LSTP). Due to different system applications, the EOT values for the LOP and LSTP devices have been optimized and set independently of each other. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values
Is	[2]] EOT value set by FEP ITWG in the Front End Processes chapter, Thermal and Thin Film, Doping, and Etching Technology Requirements tables Yellow/red feasibility coloring set by FEP ITWG projections on gate leakage, thickness control and reliability capability (high κ gate dielectrics will be required around 2005 in order to suppress gate leakage for LSTP). Due to different system applications, the EOT values for the LOP and LSTP devices have been optimized and set independently of each other. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values. <u>For a gate dielectric of thickness T_d and relative dielectric constant κ, EOT is defined by: $EOT = T_d / (\kappa/3.9)$, where 3.9 is the relative dielectric constant of thermal silicon dioxide. The ideal gate capacitance per unit area of the gate dielectric of thickness T_d is the same as that of a gate dielectric made up of thermal silicon dioxide with a thickness of EOT.</u>
	[3] Accounts for gate electrode depletion and inversion-layer quantum effects. Yellow feasibility coloring reflects FEP assessment of polysilicon doping capability; red feasibility coloring reflects the introduction of metal-gate electrodes by 2007 (which reduces the gate depletion value).
	[4] Sum of midpoint EOT and Electrical Thickness Adjustment Factor. Used in CV/I performance metric and CV ² dynamic power metric calculations. Red/yellow feasibility coloring determined by worst-case EOT and Electrical Thickness Adjustment Factor red/yellow feasibility coloring.
Was	[5] Nominal power supply voltage which has been set to smallest value to still maintain sufficient voltage over-drive to allow sufficient circuit switching noise margin (approximately 2.3 times the threshold voltage). Actual power supply voltage values may vary $\pm 10\%$, depending on the particular circuit design application or technology optimization. Due to different system applications, the power-supply voltages for the LOP and LSTP devices have been optimized and set independently of each other. Note, meeting overall system power dissipation requirements will require the use of circuit/system techniques to "turn-off" or "power-down" various circuit blocks.
Is	[5] Nominal power supply voltage which has been set to smallest value to still maintain sufficient voltage over-drive to allow sufficient circuit switching noise margin (approximately 2.3 times the threshold voltage). Actual power supply voltage target values may vary $\pm 10\%$, depending on the particular circuit design application or technology optimization. Due to different system applications, the power-supply voltages for the LOP and LSTP devices have been optimized and set independently of each other. Note, meeting overall system power dissipation requirements will require the use of circuit/system techniques to "turn-off" or "power-down" various circuit blocks.
Was	[6] Nominal sub-threshold leakage current is defined as the NMOSFET source current at room temperature with the drain bias set equal to the nominal power-supply voltage and with the gate, source, and substrate biases set to zero volts; all MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current at room temperature, and is the sum of the NMOS sub-threshold, gate, and junction leakage current components. The sub-threshold leakage current is assumed to be larger than either the gate or junction current components at either room or high-temperature conditions. The increase in sub-threshold current (and the corresponding threshold-voltage value reduction) has been set at a pace that lags the rate of increase of the high-performance device, but that still increases sufficiently to enable continued device performance scaling; power dissipation due to off-state leakage is assumed to not exceed 10% of the total chip power, which is assumed to be 100mW in 2001 and 200mW in 2010 for LOP. For LOP, the yellow feasibility coloring reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride films and the potential need for non-classical CMOS or ultra-shallow junction technology by 2007 to control short-channel effects and to limit lateral high-field effects. For LSTP, the yellow feasibility coloring in 2003 and 2004 reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride gate dielectric films, while the red feasibility color from 2005 on reflects the difficulty of implementing a high κ gate dielectric to meet the gate leakage requirements. The above sub-threshold, gate, and junction current scaling scenario also applies to PMOS devices.
Is	[6]] Nominal sub-threshold leakage current is defined as the NMOSFET source current at room temperature with the drain bias set equal to the nominal power-supply voltage and with the gate, source, and substrate biases set to zero volts; all MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current at room temperature, and is the sum of the NMOS sub-threshold, gate, and junction leakage current components. The sub-threshold leakage current is assumed to be larger than either the gate or junction current components at either room or high-temperature conditions. The increase in sub-threshold current (and the corresponding threshold-voltage value reduction) has been set at a pace that lags the rate of increase of the high-performance device, but that still increases sufficiently to enable continued device performance scaling; power dissipation due to off-state leakage is assumed to not exceed 10% of the total chip power, which is assumed to be 100mW in 2001 and 200mW in 2010 for LOP. For LOP, the yellow feasibility coloring reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride films and the potential need for non-classical CMOS or ultra-shallow junction technology by 2007 to control short-channel effects and to limit lateral high-field effects. For LSTP, the yellow feasibility coloring in 2003 and 2004 reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride gate dielectric films, while the red feasibility color from 2005 on reflects the difficulty of implementing a high κ gate dielectric to meet the gate leakage requirements. The above sub-threshold, gate, and junction current scaling scenario also applies to PMOS devices.

Notes for Table 36a through d (continued):

[7] Nominal saturation current drive is defined as the MOSFET drain current at room temperature with the gate bias and the drain bias set equal to the nominal power-supply voltage; all MOSFET device dimensions are assumed to be at their nominal/target values. Nominal PMOS saturation current-drive value is assumed to be 40–50% of the nominal NMOS saturation current-drive value. Yellow/red feasibility coloring indicates the projected need for fundamental device current-drive (transconductance/mobility) improvement by 2010 in order to continue approximate 14% per year device performance scaling. NMOS/PMOS current-drive targets are approximate with only 1.5 significant digits of accuracy. The sub-threshold slope, parasitic source/drain resistance, and parasitic gate capacitance scaling have been assumed to be similar to that for the high-performance device. (See the enclosed Excel workbook for the detailed calculations).

[8] Fundamental device mobility/transconductance improvement needed by 2010 in order to continue historical approximate 14% per year device performance scaling. Yellow/red feasibility coloring indicates the difficulty of implementing the fundamental device current-drive (transconductance/mobility) improvement required in 2010 and beyond to continue historical approximate 14% per year device performance scaling. The LOP and LSTP required improvement is projected as lagging that required for the high-performance device.

Was	[9] $\tau = CV/I$ intrinsic delay metric for NMOS device; PMOS CV/I metric assumed to scale proportionally. The CV/I metric provides an indication of the intrinsic switching delay of the device, while $1/\tau$, the reciprocal of CV/I , is a good metric for the intrinsic switching speed of the device. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. The C term includes the effect of parasitic gate capacitance, which has been assumed to be equivalent to that for the high-performance device.
Is	[9]] $\tau = CV/I$ intrinsic delay metric for NMOS device; PMOS CV/I metric assumed to scale proportionally. The CV/I metric provides an indication of the intrinsic switching delay of the device, while $1/\tau$, the reciprocal of CV/I , is a good metric for the intrinsic switching speed of the device. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. The C (gate capacitance) includes the effect of parasitic gate capacitance, which has been assumed to be equivalent to that for the high-performance device. For LSTP, τ has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.
Was	[10] Improvement in $1/\tau$ NMOS performance metric normalized to the year 2001. Maintains approximate 14% per year device performance improvement scaling trend for both LOP and LSTP. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring.
Is	[10] [10] Improvement in $1/\tau$ NMOS performance metric normalized to the year 2001. Maintains approximate 14% per year device performance improvement scaling trend for both LOP and LSTP. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. For LSTP, $1/\tau$ has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.
Was	[11] CV^2 switching energy metric for an NMOS device with dimensions $W/L_{gate}=3$. The switching energy metric indicates the amount of dynamic power required to switch the device. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring.
Is	[11]] CV^2 switching energy metric for an NMOS device with dimensions $W/L_{gate}=3$. The power-delay product indicates the amount of dynamic energy required to switch the device through a full (up and down) transition . Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. For LSTP, the power-delay product has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.
Was	[12] Static power dissipation for an NMOS device with dimensions $W/L_{gate}=3$. Assume that the device static power is primarily determined by the sub-threshold current (since the other junction and leakage current components are assumed to be lower). Yellow/red feasibility coloring is determined by the sub-threshold leakage current feasibility coloring.
Is	[12] Static power dissipation for an NMOS device with dimensions $W/L_{gate}=3$. Assume that the device static power is primarily determined by the sub-threshold current (since the other junction and leakage current components are assumed to be lower). Yellow/red feasibility coloring is determined by the sub-threshold leakage current feasibility coloring. For LSTP, the static power dissipation per device has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.

Table 37a DRAM Technology Requirements—Near-term

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)[1]	130	115	100	90	80	70	65
MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
DRAM cell size (μm^2) [2]	0.135	0.106	0.06	0.049	0.038	0.029	0.025
DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	2.04	1.8	1.2	1	0.45	0.32	0.22
Was DRAM retention time (ms) [4]	64	64	64	64	64	64	64
Is <u>Minimum</u> DRAM retention time (ms) [4]	64	64	64	64	64	64	64
DRAM soft error rate (fits) [5]	1000	1000	1000	1000	1000	1000	1000

Table 37b DRAM Technology Requirements—Long-term

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm) [1]	45	32	22
MPU / ASIC ½ Pitch (nm)	50	35	25
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
DRAM cell size (μm^2) [2]	0.0122	0.0041	0.0019
DRAM storage cell dielectric: equivalent physical oxide thickness, EOT (nm) [3]	0.084	0.028	0.01
Was DRAM retention time (ms) [4]	64	64	64
Is <u>Minimum</u> DRAM retention time (ms) [4]	64	64	64
DRAM soft error rate (fits) [5]	1000	1000	1000

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



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Notes for Table 37a and b:

Was	[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are smaller than those in the 2000 ITRS, reflecting a speedup in technology development since 1999.
Is	[1]] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are smaller than those in the 2000 ITRS, reflecting a speedup in technology development since 1999. <u>However, there is no clear evidence for a further speed up in the pace of DRAM half pitch scaling during 2001 and the early part of 2002.</u>
Was	[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F ²), and F is the DRAM half pitch. The required values of "a" are 8 for the 130nm node, 6 for 100nm DRAM half pitch, and 4 for the 32nm node. The "a" value of 8 is probably achievable with current techniques, but the "a" value of 6 will require innovative solutions, as illustrated with yellow zone in this line, while the "a" value of 4 has no known solution for 32nm node and beyond, as illustrated with red zone.
Is	[2]] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F ²), and F is the DRAM half pitch. The required values of "a" are 8 for the 130nm node, 6 for 100nm DRAM half pitch <u>in 2003</u> , and 4 for the 32nm node. The "a" value of 8 is probably achievable with current techniques, but the "a" value of 6 will require innovative solutions, as illustrated with yellow zone in this line, <u>and may be difficult for the industry to achieve per schedule in 2003.</u> The "a" value of 4 has no known solution for 32nm node and beyond, as illustrated with red zone.
Was	[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. For the 130nm through the 90 nm nodes, the dielectric material is based on Al ₂ O ₃ or Ta ₂ O ₅ with MIS structure, and hence the color is white. Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.
Is	[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. For the 130nm through the 90 nm nodes, the dielectric material is based on Al ₂ O ₃ or Ta ₂ O ₅ with MIS structure, and hence the color is white. <u>(Note that, notwithstanding the trend to Al₂O₃ or Ta₂O₅, many vendors still used oxide-nitride-oxide (ONO) dielectric in 2001.)</u> Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.

[4] Retention time is defined at 85 °C, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

[5] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

Table 38a Non-Volatile Memory Technology Requirements—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was	Flash technology node - F (nm) [1]	150	130	115	100	90	80	70
Is	Flash technology node - F (nm) [1]	150	130	107	90	80	70	65
	Flash NOR cell size—area factor a in multiples of F ² [2]	10–12	10–12	10–12	11–14	11–14	11–14	11–14
Was	Flash NAND cell size—area factor a in multiples of F ² SLC/MLC [3]	5.5	5.5	4.5	4.5	4.5	4.5/2.3	4.5/2.3
Is	Flash NAND cell size—area factor a in multiples of F ² SLC/MLC [3]	5.5	5.5	5.5	5.5	5.5	5.5	4.5
Was	Flash NOR typical cell size (µm ²) [4]	0.248	0.186	0.145	0.125	0.101	0.08	0.061
Is	Flash NOR typical cell size (µm ²) [4]	0.248	0.186	0.135	0.101	0.08	0.061	0.061
Was	Flash NOR Lg-stack (physical- µm) [5]	0.29–0.31	0.25–0.27	0.22–0.24	0.21–0.23	0.2–0.22	0.2–0.22	0.19–0.21
Is	Flash NOR Lg-stack (physical- µm) [5]	0.29–0.31	0.25–0.27	0.22–0.24	0.2–0.22	0.2–0.22	0.19–0.21	0.19–0.21
Was	Flash NOR highest W/E voltage (V) [6]	8–10	8–10	8–10	8–10	7–9	7–9	7–9
Is	Flash NOR highest W/E voltage (V) [6]	8–10	8–10	8–10	7–9	7–9	7–9	7–9
Was	Flash NAND highest W/E voltage (V) [7]	19–21	18–20	18–20	18–20	18–20	17–19	17–19
Is	Flash NAND highest W/E voltage (V) [7]	19–21	18–20	18–20	17–19	17–19	17–19	15–17
Was	Flash NOR I _{read} (µA) [8]	36–44	35–43	34–42	33–41	31–39	28–36	29–37
Is	Flash NOR I _{read} (µA) [8]	36–44	35–43	34–42	31–39	29–37	28–36	27–35
Was	Flash Coupling Ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7
Is	Flash Coupling Ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7	0.6–0.7
Was	Flash NOR tunnel oxide thickness (nm) [10]	9.5–10.5	9.5–10	9–10	9–10	8.5–9.5	8.5–9.5	8.5–9.5
Is	Flash NOR tunnel oxide thickness (nm) [10]	9.5–10.5	9–10	9–10	8.5–9.5	8.5–9.5	8.5–9.5	8–9
Was	Flash NAND tunnel oxide thickness (nm) [11]	8.5–9.5	8.5–9	8–9	8–9	8–9	7.5–8	7.5–8
Is	Flash NAND tunnel oxide thickness (nm) [11]	8.5–9.5	7–8	7–8	7–8	7–8	7–8	6–7
Was	Flash NOR interpoly dielectric thickness (nm) [12]	13–15	12–14	11–13	11–13	10–12	9–11	9–11
Is	Flash NOR interpoly dielectric thickness (nm) [12]	13–15	12–14	11–13	10–12	9–11	9–11	8.5–10.5
Was	Flash NAND interpoly dielectric thickness (nm) [13]	14–16	13–15	12–14	12–14	12–14	11–13	10–12
Is	Flash NAND interpoly dielectric thickness (nm) [13]	14–16	13–15	13–15	13–15	13–15	13–15	10–13
	Flash endurance (erase/write cycles) [14]	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05
	Flash nonvolatile data retention (years) [15]	10	10–20	10–20	10–20	10–20	10–20	10–20
	Flash maximum number of bits per cell (MLC) [16]	2	2	4	4	4	4	4
	FeRAM technology node - F (nm) [17]	500	350	250	220	180	150	130
	FeRAM cell size—area factor a in multiples of F ² [18]	60	40	24	16	10	10	10
	FeRAM cell size (µm ²) [19]	15	4.9	1.5	0.518	0.324	0.225	0.169
	FeRAM cell structure [20]	2T2C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
	FeRAM capacitor structure [21]	planar	planar	stack	stack	stack	stack	3D
	Ferro capacitor voltage (V) [22]	3	3	2.5	1.8	1.5	1.3	1.2
	FeRAM endurance (read/write cycles) [23]	1.00E+12	1.00E+13	1.00E+14	1.00E+15	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [24]	10	10	10	10	10	10	10

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Table 38b Non-Volatile Memory Technology Requirements—Long-term

Year of Production		2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Flash technology node - F (nm) [1]	50	35	25
	Flash NOR cell size —area factor a in multiples of F ² [2]	12–15	13–16	14–17
	Flash NAND cell size —area factor a in multiples of F ² SLC/MLC [3]	4.5/2.3	4.5/2.3	4.5/2.3
	Flash NOR typical cell size (µm ²) [4]	0.034	0.018	0.01
	Flash NOR Lg-stack (physical- µm) [5]	0.17–0.19	0.14–0.16	0.12–0.14
	Flash NOR highest W/E voltage (V) [6]	7–9	7–9	7–9
Was	Flash NAND highest W/E voltage (V) [7]	17–19	16–18	16–18
Is	Flash NAND highest W/E voltage (V) [7]	15-17	15-17	15-17
	Flash NOR I _{read} (µA) [8]	27–33	25–31	22–28
	Flash Coupling Ratio [9]	0.6–0.7	0.6–0.7	0.6–0.7
	Flash NOR tunnel oxide thickness (nm) [10]	8–9	8	8
	Flash NAND tunnel oxide thickness (nm) [11]	6–7	6–7	6–7
	Flash NOR interpoly dielectric thickness (nm) [12]	8–10	6–8	4–6
Was	Flash NAND interpoly dielectric thickness (nm) [13]	10–12	9–11	9–11
Is	Flash NAND interpoly dielectric thickness (nm) [13]	10-13	9-10	9-10
	Flash endurance (erase/write cycles) [14]	1.00E+06	1.00E+06	1.00E+07
	Flash nonvolatile data retention (years) [15]	10–20	20	20
	Flash maximum number of bits per cell (MLC) [16]	8	8	8
	FeRAM technology node - F (nm) [17]	100	70	50
	FeRAM cell size —area factor a in multiples of F ² [18]	8	8	8
	FeRAM cell size (µm ²) [19]	0.08	0.039	0.02
	FeRAM cell structure [20]	1T1C	1T1C	1T1C
	FeRAM capacitor structure [21]	3D	3D	3D
	Ferro capacitor voltage (V) [22]	1	0.7	0.7
	FeRAM endurance (read/write cycles) [23]	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [24]	10	10	10

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

