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Defect Reduction Cross-Cut Technology Working Group 2001 Version

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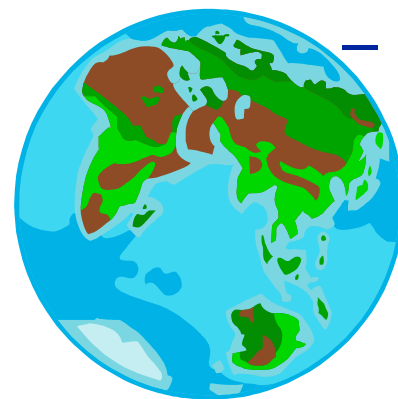
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International Technology Roadmap for Semiconductors



2001 ITRS Defect Reduction US Domestic TWG Membership

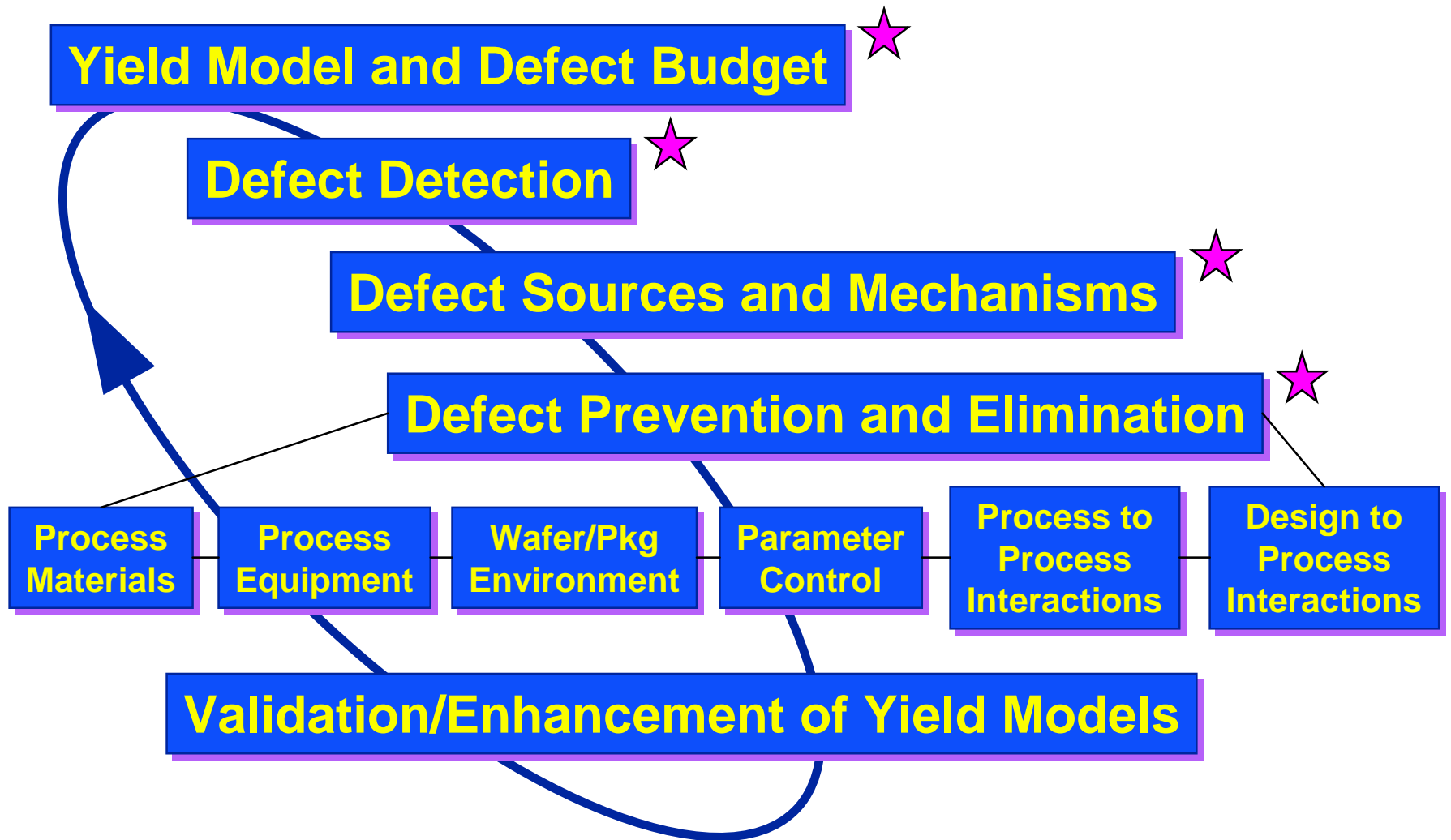
Yield Model and Defect Budget		Defect Sources and Mechanisms	
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2001 ITRS Defect Reduction JEITA WG11 Membership

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Defect Reduction TWG Yield Learning Cycle

★ Focus Topics



International Technology Roadmap for Semiconductors



Proposed Name Change

- In order to align this chapter with the industry from a yield improvement perspective we propose the following name changes:
- Chapter: Defect Reduction -> Yield Enhancement
- Sub Chapters:
 - Yield Modeling and Defect Budget
 - Defect Detection -> Defect Detection and Characterization
 - Defect Sources and Mechanisms -> Yield Learning
 - Defect Prevention and Elimination -> Wafer Environment Contamination Control

Technology Requirements:

Yield Model and Defect Budget

- **GOAL:** Provide reasonable and credible defect targets for tool suppliers
- **Approach Defect budget requirements for the 2001 ITRS:**
 - use results of a 1997, 1999, 2000 studies of current process-induced defects (PID) at Intl. SEMATECH Member Companies.
 - Calculation based on the negative binomial yield model

$$Y_{sort} = Y_s * Y_r = Y_s * \left\{ \frac{1}{\left(1 + \frac{AD}{\alpha}\right)^\alpha} \right\}$$

Y_{sort} = Probe Yield
Y_s = Systematic Limited Yield
Y_r = Random Defect Limited Yield
A = Chip Area (m²)
D₀ = Electrical Fault Density (/m²)
α = Cluster Factor

Technology Requirements: Yield Model and Defect Budget

- **Extrapolation for future technology node requirements:**

- from median PID value for typical tool in each process module by considering increase in area, increase in complexity, and shrinking feature size.

$$PID_n = PID_{n-1} * \frac{F_n}{F_{n-1} \left(\frac{S_{n-1}}{S_n} \right)}$$

Where:

PID = Process Induced Defects (/m²)

n = Technology Node of Interest

F = Faults per Mask

S = Minimum Defect Size (nm)

- **Key assumption:**

- No new process, material, or tool will be acceptable with a larger PID budget than prior processing methods.
- Defect budgeting method tends to be a worst case model since all process steps are assumed to be at minimum device geometry.

Technology Requirements: MPU/DRAM Fault Density Assumptions

- Assumptions defined in the “Overall Requirements Table Chapter” (ORTC) by the ITRS Die Size WG with $Y_{\text{sort}} = Y_s * Y_r$

P r o d u c t	<i>M P U</i>	<i>D R A M</i>
Yield Ramp Phase	<i>R A M P P H A S E E N D</i>	<i>P R O D U C T I O N P H A S E E N D</i>
Y_{OVERALL}	75 %	85 %
Y_{RANDOM}	83 %	89.5 %
Y_{SYSTEMATIC}	90 %	95 %
Cluster Parameter	5	5
Chip Size	170 mm ² through 2002, then increasing	132 mm ² in 1999, then increasing

- With this assumption Defect Budget Targets for MPU and DRAM were calculated

Yield Model and Defect Budget Tables 76-77

Key 2001 Updates

- Defect budget target calculation makes use of data from 3 different surveys of ISMT Member Companies (1997, 1999, 2000)
- Defect budget targets include wafer-handling defectivity, for 2001 reduced # of handling steps in generic process flow
- DRAM defect budget targets not extrapolated from the MPU data, but calculated based on a generic DRAM process flow
- Key assumptions:
 - Random & systematic yield targets same as 1999/2000
 - Model assumes that redundancy is sufficient such that array is not limiting DRAM yield
 - All process steps are at minimum device geometry

Yield Model and Defect Budget Tables 76-77

Key 2001 Updates

- **Technology requirement color-code determined by tool yield impact partitioning study**
- **Propose including a calculator for DRAM & MPU tool defect budget targets**
 - Critical Defect Size, RDLY target, Die Size, # Mask Levels and Cell area user definable

Table 76: YMDB - MPU

Technology Requirements -

Table 76 Yield Model and Defect Budget MPU Technology Requirements										
<i>Year of Introduction</i>	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
<i>"Technology Node" (IS)</i>	130n	115	100n	90nm	80nm	70nm	65nm	45nm	32nm	22nm
MPU										
MPU 1/2 Pitch (A)	150	130	105	90	80	70	65	45	32	22
Critical Defect Size	75	65	53	45	40	35	33	23	16	11
Chip Size (B)	170	178	186	195	204	214	223	256	294	337
Overall Electrical D0 (faults/m ²) at critical defect size or greater (C)	1742	1664	1590	1519	1452	1387	1325	1157	1007	879
Random D0 * (faults/m ²) (D)	1117	1067	1019	974	931	889	850	742	646	563
# Mask Levels (E)	23	24	24	24	25	27	28	29	29	29
Random Faults/Mask	49	44	42	41	37	33	30	26	22	19

Table 76: YMDB - MPU

Technology Requirements - continued

Year of Introduction "Technology Node" (IS)	2001 130n	2002 115	2003 100n	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
MPU Random Process Induced Defect (PID) Budget (defects/m²) for Generic Tool Type scaled to 75nm critical defect size or greater (F)										
CMP Clean	250	172	107	75	55	37	29	12	5	2
CMP Insulator	605	416	259	182	132	89	71	29	13	5
CMP Metal	683	470	293	206	149	101	80	32	14	6
Coat/Develop/Bake	109	75	47	33	24	16	13	5	2	1
CVD Insulator	537	370	230	162	117	79	63	25	11	5
CVD Oxide Mask	707	486	303	213	154	104	83	33	15	6
Dielectric Track	172	118	74	52	38	25	20	8	4	1
Furnace CVD	306	211	131	92	67	45	36	15	6	3
Furnace Fast Ramp	277	191	119	83	60	41	33	13	6	2
Furnace Oxide/Anneal	179	123	77	54	39	26	21	8	4	2
Implant High Current	240	165	103	72	52	35	28	11	5	2
Implant Low/Med Current	219	150	94	66	48	32	26	10	5	2
Inspect PLY	223	153	96	67	49	33	26	11	5	2
Inspect Visual	240	165	103	72	52	35	28	11	5	2
Litho Cell	185	128	79	56	40	27	22	9	4	2
Litho Stepper	176	121	75	53	38	26	21	8	4	2

Table 76: YMDB - MPU

Technology Requirements - continued

Year of Introduction "Technology Node" (IS)	2001 130n	2002 115	2003 100n	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
MPU Random Process Induced Defect (PID) Budget (defects/m²) for Generic Tool Type										
scaled to 75nm critical defect size or greater (F)										
Measure CD	209	144	89	63	46	31	24	10	4	2
Measure Film	179	123	77	54	39	26	21	9	4	2
Measure Overlay	166	114	71	50	36	25	20	8	3	1
Metal CVD	326	224	140	98	71	48	38	15	7	3
Metal Electroplate	168	116	72	51	37	25	20	8	4	1
Metal Etch	725	499	311	218	158	107	85	34	15	6
Metal PVD	372	256	160	112	81	55	44	18	8	3
Plasma Etch	660	454	283	199	144	97	77	31	14	6
Plasma Strip	305	210	131	92	67	45	36	14	6	3
RTP CVD	199	137	85	60	43	29	23	9	4	2
RTP Oxide/Anneal	130	90	56	39	28	19	15	6	3	1
Test	51	35	22	15	11	8	6	2	1	0
Vapor Phase Clean	458	315	196	138	100	68	54	22	10	4
Wafer Handling	21	14	9	6	4	3	2	1.0	0.4	0.2
Wet Bench	298	205	128	90	65	44	35	14	6	3

Table 77: YMDB - DRAM

Technology Requirements

Year of Introduction "Technology Node" (IS)	2001 130nm	2002 115 nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
DRAM										
DRAM / ASIC 1/2 Pitch (A)	130	115	100	90	80	70	65	45	32	22
Critical Defect Size	65	58	50	45	40	35	33	23	16	11
Chip Size (B)	127	141	157	175	147	164	183	256	239	274
Cell Array Area % @ Production	0.55	0.55	0.56	0.56	0.56	0.57	0.57	0.58	0.58	0.58
Non-Core Area	57	63	69	77	64	71	79	108	100	114
Overall Electrical D0 (faults/m ²) at critical defect size or greater (C)	2880	2622	2377	2151	2580	2329	2100	1524	1650	1450
Random D0 * (faults/m ²) (D)	1956	1780	1614	1461	1752	1581	1426	1035	1120	985
# Mask Levels (E)	20	21	21	21	22	24	25	26	26	26
Random Faults/Mask	98	85	77	70	80	66	57	40	43	38

Table 77: YMDB - DRAM

Technology Requirements – continued

Year of Introduction "Technology Node" (IS)	2001 130n	2002 115	2003 100n	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
DRAM Random Process Induced Defect (PID) Budget (defects/m²) for Generic Tool Type										
scaled to 75nm critical defect size or greater (F)										
CMP Clean	650	441	302	222	201	127	95	32	17	7
CMP Insulator	503	341	234	171	155	98	73	25	13	6
CMP Metal	771	523	359	263	238	151	112	38	21	9
Coat/Develop/Bake	201	136	93	69	62	39	29	10	5	2
CVD Insulator	558	378	259	190	172	109	81	27	15	6
CVD Oxide Mask	684	464	318	233	211	134	100	33	18	8
Dielectric Track	282	191	131	96	87	55	41	14	8	3
Furnace CVD	385	261	179	131	119	75	56	19	10	4
Furnace Fast Ramp	363	246	169	124	112	71	53	18	10	4
Furnace Oxide/Anneal	290	197	135	99	90	57	42	14	8	3
Implant High Current	337	229	157	115	104	66	49	16	9	4
Implant Low/Med Current	322	218	150	110	99	63	47	16	9	4
Inspect PLY	440	299	205	150	136	86	64	21	12	5
Inspect Visual	454	308	211	155	140	89	66	22	12	5
Litho Cell	377	256	175	129	116	74	55	18	10	4
Litho Stepper	251	170	117	85	77	49	37	12	7	3

Table 77: YMDB - DRAM

Technology Requirements – continued

Year of Introduction "Technology Node" (IS)	2001 130n	2002 115	2003 100n	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
DRAM Random Process Induced Defect (PID) Budget (defects/m²) for Generic Tool Type										
scaled to 75nm critical defect size or greater (F)										
Measure CD	376	255	175	128	116	73	55	18	10	4
Measure Film	354	240	165	121	109	69	52	17	9	4
Measure Overlay	344	234	160	117	106	67	50	17	9	4
Metal CVD	355	241	165	121	109	69	52	17	9	4
Metal Electroplate	270	183	125	92	83	53	39	13	7	3
Metal Etch	653	443	304	223	201	128	95	32	17	7
Metal PVD	389	264	181	133	120	76	57	19	10	4
Plasma Etch	691	469	321	236	213	135	101	34	18	8
Plasma Strip	531	360	247	181	164	104	77	26	14	6
RTP CVD	347	235	161	118	107	68	51	17	9	4
RTP Oxide/Anneal	254	172	118	87	78	50	37	12	7	3
Test	50	34	23	17	15	10	7	2	1	1
Vapor Phase Clean	734	498	341	250	226	143	107	36	20	8
Wafer Handling	21	14	10	7	6	4	3	1	1	0
Wet Bench	525	356	244	179	162	103	77	26	14	6

Defect Detection Table 78

Key 2001 Updates

- ITRS Node definition updated to reflect changes made to the ORTC Tables with respect to year/technology node.
- High Aspect Ratio inspection can only be achieved at extremely low throughput (1 wafer/hour) and high cost of ownership (\$20-\$50/wafer). Therefore, it is not a manufacturing process and is currently “red”.
- Backside particle size line was reinstated into Table 78 due to member interest.

Table 78: Defect Detection Technology Requirements - Short Term

Table 78: Technology Requirements for Defect Detection									
Short-term Years	NODE = 1/2 DRAM METAL 1 PITCH								
Year	2001	2002	2003	2004	2005	2006	2007	Driver	
Technology Node	130 nm	115	100	90 nm	80	70	65		
<i>Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[A, B]</i>									
Process R&D at 300 cm ² /hr (Was)	39	36	33	27	24	21	19	0.3 x DR	
Process R&D at 300 cm ² /hr - 1 W/hr (Is)	78	72	66	54	48	42	19.5	0.6 x DR	
Yield Ramp at 3000 cm ² /hr (Was)	52	48	44	36	31	28	26	0.4 x DR	
Yield Ramp at 1200 cm ² /hr - 4W/hr (Is)	104	96	88	72	56	56	52	0.8 x DR	
Volume Production at 10000 cm ² /hr (Was)	65	60	55	45	35	35	33	0.5 x DR	
Volume Production at 3000 cm ² /hr - 10W/hr (Is)	130	120	110	90	80	70	66	1.0 x DR	
<i>High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]</i>									
All stages of manufacturing (Was)	39	36	33	27	24	21	20	0.3 x DR	
All stages of manufacturing (Is)	130	120	110	90	80	70	65	1.0 x DR	
Process Verification - 1 W/hr	130	120	110	90	80	70	65	1.0 x DR	
Volume Manufacturing - 4 W/hr	130	120	110	90	80	70	65	1.0 x DR	
Cost of Ownership :Volume Man., Non-HARi, \$/wafer scanned, 10 /hr	2 - 5	2 - 5	2 - 5	3 - 7	3 - 7	3 - 7	3 - 7		
CoO HARi	20 - 50	20 - 50	20 - 50	20 - 50	20 - 50	20 - 50	20 - 50		

Table 78: Defect Detection

Technology Requirements - Short Term

Table 78: Technology Requirements for Defect Detection								
Short-term Years	NODE = 1/2 DRAM METAL 1 PITCH							
Year	2001	2002	2003	2004	2005	2006	2007	Driver
Technology Node	130 nm	115	100	90 nm	80	70	65	
<i>Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E, I]</i>								
Metal Film (Was)	51	47	43	35	30	21	19	0.3 x DR
Metal Film (Is)	91	85	77	32	56	35	33	0.5 x DR
Nonmetal Films (Was)	39	36	33	27	24	21	19	0.3 x DR
Nonmetal Films (Is)	70	65	59	49	43	35	33	0.5 x DR
Bare Silicon (Was)	39	36	33	27	24	21	19	0.3 x DR
Bare Silicon (Is)	70	65	59	49	43	35	33	0.5 x DR
Wafer Backside 200mm : # events flip method	2500	2000	2000	2000	2000	2000	1000	
Wafer Backside 200mm : Defect Size nm	200	200	200	200	100	100	100	
<i>Defect Review (Patterned wafer)</i>								
Resolution (nm) *[F]	7	7	6	5	5	4	3	0.05 x DR
Coordinate Accuracy (um) at Resolution	2	2	1	1	1	1	1	*
Coordinate Accuracy (um) at Size	15	12	12	10	10	7	7	
<i>Automatic Defect Classification at Defect Review Platform *[G, H]</i>								
Redetection: minimum defect size (nm)	52	48	44	36	30	28	26	0.4 x DR
Number of defect types (Was)	10	10	10	15	15	15	15	**
Number of defect types (Is)	10	10	12	12	15	15	15	**
Speed (seconds/defect)	7	5	5	5	5	5	5	
Speed - w/ elemental (seconds/defect)	20	15	13	10	10	10	10	

Table 78: Defect Detection

Technology Requirements – Long Term

Table 78: Technology Requirements for Defect Detection				
<i>Long-term Years</i>				
<i>Year</i>	<i>2010</i>	<i>2013</i>	<i>2016</i>	<i>Driver</i>
<i>Technology Node</i>	45 nm	32 nm	22 nm	
<i>Patterned Wafer Inspection, PSL Spheres at 90% Capture</i>				
Process R&D at 300 cm ² /hr (Was)	14	9.5	6.5	0.3 x DR
Process R&D at 300 cm ² /hr - 1 W/hr (Is)	27	19	13	0.6 x DR
Yield Ramp at 3000 cm ² /hr (Was)	18	13	9	0.4 x DR
Yield Ramp at 1200 cm ² /hr - 4W/hr (Is)	36	26	18	0.8 x DR
Volume Production at 10000 cm ² /hr (Was)	23	16	11	0.5 x DR
Volume Production at 3000 cm ² /hr - 10W/hr (Is)	46	32	22	1.0 x DR
<i>High Aspect Ratio Feature Inspection: Defects other than Residue</i>				
All stages of manufacturing (Was)	18	12	9	0.3 x DR
All stages of manufacturing (Is)	45	32	22	1.0 x DR
Process Verification - 1 W/hr	45	32	22	1.0 x DR
Volume Manufacturing - 4 W/hr	45	32	22	1.0 x DR
Cost of Ownership :Volume Man., Non-HARi, \$/wafer scanned, 10 /hr	3 - 7	3 - 5	3 - 5	

Table 78: Defect Detection

Technology Requirements – Long Term

Table 78: Technology Requirements for Defect Detection				
<i>Long-term Years</i>				
<i>Year</i>	<i>2010</i>	<i>2013</i>	<i>2016</i>	<i>Driver</i>
<i>Technology Node</i>	45 nm	32 nm	22 nm	
<i>Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E]</i>				
Metal Film (Was)	14	9.5	6.5	0.3 x DR
Metal Film (Is)	23	16	11	0.5 x DR
Nonmetal Films (Was)	14	9.5	6.5	0.3 x DR
Nonmetal Films (Is)	23	16	11	0.5 x DR
Bare Silicon (Was)	14	9.5	6.5	0.3 x DR
Bare Silicon (Is)	23	16	11	0.5 x DR
Wafer Backside 200mm : # events flip method	1000	1000	500	
Wafer Backside 200mm : Defect Size nm	100	60	50	
<i>Defect Review (Patterned wafer)</i>				
Resolution (nm) *[F]	3	2	2	0.05 x DR
Coordinate Accuracy (um) at Resolution	0.5	0.5	0.5	*
Coordinate Accuracy (um) at Size	5	5	5	
<i>Automatic Defect Classification at Defect Review Platform</i>				
Redetection: minimum defect size (nm)	18	13	9	0.4 x DR
Number of defect types (Was)	20	20	25	**
Number of defect types (Is)	20	20	25	**
Speed (seconds/defect)	5	5	5	
Speed - w/ elemental (seconds/defect)	10	10	10	

Yield Learning

Key 2001 Updates

- ITRS Node definition updated to reflect changes made to the ORTC Tables with respect to year/technology node.
- Yield Learning
 - The time necessary to source manufacturing problems is approximately 50% of the theoretical process cycle time on average during yield ramp
 - In order to keep the yield learning rate manageable, the process development and technology transfer to manufacturing must be optimized to minimize new defect sources/mechanisms during yield ramp.

Yield Learning

Key 2001 Updates

- **Yield Learning (continued)**
 - **Integrated Data Management (IDM) is critical for maintaining productivity comprehending**
 - **integrated circuit design**
 - **visible defects**
 - **non-visual defects**
 - **parametric data**
 - **electrical test faults**
 - **process trends and excursions**
 - **rapid identification of yield detracting mechanisms**

Table 79a: Yield Learning

Technology Requirements - Short Term

Table 79a: Technology Requirements for Yield Learning							
Short Term Years							
<i>Year of Production</i>	2001	2002	2003	2004	2005	2006	2007
<i>DRAM ½ Pitch (Sc. 2.0)</i>	130	115	100	90	80	70	65
<i>MPU Printed Gate Length (Sc. 3.7)</i>	90	75	65	53	45	40	35
<i>Wafer size (mm)</i>	300	300	300	300	300	300	300
<i>Wafer area (mm²)</i>	70714	70714	70714	70714	70714	70714	70714.29
<i>Number of mask levels</i>	25	25	25	27	27	27	29
<i>Number of processing steps</i>	490	503	516	530	543	556	570
<i>Cycle time during ramp (# days)</i>	25	25	25	27	27	27	29
<i>Defect/Fault Sourcing Complexity [A], [F]</i>							
<i>Logic transistor density/cm² (1E6)</i>	14	19	26	35	47	63	85
<i>Defect sourcing complexity factor (1E9) [B]</i>	7	10	13	18	25	35	49
<i>Defect sourcing complexity trend [C]</i>	1	1	2	3	4	5	7
<i>Data Analysis for Rapid Defect/Fault Sourcing</i>							
<i>Patt wfr insp sensitivity (nm) during yield ramp</i>	52	46	40	36	32	28	26
<i>Average # of inspections/wafer during full flow</i>	5	5	5	5.4	5.4	5.4	5.8
<i>(# data items/wafer) (1E13) [D]</i>	5.5	7.1	9.4	12.5	15.8	20.7	25.7
<i>Defect data volume (DV) trend [E]</i>	1	1	2	2	3	4	5
<i>Yield Learning During Ramp from 30% to 80% Sort Yield</i>							
<i># of yield learning cycles/year based on full flow cycle time</i>	14.6	14.6	14.6	13.5	13.5	13.5	12.6
<i>Required yield improvement rate per learning cycle</i>	3.4	3.4	3.4	3.7	3.7	3.7	4.0
<i>Time to identify & fix new defect/fault source during ramp</i>	12.5	12.5	12.5	13.5	13.5	13.5	14.5
<i># of learning cycles/yr for 1 defect/fault source/month</i>	8.6	8.6	8.6	7.5	7.5	7.5	6.6
<i>Req yld impr rate/learning cycle for 1 defect/fault source/month</i>	5.8	5.8	5.8	6.7	6.7	6.7	7.6
<i>Excursion Control During Manufacturing</i>							
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Table 79b: Yield Learning

Technology Requirements - Long Term

Table 79b: Technology Requirements for Yield Learning			
<i>Long Term Years</i>			
<i>Year of Production</i>	2010	2013	2016
<i>DRAM ½ Pitch (Sc. 2.0)</i>	45	32	22
<i>MPU Printed Gate Length (Sc. 3.7)</i>	25	18	13
Wafer size (mm)	450	450	450
Wafer area (mm ²)	159107	159107	159107
Number of mask levels	31	33	35
Number of processing steps	610	650	690
Cycle time during ramp (# days)	31	33	35
<i>Defect/Fault Sourcing Complexity [A], [F]</i>			
Logic transistor density/cm ² (1E6)	210	519	1279
Defect sourcing complexity factor (1E9) [B]	128	337	883
Defect sourcing complexity trend [C]	18	48	126
<i>Data Analysis for Rapid Defect/Fault Sourcing</i>			
Patt wfr insp sensitivity (nm) during yield ramp	18	13	9
Average # of inspections/wafer during full flow	6.2	6.6	7
(#data items/wafer) (1E13) [D]	57.4	120.8	271.2
Defect data volume (DV) trend [E]	10	22	49
<i>Yield Learning During Ramp from 30% to 80% sort yield</i>			
# of yield learning cycles/year based on full flow cycle time	11.8	11.1	10.4
Required yield improvement rate per learning cycle	4.2	4.5	4.8
Time to identify & fix new defect/fault source during ramp	15.5	16.5	17.5
# of learning cycles/yr for 1 defect/fault source/month	5.8	5.1	4.4
Req yld impr rate/learning cycle for 1 defect/fault source/month	8.7	9.9	11.3
<i>Excursion Control During Manufacturing</i>			
TBD	TBD	TBD	TBD

Wafer Environment Contamination Control

Key 2001 Updates

Focus on:

- **Aligning tables to ORTC requirements**
- **Aligning critical particle size to Defect Detection (1X DR for volume production)**
- **Further Clarification of PoP, PoC, PoU**
- **Better interlock with other TWGs for introduction of new materials, device architectures**

- **Do not anticipate major deltas to plan and**
- **Do not expect much yellow/red on tables.**

Wafer Environment Contamination Control

Key 2001 Updates

- **Atmospheric/Airborne Wafer Environmental Control**
 - Believe assumptions used in past will continue to hold up (e.g. particle deposition, molecular adsorption)
 - No real drivers identified to justify significant deltas from 1999/2000
 - Will tap into SEMI mini-environment group currently collecting data on Atomic/Molecular Contamination (AMC) for standards
 - Must consider capture of reticle requirements for AMC
- **Ultra-Pure H₂O**
 - Particles: align with defect detection
 - Current mis-match between projected capability (filtration) and detection. Will show projected capability in table.
 - Create “most critical” / “less Critical” categories for ions and metallics.
 - Must coordinate better w/ ESH on water conservation/reclaim.
 - Need sanity check on surface prep.

Wafer Environment Contamination Control

Key 2001 Updates

- **Chemicals**
 - Focus on correcting inconsistencies: Chemical vs Water.
- **Gases**
 - Basically no changes except for realigning w/ ORTC Scenarios
 - Likely to remove corrosives for metal etch and add new category for ILD precursors.

Table 80: Wafer Environment Contam. Control Technology Requirements – Near Term

Table 80a Defect Prevention and Elimination Technology Requirements—Near Term

Year of Introduction "Technology Node"	2001 130nm	2002 115	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm
<i>Wafer Environment Control</i>							
Critical particle size (nm) [A]	65	58	52	45	38	35	33
Particles ³ critical size (/m ³) [B]	5	4	3	2	2	1	1
<i>Airborne Molecular Contaminants (pptM) [C]</i>							
Lithography—Bases (as amine, amide, or NH ₃)	750	750	750	750	750	<750	<750
Gate—Metals (as Cu, E=2 × 10 ⁻⁵) [C]	0.2	0.2	0.15	0.1	0.1	0.07	<0.07
Gate—Organics (as molecular weight greater than or equal to 250, E=1 × 10 ⁻³) [D]	100	90	80	70	60	60	50
—Organics(as CH ₂)	1800	1620	1440	1260	1100	900	<900
Salicidation contact—acids (as Cl ⁻ , E=1 × 10 ⁻⁵)	10	10	10	10	10	<10	<10
Salicidation contact—bases (as NH ₃ , E=1 × 10 ⁻⁶)	20	16	12	10	8	4	<4
Dopants (P or B) [F]	< 10	< 10	< 10	< 10	< 10	< 10	< 10
<i>Process Critical Materials</i>							
Critical particle size (nm) [A]	65	58	52	45	38	35	33
<i>Ultrapure Water</i>							
Total oxidizable carbon (ppb)	1	1	< 1	< 1	< 1	< 1	< 1
Bacteria (CFU/ liter)	< 1	< 1	< 1	< 1	< 1	< 1	< 1
Total Silica (ppb)	0.05	0.05	0.05	0.05	0.01	0.01	0.01
Dissolved oxygen (ppb)	1	1	1	1	1	1	1
Particles ³ critical size (/ml)	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2
Critical cation, anion, metals (ppt, each)	< 20	< 20	< 20	10	10	10	10

Table 80: Wafer Environment Contam. Control Technology Requirements – Near Term (cont.)

Year of Introduction "Technology Node"	2001 130nm	2002 115 nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm
<i>Liquid Chemicals [E]</i>							
Particles ³ critical size (/ml)							
HF-, H2O2, NH4OH: Fe, Cu (ppt, each)	< 150	<135	< 110	< 100	< 90	<50	<50
Critical cation, anion, metals (ppt, each)	< 10	< 10	< 10	< 5	< 5	< 5	<1
HF-only TOC (ppb)	< 30	< 30	< 25	< 20	< 15	<10	<10
HCl, H2SO4: All impurities (ppt)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
BEOL Solvents, Strippers K, Li, Na (ppt, each)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
<i>Bulk Ambient Gases</i>							
N2,O2,Ar,H2: H2O,O2,CO2,CH4 (ppt, each)	< 1000	< 1000	< 1000	< 1000	< 1000	<100	< 100
Particles > critical size (liter)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
<i>Specialty Gases</i>							
POU Particles ³ critical size (/liter) [D]	2	2	2	2	2	2	2
<i>Corrosives—metal etchants</i>							
O2 (ppbv)	< 500	< 500	< 500	< 200	< 200	< 200	< 100
H2O (ppbv)	< 500	< 500	< 500	< 200	< 200	< 200	< 100
<i>Inerts—Oxide/PR Etchants/Strippers</i>							
O2 (ppbv)	< 1000	< 1000	< 1000	< 500	< 500	<500	< 100
H2O (ppbv)	< 1000	< 1000	< 1000	< 500	< 500	<500	< 100
Total metallics (pptwt)	< 500	< 500	< 500	< 500	< 500	<100	< 100

Table 80: Wafer Environment Contam. Control Technology Requirements – Long Term

Year of Introduction "Technology Node"	2010 45nm	2013 32nm	2016 22nm
<i>Wafer Environment Control</i>			
Critical particle size (nm) [A]	23	16	11
Particles ³ critical size (/m ³) [B]	1	<1	<1
<i>Airborne Molecular Contaminants (pptM) [C]</i>			
Lithography—Bases (as amine, amide, or NH ₃)	<750	<750	<750
Gate—Metals (as Cu, E=2 × 10 ⁻⁵) [C]	<0.07	<0.07	<0.07
Gate—Organics (as molecular weight greater than or equal to 250, E=1 × 10 ⁻³) [D]	40	30	20
—Organics(as CH ₂)	<900	<900	<900
Salicidation contact—acids (as Cl ⁻ , E=1 × 10 ⁻⁵)	<10	<10	<10
Salicidation contact—bases (as NH ₃ , E=1 × 10 ⁻⁶)	<4	<4	<4
Dopants (P or B) [F]	<10	<10	<10
<i>Process Critical Materials</i>			
Critical particle size (nm) [A]	23	16	11
<i>Ultrapure Water</i>			
Total oxidizable carbon (ppb)	<1	<1	<1
Bacteria (CFU/ liter)	<1	<1	<1
Total Silica (ppb)	0.01	<0.01	<0.01
Dissolved oxygen (ppb)	1	<1	<1
Particles ³ critical size (/ml)	<0.2	<0.2	<0.2
Critical cation, anion, metals (ppt, each)	10	<10	<10

Table 80: Wafer Environment Contam. Control Technology Requirements – Long Term (cont.)

Year of Introduction "Technology Node"	2010 45nm	2013 32nm	2016 22nm
<i>Liquid Chemicals [E]</i>			
Particles ³ critical size (/ml)			
HF-, H ₂ O ₂ , NH ₄ OH: Fe, Cu (ppt, each)	<50	<40	<40
Critical cation, anion, metals (ppt, each)	<1	<1	<1
HF-only TOC (ppb)	<8	<6	<4
HCl, H ₂ SO ₄ : All impurities (ppt)	< 1000	< 1000	< 1000
BEOL Solvents, Strippers K, Li, Na (ppt, each)	< 1000	< 1000	< 1000
<i>Bulk Ambient Gases</i>			
N ₂ , O ₂ , Ar, H ₂ : H ₂ O, O ₂ , CO ₂ , CH ₄ (ppt, each)	<100	<100	<100
Particles > critical size (liter)	< 0.1	< 0.1	< 0.1
<i>Specialty Gases</i>			
POU Particles ³ critical size (/liter) [D]	2	2	2
<i>Corrosives—metal etchants</i>			
O ₂ (ppbv)	<100	<50	<50
H ₂ O (ppbv)	<100	<50	<50
<i>Inerts—Oxide/PR Etchants/Strippers</i>			
O ₂ (ppbv)	<100	<50	<50
H ₂ O (ppbv)	<100	<50	<50
Total metallics (pptwt)	<100	<50	<50

Defect Detection and Characterization

Key Issues for 2002

- **High Aspect Ratio Inspection (HARI)**
 - detection of defects occurring deep within structures having depth to width ratios greater than 3
 - treated separately from patterned wafer inspection due to special sensitivity requirements
 - not achievable in manufacturing environment due to low throughput and high cost of ownership
- **Automatic Defect Classification and Review (SEM)**
 - Available technology can theoretically achieve required speed (defects/sec) but practically falls short of required goal
 - Dwell time required for EDX limits required throughput for automatic elemental classification

Yield Learning

Key Issues for 2002

- **Yield Learning**
 - Tools are needed to detect, review, classify, analyze and source continuously shrinking visible defects
 - Techniques needed to rapidly isolate failures and partition them into those caused by visible defects, non-visual defects, and parametric issues
 - Automatic Defect Classification (ADC) and Spatial Signature Analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information
 - Defect Sourcing
 - The electrical fault must be isolated (localized) within the chip.
 - The complexity of this task is proportional to the number of transistors per unit area (cm^2) times the number of process steps, forming the defect sourcing complexity factor as shown in Table 79
 - In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity

Yield Learning

Key Issues for 2002

- Yield Learning
 - Data Management
 - A fundamental impediment to efficient IDM is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories
 - Retrieval of data from a variety of database sources will be required to efficiently reduce data sources to process-related information in a timely manner.
 - Methods needed for integrating workflow information (such as WIP data) with the DMS, especially in commercial DMS systems
 - Methods needed for recording time-based data (from *in situ* process sensors, tool health, and tool log data) such that it can be correlated with lot and wafer-based data are needed
 - Yield prediction tools and methods continue to be limited to a small number of experts. Ability needs to be transferred to a broader engineering group. Will result in the rapid prioritization of defect generating mechanisms and faster engineering response to prioritized issues

Difficult Challenges

65nm node and above

- **Yield Model and Defect Budget**
 - Random and systematic yield models have to be developed and validated
 - Process induced defects, equipment generated particles, product/process measurements, and design/layout sensitivities have to be correlated to yield
- **Defect Detection and Characterization**
 - High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/vias/trenches, and especially defects near/at the bottom of these features
 - Need recommendation for types of wafers (preparation) and process to be used for maximum sensitivity at each process step
 - Current detection recipes relatively insensitive to wafer-edge defectivity (exclusion area = 2 to 10 mm)

Difficult Challenges

65nm node and above

- **Yield Learning**
 - Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions
 - Wafer-edge management required for yield/defectivity optimization
 - Specific recommendations for test structures and short loops including warning limits for generic process flows
 - Specific sampling model, including evaluation of inventory risk at each sampling level.
- **Wafer Environment Contamination Control**
 - Need adaptive water reclaim procedures keyed to particular process needs (define contaminants of interest and those not of interest)

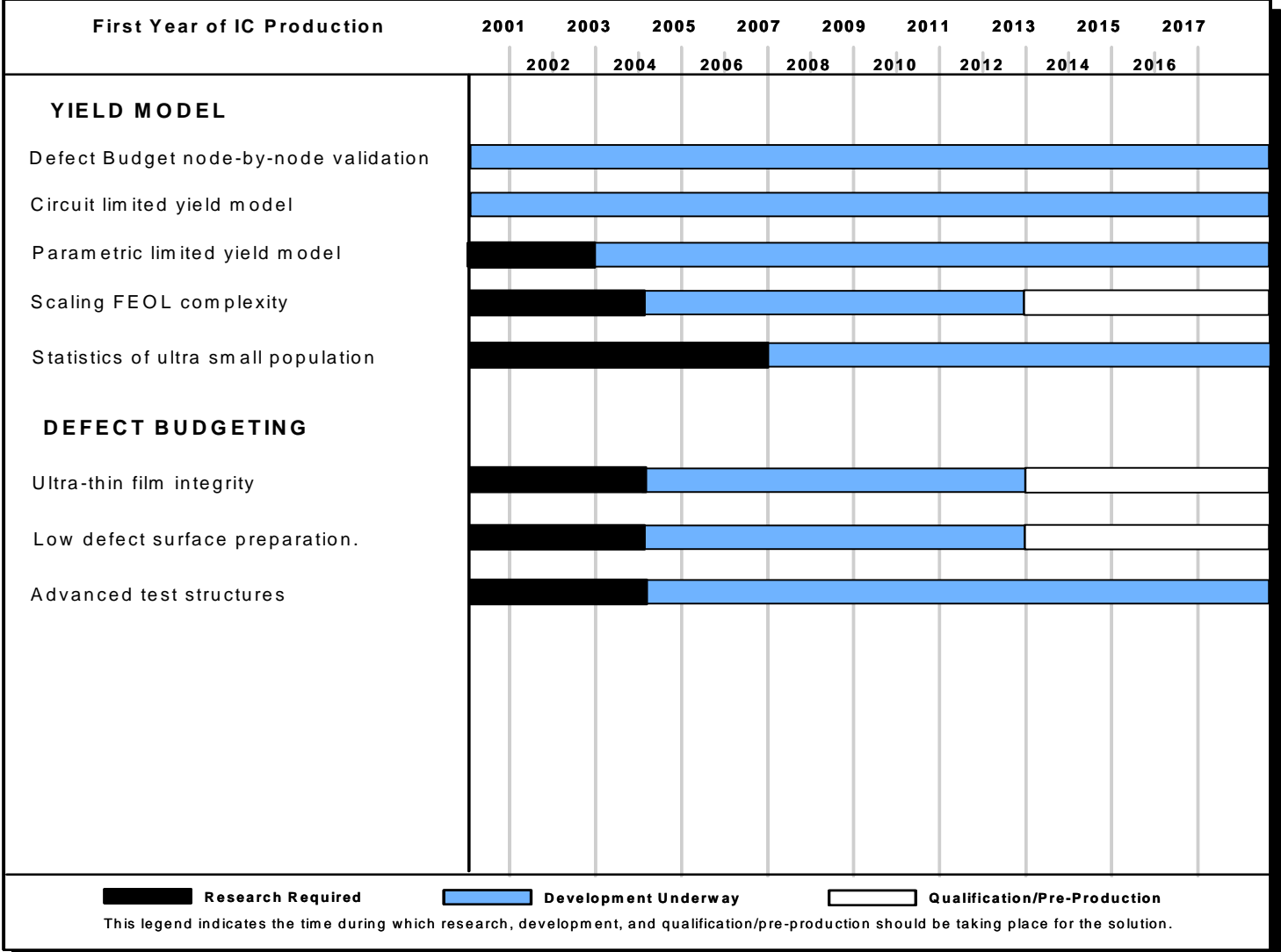
Difficult Challenges

Less than 65nm

- **Yield Model and Defect Budget**
 - Yield models must comprehend greater parametric sensitivities, impact of circuit design, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.
- **Defect Detection and Characterization**
 - Lack of enabling technology to detect or review defects
- **Yield Learning**
 - Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected
 - IC designs must be optimized for a given process capability and must be testable/diagnosable.

Yield Model and Defect Budget

Proposed Solutions



Yield Learning

Proposed Solutions

Figure 57 Yield Learning Potential Solutions

