

International Technology
Roadmap for
Semiconductors
2000 Update

Modeling and Simulation

TABLE OF CONTENTS

Modeling and Simulation	1
Summary	1
2000 Update Tables	2
Table 87a Modeling and Simulation Technology Requirements: Capabilities—Near Term**	2
Table 87a Modeling and Simulation Technology Requirements: Capabilities—Near Term**	3
Table 87b Modeling and Simulation Technology Requirements: Accuracy/Speed—Near Term**	4
Table 87c Modeling and Simulation Technology Requirements: Capabilities—Long Term**	7

MODELING AND SIMULATION

SUMMARY

- Next two generations (130nm, 100nm) provide many modeling challenges:
- High frequency circuit models (RLC, transistor)
- Model cross-die variation due to litho, etch, thin film (e.g., OPC, CMP, equipment modeling)
- Model lithography technology tradeoffs (resolution enhancement techniques, wavelength, PSM)
- Goals for cost reduction due to TCAD
- Beyond 100nm, basic theoretical research needed:
- Gate stack process and electrical model (atomic level)
- Limits of MOS devices, innovative MOS devices and beyond
- University research funding necessary

TECHNOLOGY REQUIREMENTS

Evaluations of the Technology Requirements for Modeling and Simulation during 2000 resulted in a change to the tables in the status of the solutions for each requirement from *Solutions being Pursued* [yellow] to *Solutions Existing* [white].

COST REDUCTION

- Goal of TCAD Technology Requirements: overall development cost reduction
- High volume 300mm wafer production in 2001: increased cost and fewer wafers for development
- Successful TCAD role in development of derivative processes
- More effort needed in predictive modeling, backend models

PROCESS TCAD (ACCURACY)

- Thermal processes: lower temperature, shorter time
- Increased impact of interfaces, defects
- Experimental evaluation of dopant profiles still an issue
- Calibration is necessary for effective use

DEVICE SIMULATION (ACCURACY)

- <20nm gate oxides increases importance of gate current modeling
- Off current modeling and cut-off frequency modeling remain important issues

LONG TERM DEVICE MODELING

MODELING LIMITS OF MOS DEVICES

- Noise margins
- Atomic-level fluctuations
- Reduction of yield due to statistical variation

MODELING FOR INNOVATIVE MOS AND BEYOND

- dual-gate MOS
- SOI
- vertical MOS
- quantum effect devices? Others?

POTENTIAL SOLUTIONS: NEW ITWG RECOMMENDATIONS (2000)

EQUIPMENT MODELING:

Equipment suppliers should *supply physical models* and modeling information with equipment

DEVICE MODELING:

Focus efforts on *limits to MOS*, and *alternatives beyond MOS*

Increase modeling efforts in *opto-electronics*

CIRCUIT MODELING:

Communication of *process effects to designers* (within-die variation, more detailed interconnect parasitics)

Increased effort on *industry standard circuit models*

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(1999 ITRS)</i>	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)</i>	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

2000 UPDATE TABLES

Table 87a Modeling and Simulation Technology Requirements: Capabilities—Near Term**
WAS

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
<i>Equipment/Topography</i>							
Equipment simulation	—	Gate stack and interconnect uniformity models			Effect of processing conditions on material properties		
Equipment/feature scale link	—	Plasma etch: feature/equipment model			Within-chip feature variation		
<i>Lithography</i>							
Lithography: evaluate wavelength	—	Evaluate 248 nm versus 193 nm			Evaluate 193 nm versus 157 nm		
Resist models	—	193, 157 nm resist models			Detailed chemical resist development model		
<i>Front End Process Modeling</i>							
Gate Stack: evaluate materials	—	Model alternate dielectrics			Model metal versus poly gate		
Diffusion and activation coefficients	—	Kinetics of diffusion and activation			Interface interactions with point defects and dopants		
Stress/extended defects	—	Front end stress model			Extended defects and dislocations		
<i>Device Modeling (Numerical)</i>							
Gate stack models	—	Gate current tunneling models			Full quantum gate stack models		
Reliability models	—	Transistor reliability models (gate oxide)			Interconnect reliability models (electromigration, stress)		
Noise/variation	—	Dopant fluctuation			Noise models		
<i>Circuit Element Modeling/ECAD</i>							
New circuit element models	—	SOI circuit model			Gate tunneling current		
Interconnect models	—	Full-chip RLC			On-chip Inductance effects		
System-on-a-chip	—	Unified analog/digital			DRAM/Flash/embedded memory models		
<i>Package Modeling</i>							
Package models	—	Complex interconnect geometries; multiple power and ground planes			Thermo-mechanical models		
Unified package/chip models	—	Unified package/chip circuit models			Unified RLC extraction for package/chip		
<i>Numerics</i>							
Numerical algorithms	—	Robust, reliable 3D grid generation			Highly efficient optimization algorithms		

This table is meant to outline new capability requirements needed for future technology nodes; the column for the 180 nm node (1999) is blank only because the development of this technology is basically complete. Furthermore, if the development of capabilities specified for later nodes could be accelerated, they would in most cases be helpful for earlier technology nodes.

Solutions Exist

Solutions Being Pursued

No Known Solutions

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 87a Modeling and Simulation Technology Requirements: Capabilities—Near Term**
IS

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
<i>Equipment/Topography</i>							
Equipment simulation	—	Gate stack and interconnect uniformity models		Effect of processing conditions on material properties			
Equipment/feature scale link	—	Plasma etch: feature/equipment model		Within-chip feature variation			
<i>Lithography</i>							
Lithography: evaluate wavelength	—	Evaluate 248 nm versus 193 nm		Evaluate 193 nm versus 157 nm			
Resist models	—	193, 157 nm resist models		Detailed chemical resist development model			
<i>Front End Process Modeling</i>							
Gate Stack: evaluate materials	—	Model alternate dielectrics		Model metal versus poly gate			
Diffusion and activation coefficients	—	Kinetics of diffusion and activation with interface interactions with point defects and dopants					
Stress/extended defects	—	Front end stress model		Extended defects and dislocations			
<i>Device Modeling (Numerical)</i>							
Gate stack models	—	Gate current tunneling models		Full quantum gate stack models			
Reliability models	—	Transistor reliability models (gate oxide)		Interconnect reliability models (electromigration, stress)			
Noise/variation	—	Dopant fluctuation		Noise models			
<i>Circuit Element Modeling/ECAD</i>							
New circuit element models	—	SOI circuit model		Gate tunneling current			
Interconnect models	—	Full-chip RLC		On-chip Inductance effects			
System-on-a-chip	—	Unified analog/digital		DRAM/Flash/embedded memory models			
<i>Package Modeling</i>							
Package models	—	Complex interconnect geometries; multiple power and ground planes		Thermo-mechanical models			
Unified package/chip models	—	Unified package/chip circuit models		Unified RLC extraction for package/chip			
<i>Numerics</i>							
Numerical algorithms	—	Robust, reliable 3D grid generation		Highly efficient optimization algorithms			

This table is meant to outline new capability requirements needed for future technology nodes; the column for the 180 nm node (1999) is blank only because the development of this technology is basically complete. Furthermore, if the development of capabilities specified for later nodes could be accelerated, they would in most cases be helpful for earlier technology nodes.

Solutions Exist

Solutions Being Pursued

No Known Solutions

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 87b Modeling and Simulation Technology Requirements: Accuracy/Speed—Near Term**
WAS

YEAR TECHNOLOGY NODE	1999 180 nm	2002 130 nm	2005 100 nm	Driver
OVERALL TECHNOLOGY COST REDUCTION TARGET (DUE TO TCAD)	20%	25%	35%	
<i>Equipment/Topography Modeling</i>				
Etch/dep. cross wafer uniformity (% accuracy of the control spec)	20%	10%	10%	M
2D/3D topography accuracy	36 nm (20%)	20 nm (15%)	10 nm (10%)	M
<i>Lithography Modeling</i>				
Resist profile prediction accuracy	27 nm (15%)	13 nm (10%)	10 nm (10%)	
OPC model accuracy	9 nm (5%)	6.5 nm (5%)	5 nm (5%)	
<i>Front End Process Modeling</i>				
Vertical and lateral junction depth simulation accuracy	18 nm (10%)	13 nm (10%)	10 nm (10%)	
Total source/drain series resistance (accuracy)	20%	20%	20%	
Long-channel V_t (accuracy)	5% (75–90mV)	4% (48–60mV)	3% (27–36mV)	
<i>Device Modeling (Numerical)</i>				
Accuracy of f_t at given f_t (% of maximum chip frequency)	10%	10%	10%	
Gate leakage current accuracy (%) (decreases due to increase of I_g/I_d)	100%	70%	40%	
I_{off} accuracy	100%	70%	40%	
V_t rolloff accuracy (mV)	25mV	20mV	20mV	
<i>Circuit Element Modeling/ECAD</i>				
I-V error—compact model accuracy	5%	5%	5%	
Sub-threshold current—compact	95%	50%	10%	
Intrinsic MOS C-V—compact model accuracy	<7%	<6%	<5%	
Parasitic C-V—compact model accuracy	5–10%	5–10%	5–10%	
G_m and r_0 at $V_t+150mV$ versus L , V_{bs} , and T	5%	4%	3%	
Circuit delay accuracy (% of maximum chip frequency)	10%	5%	5%	
RLC delay accuracy (% of maximum chip frequency)	10%	5%	5%	
<i>Package Modeling</i>				
Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	
Stress model accuracy (% of yield stress)	10%	10%	10%	
Temperature distribution for chip and package (accuracy)	5°C	5°C	5°C	
<i>Numerical Methods</i>				
Speed-up of algorithms for 3D process/device	1x	2x	4x	
Linear solvers (kilo equations/minute)	150K	300K	600K	
Parallel speed-up	1x	2x	4x	
MFLOPS required	80	1000	4000	

Solutions Exist



Solutions Being Pursued



No Known Solutions



** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numerals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 87b Modeling and Simulation Technology Requirements: Accuracy/Speed—Near Term
*IS***

YEAR TECHNOLOGY NODE	1999 180 nm	2002 130 nm	2005 100 nm	Driver
OVERALL TECHNOLOGY COST REDUCTION TARGET (DUE TO TCAD)	20%	25%	35%	
<i>Equipment/Topography Modeling</i>				
Etch/dep. cross wafer uniformity (% accuracy of the control spec)	20%	10%	10%	M
2D/3D topography accuracy	36 nm (20%)	20 nm (15%)	10 nm (10%)	M
<i>Lithography Modeling</i>				
Resist profile prediction accuracy	27 nm (15%)	13 nm (10%)	10 nm (10%)	
OPC model accuracy	9 nm (5%)	6.5 nm (5%)	5 nm (5%)	
<i>Front End Process Modeling</i>				
Vertical and lateral junction depth simulation accuracy	18 nm (10%)	13 nm (10%)	10 nm (10%)	
Total source/drain series resistance (accuracy)	20%	20%	20%	
Long-channel V_t (accuracy)	5% (75–90mV)	4% (48–60mV)	3% (27–36mV)	
<i>Device Modeling (Numerical)</i>				
Accuracy of f_t at given f_t (% of maximum chip frequency)	10%	10%	10%	
Gate leakage current accuracy (%) (decreases due to increase of I_g/I_d)	100%	70%	40%	
I_{off} accuracy	100%	70%	40%	
V_t rolloff accuracy (mV)	25mV	20mV	20mV	
<i>Circuit Element Modeling/ECAD</i>				
I-V error—compact model accuracy	5%	5%	5%	
Sub-threshold current—compact	95%	50%	10%	
Intrinsic MOS C-V—compact model accuracy	<7%	<6%	<5%	
Parasitic C-V—compact model accuracy	5–10%	5–10%	5–10%	
G_m and r_0 at $V_t+150mV$ versus L , V_{bs} , and T	5%	4%	3%	
Circuit delay accuracy (% of maximum chip frequency)	10%	5%	5%	
RLC delay accuracy (% of maximum chip frequency)	10%	5%	5%	
<i>Package Modeling</i>				
Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	
Stress model accuracy (% of yield stress)	10%	10%	10%	
Temperature distribution for chip and package (accuracy)	5°C	5°C	5°C	
<i>Numerical Methods</i>				
Speed-up of algorithms for 3D process/device	1x	2x	4x	
Linear solvers (kilo equations/minute)	150K	300K	600K	
Parallel speed-up	1x	2x	4x	
MFLOPS required	80	1000	4000	

Solutions Exist



Solutions Being Pursued



No Known Solutions



** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numerals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(1999 ITRS)</i>	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)</i>	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 87c Modeling and Simulation Technology Requirements: Capabilities—Long Term
WAS**

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Equipment/Topography</i>			
Equipment simulation	Ab initio simulation of materials properties	Computer engineered materials and process recipes	
<i>Lithography</i>			
Next generation lithography	EUV and E-beam system	Beyond roadmap lithography models	
Resist technology	EUV resists	Finite polymer-size effects	Non-conventional photo-resist models
<i>Front End Process Modeling</i>			
Advanced process models	Metastable activation (>solid solubility)	Alternative materials (such as SiGe)	Atomistic process model
Advanced doping models	Solid source	New technology needed	
<i>Numerical Device Modeling</i>			
Alternative device models	2D quantum models for MOS	Single electron transistor	Quantum effect devices
<i>Circuit Element Modeling/ECAD</i>			
Advanced circuit models	Quantum effects/non-quasi-static	Circuit models for alternative devices	New technology needed
<i>Package Modeling</i>			
Electrical/optical models	Full-wave analysis	Mixed electrical/optical analysis	New technology needed
<i>Numerics</i>			
Numerical algorithms	Exploit parallel computation	Efficient atomistic/quantum methods	Multi-scale simulation (atomistic-continuum)

Solutions Exist

Solutions Being Pursued

No Known Solutions

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(1999 ITRS)</i>	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE <i>(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)</i>	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 87c Modeling and Simulation Technology Requirements: Capabilities—Long Term**
IS

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Equipment/Topography</i>			
Equipment simulation	Ab initio simulation of materials properties	Computer engineered materials and process recipes	
<i>Lithography</i>			
Next generation lithography	EUV and E-beam system	Beyond roadmap lithography models	
Resist technology	EUV resists	Finite polymer-size effects	Non-conventional photo-resist models
<i>Front End Process Modeling</i>			
Advanced process models	Metastable activation (>solid solubility)	Alternative materials (such as SiGe)	Atomistic process model
Advanced doping models	Solid source	New technology needed	
<i>Numerical Device Modeling</i>			
Alternative device models	2D quantum models for MOS	Single electron transistor	Quantum effect devices
<i>Circuit Element Modeling/ECAD</i>			
Advanced circuit models	Quantum effects/non-quasi-static	Circuit models for alternative devices	New technology needed
<i>Package Modeling</i>			
Electrical/optical models	Full-wave analysis	Mixed electrical/optical analysis	New technology needed
<i>Numerics</i>			
Numerical algorithms	Exploit parallel computation	Efficient atomistic/quantum methods	Multi-scale simulation (atomistic-continuum)

Solutions Exist

Solutions Being Pursued

No Known Solutions

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.