International Technology Roadmap for Semiconductors

2000 Update

Interconnect

TABLE OF CONTENTS

Interconnect....1
Summary....1
2000 Update Tables....2
Table 46a MPU Interconnect Technology Requirements—Near Term Years**....2
Table 46b MPU Interconnect Technology Requirements—Long Term Years**....4
Table 47a DRAM Interconnect Technology Requirements—Near Term....5
Table 47b DRAM Interconnect Technology Requirements—Long Term....5
Table 48a SoC Interconnect Technology Requirements—Near Term....6
Table 48b SoC Interconnect Technology Requirements—Long Term....6

INTERCONNECT

SUMMARY

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes. Although copper containing chips were introduced in 1998, copper must be combined with new insulators to meet the overall roadmap performance specifications. The introduction of new low dielectric constant materials, CVD metal/barrier seed layers, and additional process elements for SoC provide significant process and process integration challenges. The 2000 Update to the ITRS has refined the reliability specifications and reintroduced the concept of FITS/unit length to underscore the reliability challenge facing the very long integrated wiring length. Planarization metrics were substantially updated; the dishing metric was eliminated from local and intermediate levels and replaced by a single thinning metric. Similarly, a combined dishing and erosion metric was created for global levels. Finally, the global dishing specifications have been revised in isolated features. The technology requirements for specific dielectric constants have been clarified by including both a bulk dielectric constant target along with the effective dielectric constant target so that interpolations may be made for the many possible integration options. Changes were also made to the technical requirements for barrier thickness by relaxing the targets without an impact on performance. The 2001 ITRS is expected to continue to refine the tables to assist the industry in managing this rapid rate of materials introduction and the concomitant fabrication complexity.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

2000 UPDATE TABLES

*Table 46a MPU Interconnect Technology Requirements—Near Term Years***

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
MPU ½ pitch	230	210	180	160	145	130	115
MPU gate length (nm)	140	120	100	**90**	80	70	65
Number of metal levels	6-7	6–7	7	7–8	8	8	8–9
Number of optional levels—ground planes/capacitors	0	0	0	2	2	2	2
Total interconnect length (m) – active wiring only (footnote for calculation)	**10836**	**12632**	**14654**	**18624**	**21546**	**25249**	**31659**
FITS/m X 10E-3 (fitting footnote)	**0.46**	**0.40**	**0.34**	**0.27**	**0.23**	**0.20**	**0.16**
Jmax (A/cm^2)—wire (at 105°C)	5.8E5	7.1E5	8.0E5	9.6E5	1.1E6	1.3E6	1.4E6
Imax (mA)—via (at 105°C)	0.36	0.36	0.33	0.32	0.29	0.27	0.24
Local wiring pitch (nm)	500	450	405	365	330	295	265
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Cu local dishing (nm), 5% × height	18	16	15	14	13	12	11
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**36**	**32**	**30**	**28**	**26**	**24**	**22**
Intermediate wiring pitch (nm)	640	575	520	465	420	375	340
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/2.2
Cu intermediate dishing (nm), 15 micron wide wire, 10% × height	64	60	57	51	46	43	41
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	**64**	**60**	**57**	**51**	**46**	**43**	**41**

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production Technology Node (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Year of Production Technology Node **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

*Table 46a MPU Interconnect Technology Requirements—Near Term Years (continued)***

Year Technology Node	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
MPU ½ pitch	230	210	180	160	145	130	115
MPU gate length (nm)	140	120	100	**90**	80	70	65
Minimum global wiring pitch (nm)	1050	945	850	765	690	620	560
Global wiring A/R (Al)	2	2.1	2.2	2.3	2.4	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/2.8
Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 micron wide wire	**116**	**109**	**102**	**95**	**90**	**84**	**76**
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height	116	109	102	95	90	84	76
Cu thinning global wiring due to dishing (nm), 100 micron wide feature	**80**	**72**	**65**	**59**	**53**	**48**	**43**
Conductor effective resistivity (μΩ-cm) Al wiring	3.3	3.3	3.3	3.3	3.3	**	**
Conductor effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu wiring) (nm)***	17	16	14	13	12	11	10
Interlevel metal insulator — effective dielectric constant (κ)	3.5–4.0	3.5–4.0	2.7–3.5	2.7–3.5	2.2–2.7	2.2–2.7	1.6–2.2
Interlevel metal insulator — effective dielectric constant (κ)	**3.5–4.0**	**3.5–4.0**	**2.9–3.5**	**2.9–3.5**	**2.2–2.9**	**2.2–2.9**	**1.6–2.2**
Interlevel metal insulator (minimum expected) — bulk dielectric constant (κ)	**2.9**	**2.9**	**2.7**	**2.7**	**2.0**	**2.0**	**1.3**

* *Assumes a conformal barrier/nucleation layer*
** *This technology is not expected to extend to this node*
*** *Calculated for a conformal layer in local wiring to meet minimum effective conductor resistivity*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE **(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)**	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

*Table 46b MPU Interconnect Technology Requirements—Long Term Years***

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
MPU ½ pitch	80	55	40
MPU gate length (nm)	45	**33**	22
Number of metal levels	9	9–10	10
Number of optional levels – ground planes/capacitors	3	4	4
Total interconnect length (m) – active wiring only (footnote for calculation)	51730	91532	148835
FITS/m X 10E-3 (fitting footnote)	0.10	0.05	0.03
Jmax (A/cm^2)—wire (at 105°C)	2.1E6	3.7E6	4.6E6
Imax (mA)—via (at 105°C)	0.18	0.16	0.11
Local wiring pitch (nm)	185	130	95
Local A/R (for Cu)	1.9	2.1	2.3
Cu local dishing (nm), 5% × height	9	7	5
Intermediate wiring pitch (nm)	240	165	115
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Cu intermediate wiring dishing (nm), 15 micron wide wire, 10% × height	30	22	17
Minimum global wiring pitch (nm)	390	275	190
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height	55	38	29
Conductor effective resistivity (μΩ-cm) Cu wiring	2.2	<1.8	<1.8
Barrier/cladding thickness (nm)	0	0	0
Barrier/cladding thickness (nm)	7	5	4
Interlevel metal insulator— effective dielectric constant (κ)	1.5	<1.5	<1.5
Interlevel metal insulator— effective dielectric constant (κ)	1.6	<1.6	<1.3
Interlevel metal insulator (minimum expected) — bulk dielectric constant (κ)	1.3	<1.3	1.1

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 Update										
Year of Production *Technology Node* **(1999 ITRS)**	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Year of Production *Technology Node* **(Proposed node years are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)**	*1999* *180 nm*	*2000*	*2001* **130 nm**	*2002*	*2003*	*2004* **90nm**	*2005*	2008 **[60 nm]**	2011 **[40 nm]**	2014 **[30 nm]**

Table 47a DRAM Interconnect Technology Requirements—Near Term

Year *Technology Node*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
DRAM ½ pitch	**180**	**165**	**150**	**130**	**120**	**110**	**100**
Number of metal levels	**3**	**3**	**3**	**3–4**	**4**	**4**	**4**
Contact A/R—stacked capacitor	**9.3**	**10.0**	**10.7**	**11.4**	**11.9**	**12.4**	**13.0**
Local wiring pitch (nm) noncontacted	**360**	**330**	**300**	**260**	**240**	**210**	**200**
Specific contact resistance (Ω-cm^2)	**3.0E-7**	**2.5E-7**	**2.0E-7**	**1.7E-7**	**1.6E-7**	**1.1E-7**	**1.0E-7**
Specific via resistance (Ω-cm^2)	**7E-9**	**5E-9**	**3E-9**	**2E-9**	**2E-9**	**1E-9**	**1E-9**
Conductor effective resistivity (μΩ-cm)*	**3.3**	**3.3**	**3.3**	**3.3**	**3.3**	**3.3**	**2.2**
Interlevel metal insulator—effective dielectric constant (κ)	**4.1**	**4.1**	**4.1**	**3.0–4.1**	**3.0–4.1**	**3.0–4.1**	**2.5–3.0**

* *Assumes a conformal barrier/nucleation layer*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 47b DRAM Interconnect Technology Requirements—Long Term

Year *Technology Node*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM ½ pitch	**70**	**50**	**35**
Number of metal levels	**4**	**4**	**4**
Contact A/R—stacked capacitor	**14.1**	**16.1**	**23.1**
Local wiring pitch (nm) non-contacted	**140**	**100**	**70**
Specific contact resistance (Ω-cm^2)	**5.0E-8**	**2.5E-8**	**1.5E-8**
Specific via resistance (Ω-cm^2)	**6E-10**	**3E-10**	**1.5E-10**
Conductor effective resistivity (μΩ-cm)*	**2.2**	**2.2**	**2.2**
Interlevel metal insulator— effective dielectric constant (κ)	**2.5–3.0**	**2.0–2.5**	**2.0–2.3**

* *Assumes a conformal barrier/nucleation layer*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

Table 48a SoC Interconnect Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
MPU ½ pitch (nm)	230	210	180	160	145	130	115
ASIC gate (nm)	180	165	150	130	120	110	100
Number of metal levels	6	6	7	7	7–8	8	8
Number of optional levels—passive elements	1	1	2	2	4	4	4
Local wiring pitch (nm)	450	405	360	325	290	260	230
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Intermediate wiring pitch (nm)	560	505	450	405	360	325	285
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Intermediate via A/R (Al)	2.8	2.8	2.9	2.9	3.0	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/2.2
Global wiring pitch (nm)	900	810	720	650	580	520	460
Global wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/2.8
Interlevel metal insulator—effective dielectric constant (κ)	3.5–4.0	3.5–4.0	2.7–3.5	2.7–3.5	2.2–2.7	2.2–2.7	1.6–2.2

** *This technology is not expected to extend to this node.*

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Table 48b SoC Interconnect Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
MPU ½ pitch (nm)	80	55	40
ASIC gate (nm)	70	50	35
Number of metal levels	9	9–10	10
Number of optional levels—passive elements	6	6	6
Local wiring pitch (nm)	165	120	85
Local wiring A/R (for Cu)	1.9	2.1	2.2
Intermediate wiring pitch (nm)	210	145	110
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Global wiring pitch (nm)	330	240	170
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Interlevel metal insulator— effective dielectric constant (κ)	1.5	< 1.5	< 1.5

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.