

2000 Test Roadmap Update

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International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

2000 TTWG Members

US Members		International Members	
Name	Company	Name	Company
• Mark Baber	Lucent	Peter Muhmenthaler	Infineon
• Bill Ortner	Lucent	Rene Segers	Philips
• Yi Cai	Lucent	Kazumi Hatayama	Hitachi
• Richard Antley	TI	Mr Ohta	Matsushita
• Marc Mydill	TI	Mr. Satou	Hitachi
• Anne Gattiker	IBM	Kang Chil Lee	Hyundai
• Don Weater	IBM		
• Phil Nigh	IBM		
• Uli Schoettmer	Agilent		
• Peter Maxwell	Agilent		
• Tim Sheen	Teradyne		
• Robert Nesbitt	Schlumberger		
• Paul Roddy	Motorola		
• Donland Edenfeld	Intel		
• Roger Barth	Intel		
• Michael Rogers	Intel		
• Rochit Rajsuman	Advantest		
• Yervant Zorian	Logic Vision		



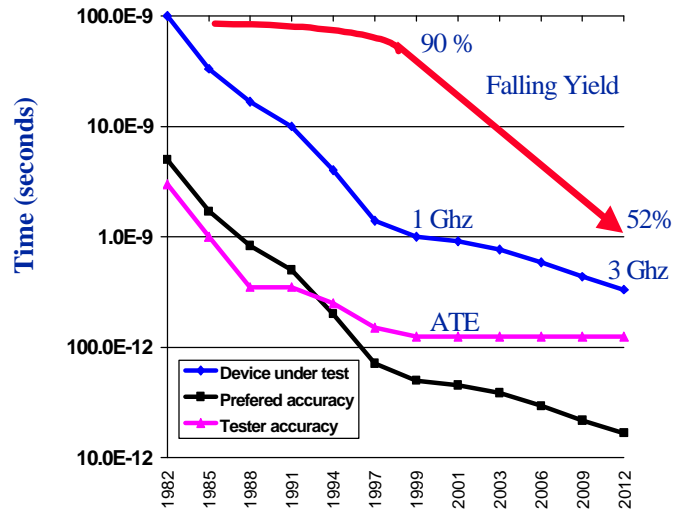
The 2000 Test Evolution WHY!

- In the Next Decade Traditional Functional Test will be phased out by Semiconductor Manufacturers as a standard test methodology and DFT/BIST will dominate the landscape
 - **The three main reasons are**
 - *Cost*
 - *Performance*
 - *Development time*
- Test will fork into three directions (no global solution to replace functional test)
 - **Test During Burn-In (TDBI) & Wafer Level Test(WLT)**
 - **Low Cost Testers (LCT)**
 - **System Level Test (SysTest)**

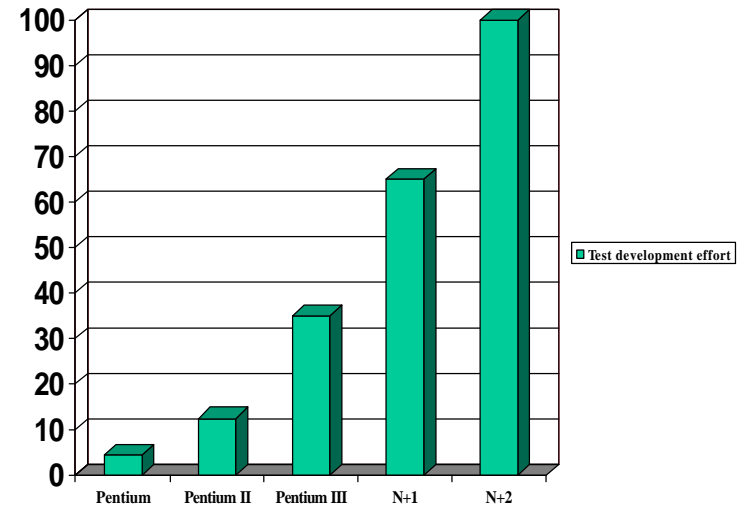


The 2000 TEST EVOLUTION

Tester Accuracy impact of Yield

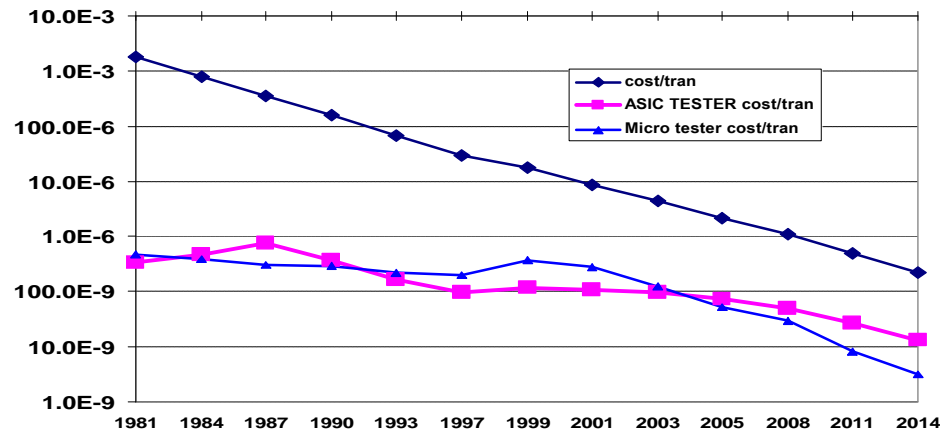


Test Program Development Effort

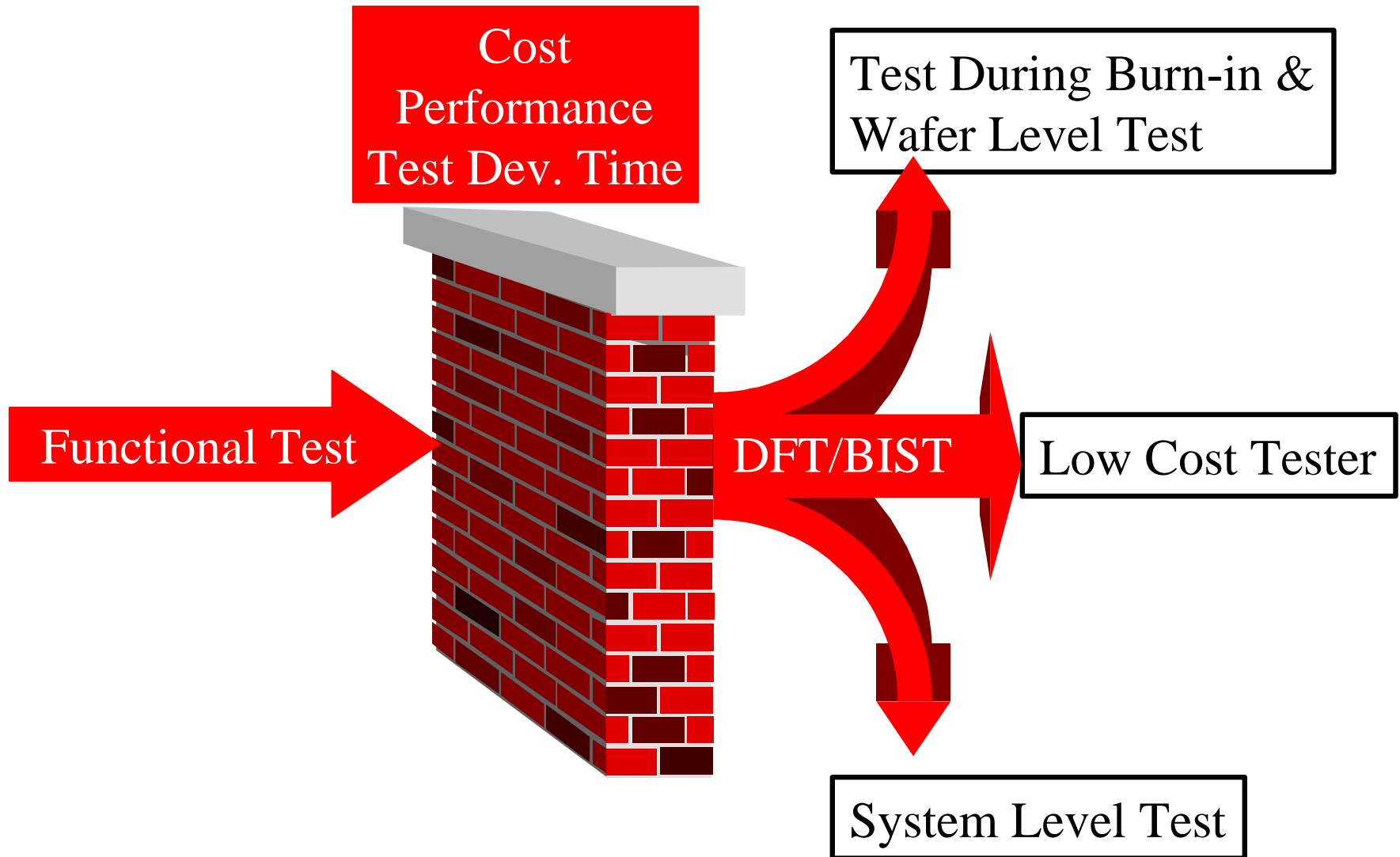


-Source: ITRS Design TWG

Tester Cost per Transistor 1999 ITRS



The 2000 TEST EVOLUTION



-Source: ITRS Design TWG



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Why Functional Test Will Phase Out

- Cost - The cost of test has been growing as a percent of overall device cost every generation
 - **Lower ASP families report test cost 20 to 50%**
- Performance - The ability to get Tester signals in and out of the device are reaching physical limits
 - **Tester accuracy inadequate for requirements**
 - **Interface between DUT and Tester creates an environment that does not match the device environment in a system**
- Test Development Time
 - **Transistor count grew from 1M to 40M while operating frequency went from 50 MHz to 800 MHz during the 90's**
 - **Development and debug of functional vectors has grown from several man months to 10's of man years during the 90's**



Test Strategies After Functional Test

- Test During Burn-In and Wafer Level Test
 - **TDBI requires DFT/BIST strategy to allow the burn-in oven to exercise all the device transistors from a limited number of pins**
 - Can become a subset of the Structural test DFT/BIST requirements
 - Structural test could be performed during Burn-in
 - **Full Wafer Level Test(FWLT) will also require a test methodology that will allow limited pin contact across the die to limit the total probe card pin count**
 - Gram force per pin which drives the maximum chuck force capability
 - DFT/BIST strategy will be required to drive FWLT



Test Strategies After Functional Test(cont.)

- Low Cost Tester (LCT)
 - **As high performance devices use DFT/BIST test methods to perform accurate AC tests that meet yield and DPM goals, then the semiconductor manufacturers will use LCT**
 - Scan & BIST methodologies have been proven that can accomplish the above goals
 - Impacts that DFT/BIST implementations has on Die size and performance are acceptable with today's and future technology nodes
- System Level Test (SLT)
 - **Many manufacturers of complex devices today have implemented SLT because of quality and performance levels associated with functional test**
 - Takes far to long to develop a functional test too find quality related test escapes
 - Most MPU's are now multi die shipped in some form of daughter card technology



Test TWG 2000/1 Focus/Direction

- **Little Update in 2000 except DFT/BIST**
- **2001 Revamp Tables**
 - ✓ Yld Vs Accuracy
 - ✓ High Performance ASIC
 - ✓ High Performance Logic
 - ✓ Low End Logic
 - ✓ Mixed Signal
 - ✓ Commodity DRAM
 - ✓ Commodity Flash
 - ✓ Embedded DRAM
 - ✓ Embedded Flash
 - ✓ DFT/BIST

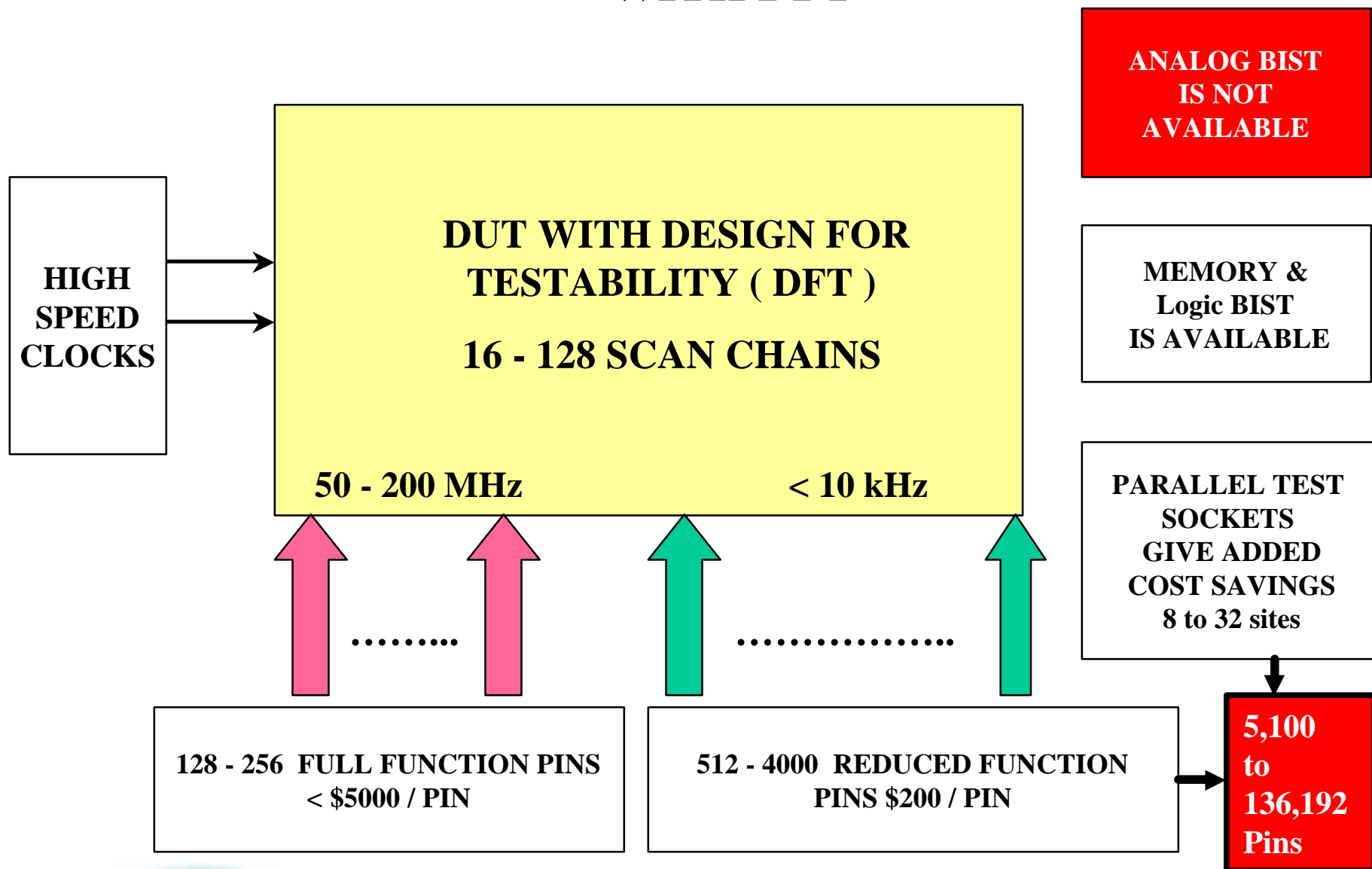


Possible new groupings:

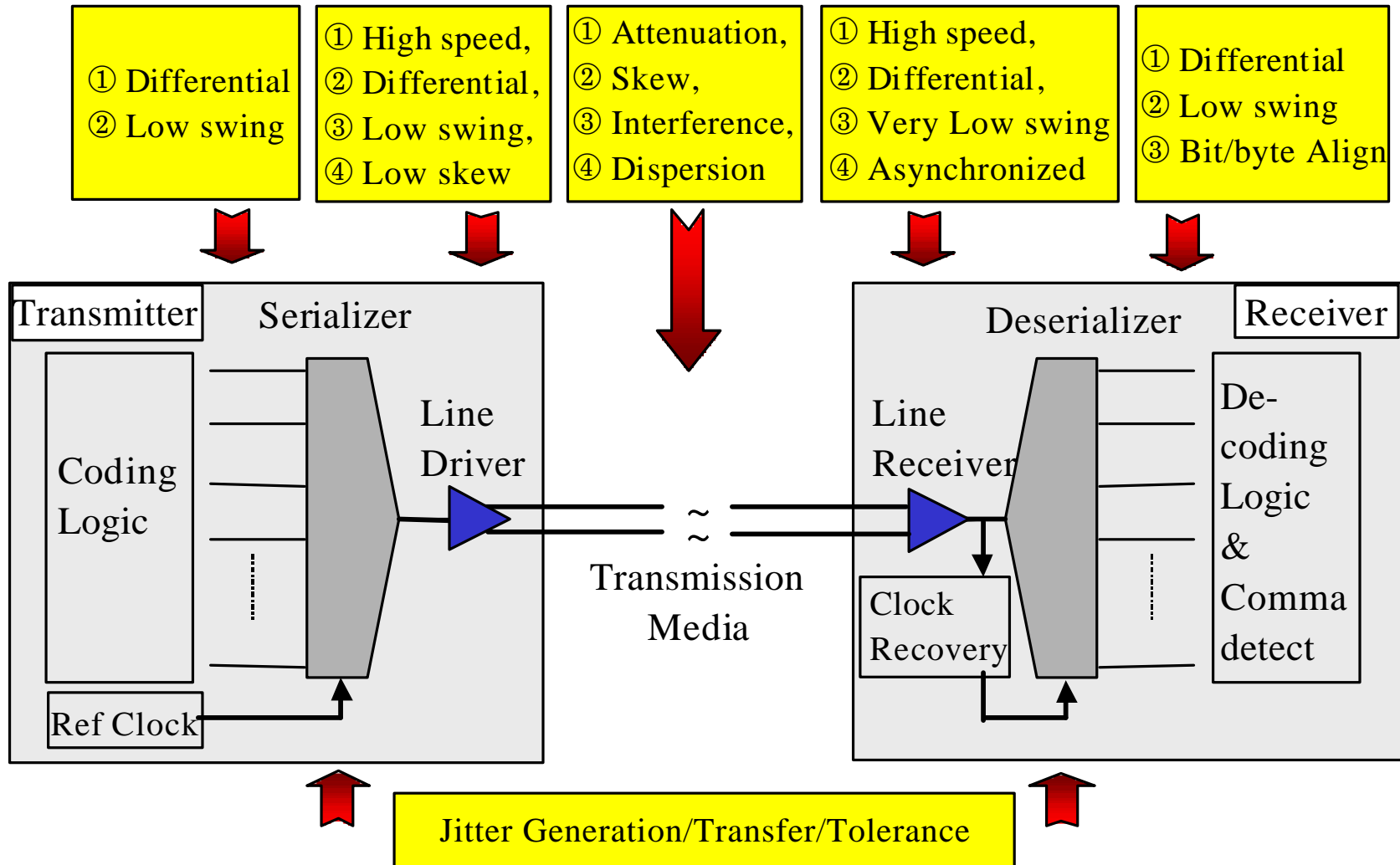
DFT/BIST
Memory Test
Characterization Test
Manufacturing Test
SOC Test?????



LOW COST TESTING OF DEVICES DESIGNED WITH DFT



Challenges for Testing Serial Communication Devices



High Frequency Serial Communications Test Challenges

- SONET, SERDES, Firewire, Gigabit Ethernet and Fibre channel etc.
 - These high speed buffers operate from 1.25 to 10 Gb/s and are replacing conventional 100 -200 Mb/s parallel buses
 - Some high frequency serial ports 16 in and 16 out are being implemented now
 - Noise measurements are very important and time consuming in manufacturing.
 - Separate rack-and-stack instrument approaches are not acceptable in manufacture.



MAJOR TESTING CONCERNS

- **TEST COSTS, TEST ACCURACY, TEST DEVELOPMENT TIME ARE SERIOUS ISSUES.**
- **ANALOG BIST IS NOT AVAILABLE**
- **HIGH-SPEED INTERFACES (PROBES, SOCKETS, TRANSMISSION LINES) ARE A MAJOR PROBLEM.**
- **FAILURE MODE ANALYSIS (FMA) IS A VERY IMPORTANT ISSUE. BIST TOOLS SHOULD PROVIDE THIS CAPABILITY.**

