

2000 Metrology Roadmap

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AGENDA

- **Microscopy Requirements**
 - 1999 ITRS
 - Impact of ITRS
 - Depth of Focus Issue
 - New Data and Ultimate Limit
 - New Structures Impact
- **Changes and Issues for 2000 Update**



1999 ITRS Microscopy Requirements

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2003 100 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch</i>	180	165	150	130	120	110	100	D ^{1/2}
<i>Logic Isolated Lines</i>	140	120	100	85	80	70	65	M Gate
Microscopy and Lithography								
Microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	MPU
Wafer Gate CD Control*	13	12	10	8.5	8	7	6.3	MPU
Wafer CD Tool Precision* P/T=.2 Isolated Lines**	2.6	2.4	2.0	1.8	1.6	1.4	1.3	MPU
Mask Area Metrology Tool Precision P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2	MPU

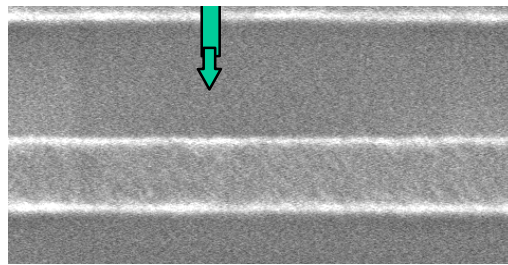


1999 ITRS Lithography

Metrology

Improve CD-SEM thru 100 nm node

NEED: Determine CD from Fundamental Model



CD-SEM

2D / 3D Information

Becoming available as model based CD and as in-line CD-SEM with tilt image

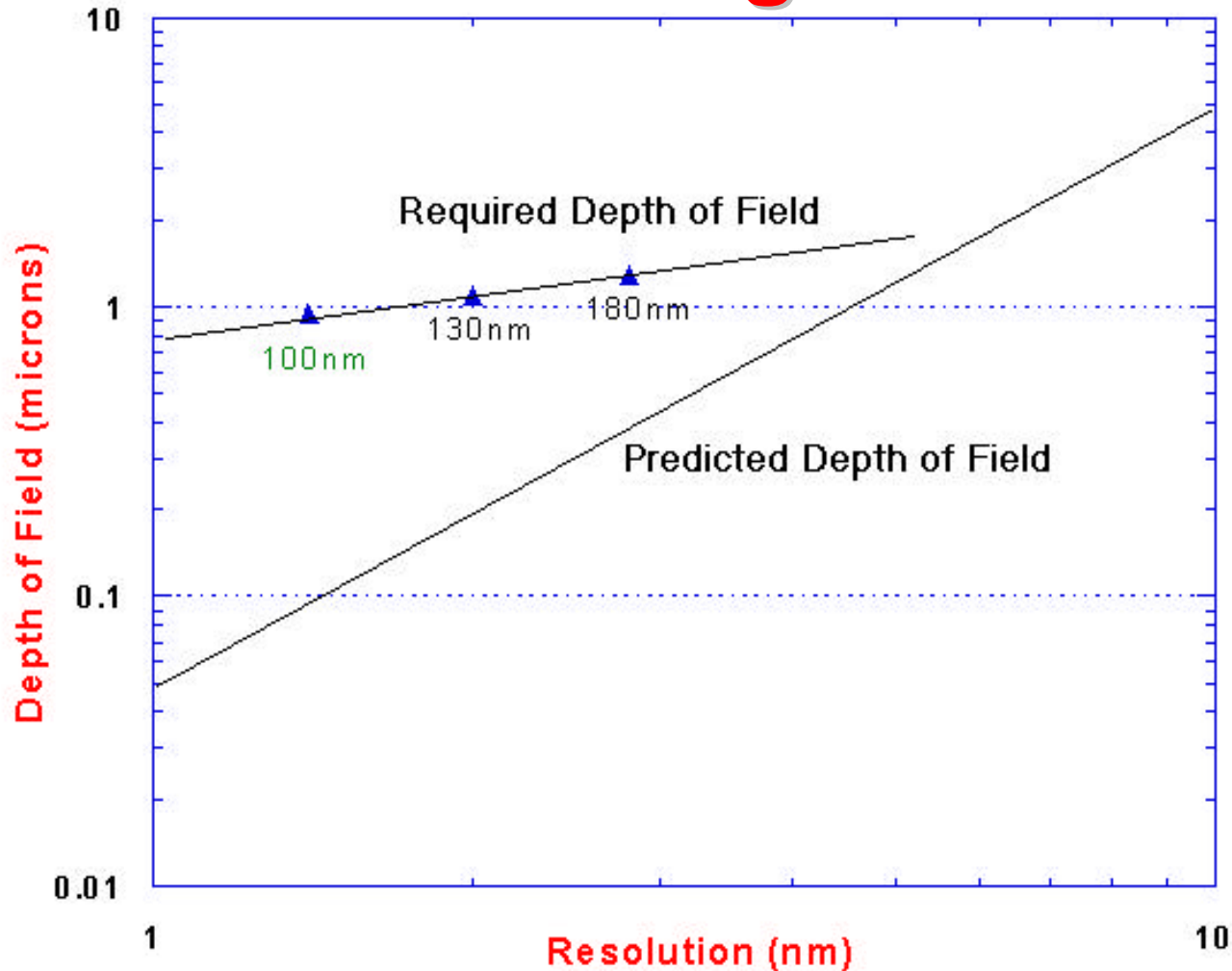
Not all sidewalls are planar



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New Data showing DoF Issues



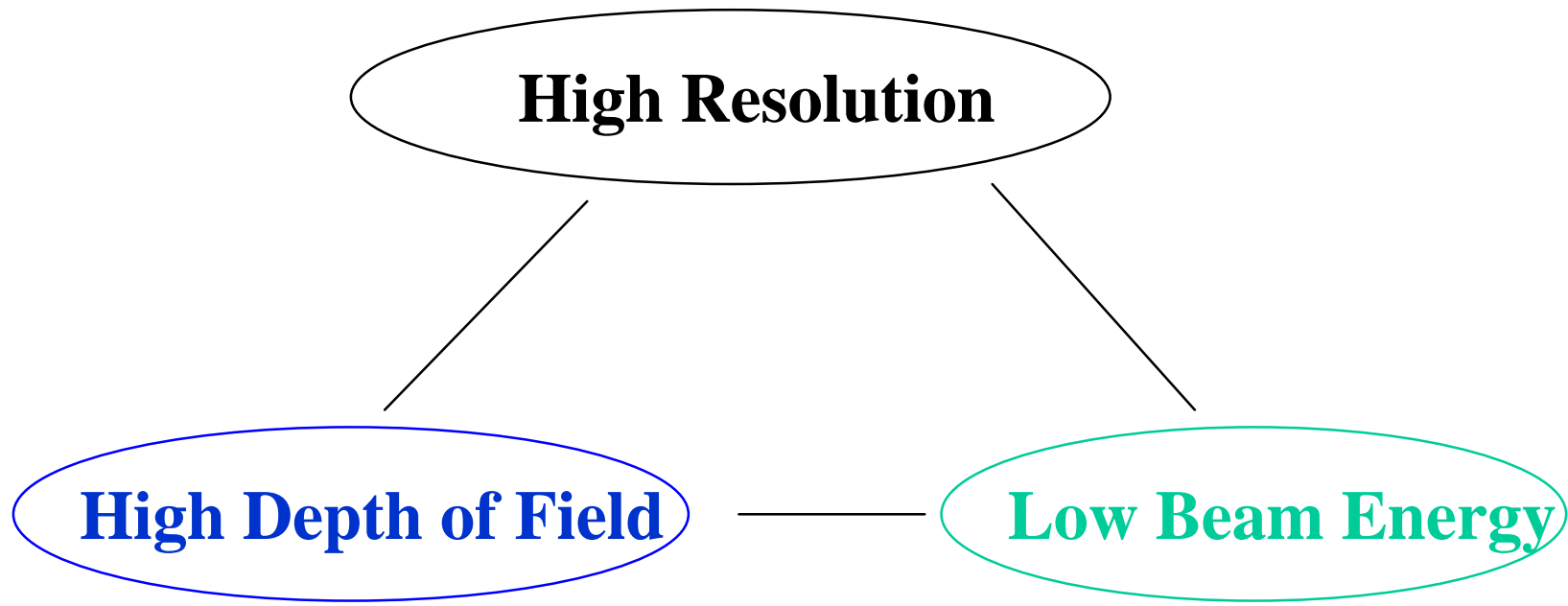
Data from Sato and Mizuno, EIPBN
2000, Palm Springs, CA



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PICK ANY TWO



**High Voltage ~200 keV is limited to
1 nm resolution for SE imaging**

Many Thanks to David Joy



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SEM Depth of Focus Issue

**DoF needs to be a Tool Specification
Listed in Roadmap**

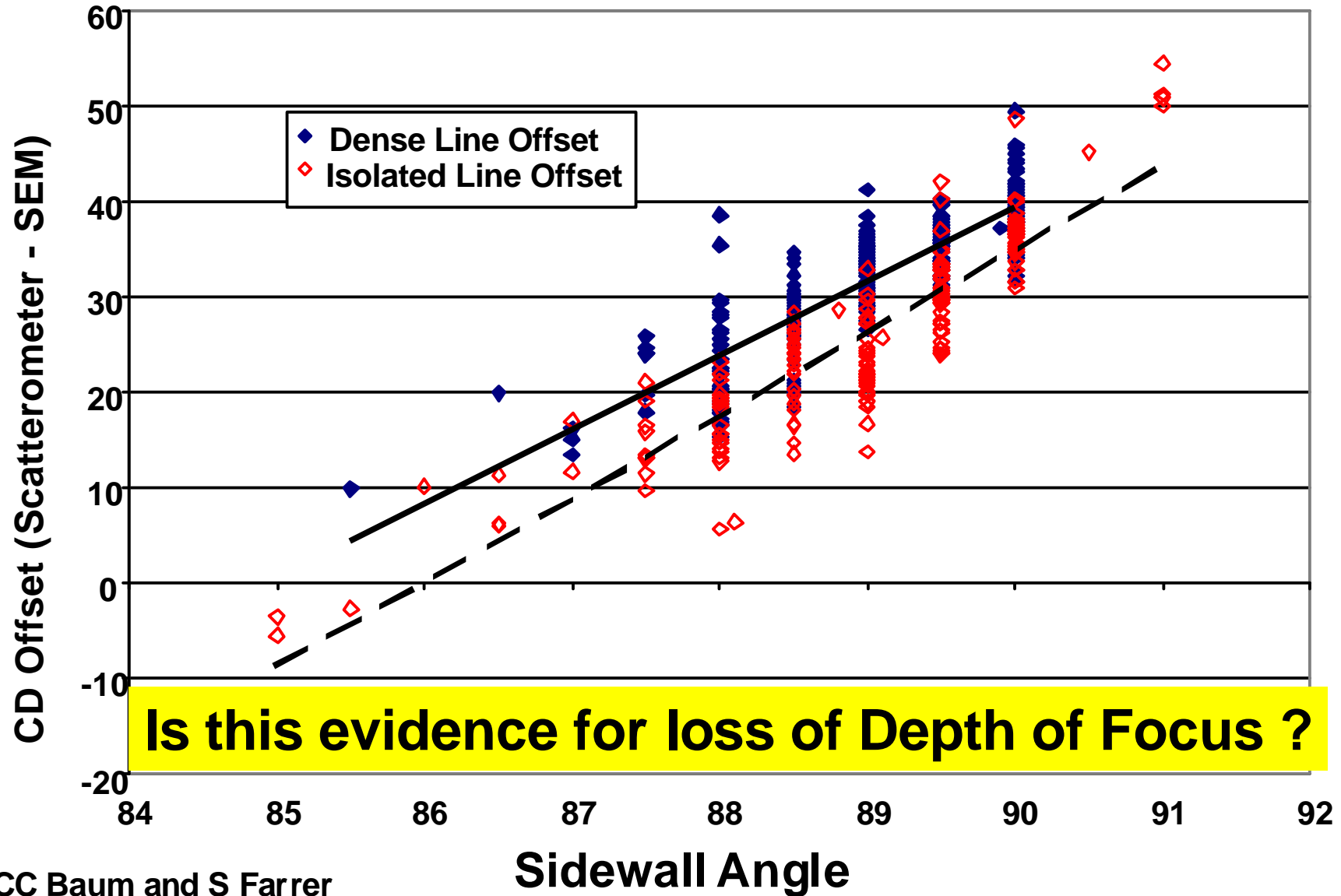


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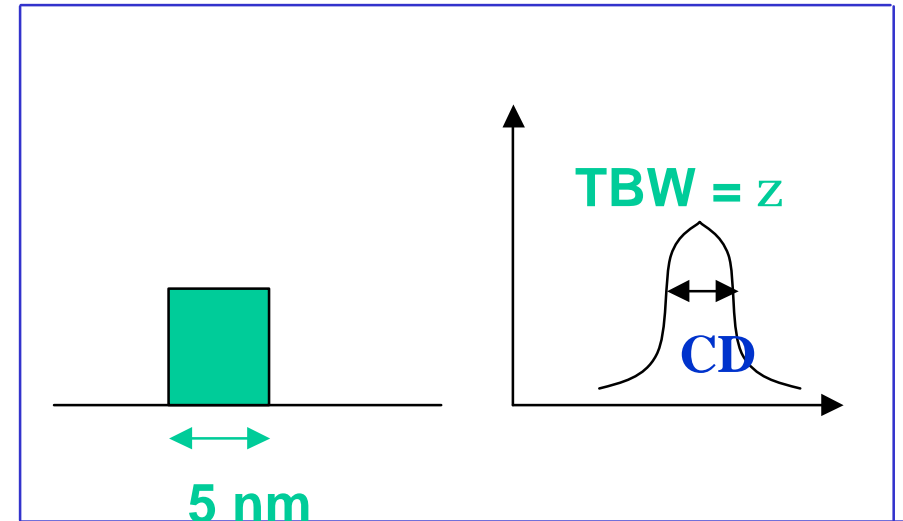
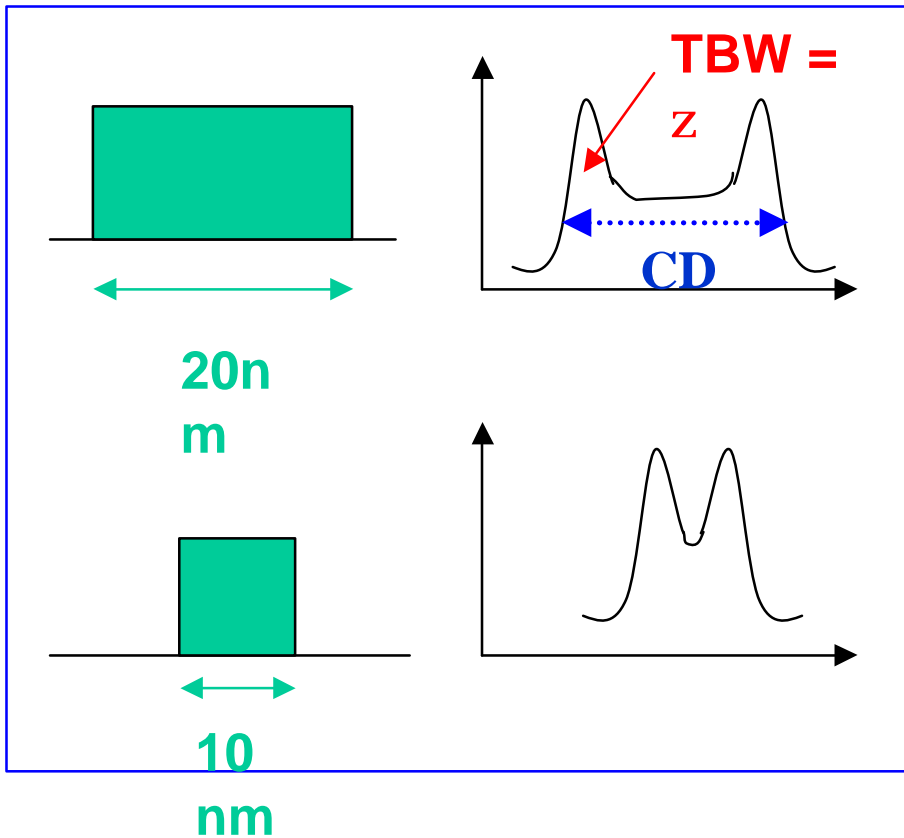
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New Data showing DoF Issues

Offset from CD-SEM by Angle



Fundamental Limit of a perfect CD-SEM



Gabor's limit

The limit of CD -SEM is based on Secondary Electron resolution is

z

the range of secondary electrons in the material

Many Thanks to David Joy



Table of Electron Ranges

Material	Z_{se}	Material	Z_{se}
Carbon	5.5nm	Silicon	3nm
Chromium	2.5nm	Copper	2.5nm
Silver	3.5nm	Gold	1.0nm
GaAs	5nm	SiO ₂	5nm
Si ₃ N ₄	4.5nm	PMMA	5nm

Porous low k ??? At 50 % porosity multiply Z_{se} by ~ 2
 $Z_{se} \sim 10 \text{ nm} ???$

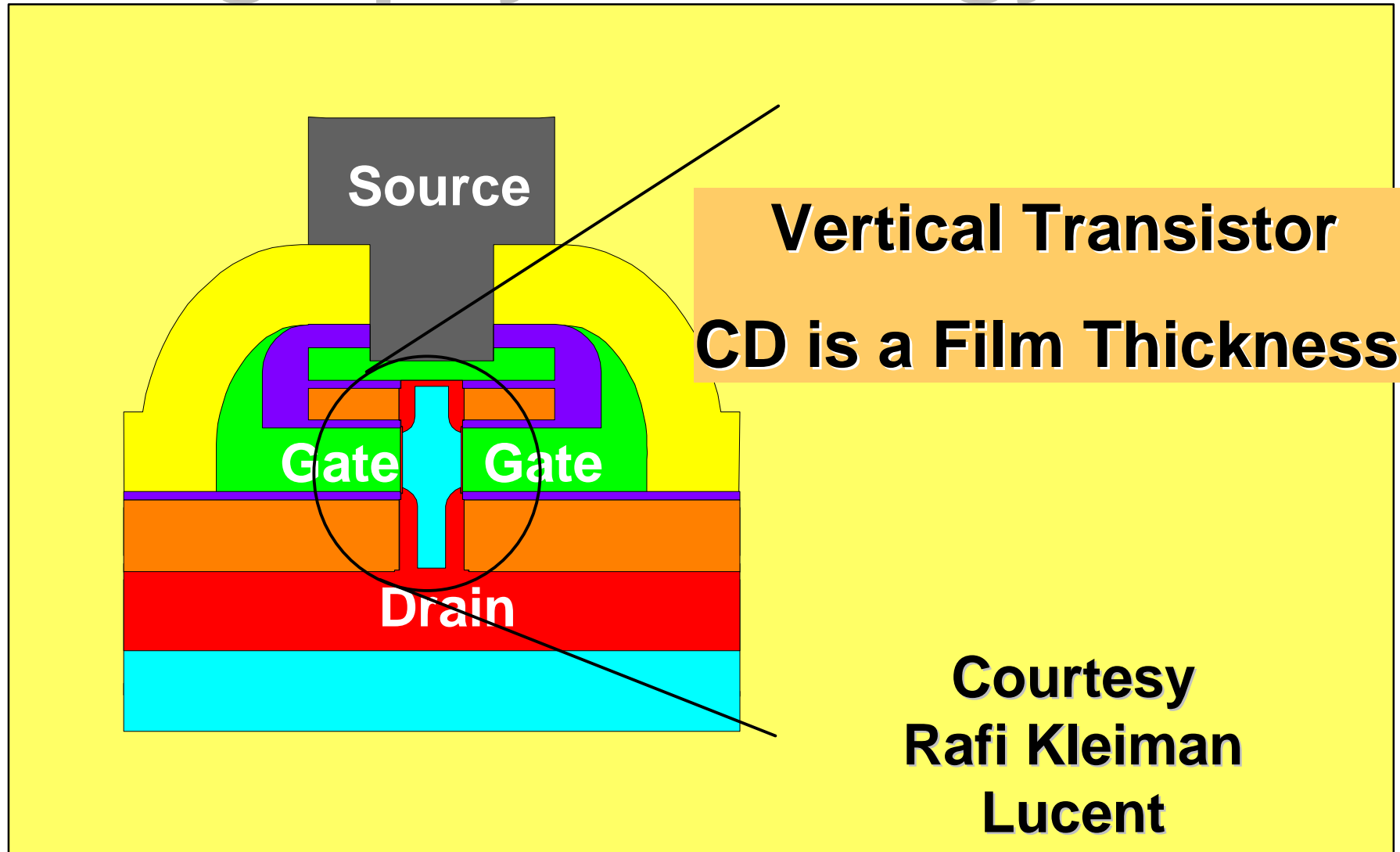
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Lithography Metrology



Metrology Update Items

- Depth of Focus Metric - Litho CD Measurements
- Address Overlay Box-in-Box Target Issues for Phase Shift and Optical Proximity Correction Masks
- New Devices change metrology
- **Add trench sidewall shape and depth (3D) measurement metric (STI, capacitor, trench gate for power device, SOI)**
- Adding New Integrated Metrology Requirements for particle detection, end point, and wafer surface temperature
- Improved Pattern Recognition Needed



Metrology Update Items

- **Add dopant Conc. Gradient specification to Spatial Resolution Metric for 2D Dopant Profiling**
- **Add to CMP flatness measurement discussion**
- **Integrated Metrology changes 4Q99: rewrite section Include Factory Integration Issues Discussion**
- **Enhance Materials Characterization Potential**

Solutions

- potential solutions for small volume analysis
- thin film characterization
- potential solution for 1 nm stress analysis (no known solutions)
- **Footnote explaining near term red**
- **Is reference materials section sufficiently clear about**

Metrology Update Items

- **Overlay structures in kerf (scribe lane) do not represent the intrafield registration adequately.**



Requirements Tables Update



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TABLE 02a Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
<i>DRAM ½ Pitch</i>	180	165	150	130	120	110	100	<i>D½</i>
<i>Was : MPU Gate Length</i>	140	120	100	85	80	70	65	<i>MPU gate</i>
<i>Is : MPU Gate Length</i>	140	120	100	90	80	70	65	<i>MPU ASIC</i>
<i>New : Final Physical Bottom Gate Length after etch (nm)</i>	126	108	90	81	72	63	59	<i>MPU ASIC</i>
Microscopy								
<i>Was : Inline, nondestructive microscopy resolution (nm) for P/T=0.1</i>	1.4	1.2	1.0	0.85	0.8	0.7	0.65	<i>MPU Gate</i>
<i>Is : Inline, nondestructive microscopy resolution (nm) for P/T=0.1 P/T >> 0.1 for 1999 and 2000</i>	1.3	1.1	0.9	0.8	0.7	0.6	0.6	<i>MPU Gate</i>
<i>Was: Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]</i>	6.3 200	6.7 175	7.1 160	7.5 140	8.0 130	8.5 120	9 110	<i>D½</i>
<i>Is: Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]</i>	6.3 200	6.7 175	7.1 160	7.5 140	8.0 130	8.5 120	9 110	<i>D½</i>
Materials and Contamination Characterization								
<i>Was: Real particle detection limit (nm) [B]</i>	90	82	75	65	60	55	50	<i>D1/2</i>
<i>Is: Real particle detection limit (nm) [B]</i>	90	82	75	65	60	55	50	<i>D 1/2</i>
<i>Was: Minimum particle size for compositional analysis (on dense lines) (nm)</i>	48	40	33	28	27	23	22	<i>MPU Gate</i>
<i>Is: Minimum particle size for compositional analysis (on dense lines) (nm)</i>	60	55	50	43	40	37	33	<i>D 1/2</i>
<i>Specification limit of total surface contamination Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni (atoms/cm²)</i>	£9·10 ⁹	£7·10 ⁹	£6·10 ⁹	£4.4·10 ⁹	£3.4·10 ⁹	£2.9·10 ⁹	£2.5·10 ⁹	<i>MPU Gate</i>
<i>Was: Surface detection limits for individual elements Ca, Co, Cu, Cr, Fe, K, Mo, Nm, Na, Ni (atoms/cm²) with signal to noise of 3:1 for each element</i>	£9·10 ⁸	£7·10 ⁸	£6·10 ⁸	£4.4·10 ⁸	£3.4·10 ⁸	£2.9·10 ⁸	£2.5·10 ⁸	<i>MPU Gate</i>
<i>Is: Surface detection limits for individual elements Ca, Co, Cu, Cr, Fe, K, Mo, Nm, Na, Ni (atoms/cm²) with signal to noise of 3:1 for each element</i>	£5.9·10 ⁸	£5.5·10 ⁸	£4.2·10 ⁸	£3.9·10 ⁸	£2.9·10 ⁸	£2.4·10 ⁸	£2.2·10 ⁸	<i>Smallest from MPU or DRAM</i>

Table 84a Front End Processes Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch	180	165	150	130	120	110	100	D½
MPU Gate Length	140	120	100	85	80	70	65	M Gate
<i>Is</i> : MPU Gate Length	140	120	100	90	80	70	65	MPU gate
<i>New</i> : Final Physical Bottom Gate Length after etch (nm)	126	120	100	90	80	70	65	MPU ASIC
<i>Was</i> : Oxygen range (ASTM "79) in heavily doped substrates; measurement precision ± 0.5 ppma [A]	18–31	18–31	18–31	18–31	18–31	18–31	18–31	
<i>Is</i> : Oxygen range (ASTM "79) in heavily doped substrates; measurement precision ± 0.5 ppma [A]	19–31	18–31	18–31	18–31	18–31	18–31	18–31	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm ³)	1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	< 1 × 10 ¹⁰	
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm ³)	1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	< 1 × 10 ⁹	
<i>Was</i> : Logic dielectric equivalent thickness (nm) ± 3σ process range	1.9–2.5 ± 4%	1.9–2.5 ± 4%	1.5–1.9 ± 4%	1.5–1.9 ± 4%	1.5–1.9 ± 4%	1.2–1.5 ± 4%	1.0–1.5 ± 4%	M Gate
<i>Is</i> : Logic dielectric equivalent thickness (nm) ± 3σ process range	1.9–2.5 ± 4%	1.9–2.5 ± 4%	1.5–1.9 ± 4%	1.5–1.9 ± 4%	1.5–1.9 ± 4%	1.2–1.5 ± 4%	1.0–1.5 ± 4%	MPU Gate
Logic dielectric measurement precision 3σ (nm) [B]	0.0075	0.0075	0.006	0.006	0.006	0.005	0.004	M Gate



Table 84a Front End Processes Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch	180	165	150	130	120	110	100	D½
MPU Gate Length	140	120	100	85	80	70	65	M Gate
<i>Is</i> : MPU Gate Length	140	120	100	90	80	70	65	MPU gate
<i>New</i> : Final Physical Bottom Gate Length after etch (nm)	126	120	100	90	80	70	65	MPU ASIC
<i>Was</i> : DRAM capacitor structure dielectric material process control requirements	Cyl. MIS Ta ₂ O ₅	Cyl. MIS Ta ₂ O ₅	Cyl. MIS Ta ₂ O ₅	Pedestal MIM Ta ₂ O ₅	Pedestal MIM Ta ₂ O ₅	Pedestal MIM Ta ₂ O ₅	Pedestal MIM BST	D½
(Dielectric constant) Equivalent oxide thickness (nm)	(22) 3.0	(22) 3.0	(22) 3.0	(50) 0.95	(50) 0.95	(50) 0.95	(250) 0.45	
<i>Is</i> : DRAM capacitor structure dielectric material process control requirements	Cyl. MIS Ta ₂ O ₅	Cyl. MIS Ta ₂ O ₅	Cyl. MIS Ta ₂ O ₅	Pedestal MIM Ta ₂ O ₅	Pedestal MIM Ta ₂ O ₅	Pedestal MIM Ta ₂ O ₅	Pedestal MIM BST	D½
(Dielectric constant) Equivalent oxide thickness (nm)	(22) 3.0	(22) 3.0	(22) 3.0	(50) 0.95	(50) 0.95	(50) 0.95	(250) 0.45	
<i>Was</i> : DRAM capacitor dielectric physical thickness (nm) ± 3 σ process range	11.5 ±4%	11.5 ±4%	11.5 ±4%	12.2 ±4%	12.2 ±4%	12.2 ±4%	28.7 ±4%	D½
<i>Is</i> : DRAM capacitor dielectric physical thickness (nm) ± 3 σ process range	11.5 ±4%	11.5 ±4%	11.5 ±4%	12.2 ±4%	12.2 ±4%	12.2 ±4%	28.7 ±4%	D½
<i>Was</i> : DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.046	0.046	0.046	0.049	0.049	0.049	0.11	D½
<i>Is</i> : DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.046	0.046	0.046	0.049	0.049	0.049	0.11	D½
2 and 3D dopant profile spatial resolution (nm)	3	3	3	2	2	2	1.5	
At-line dopant concentration precision (across concentration range) [D]	5%	5%	5%	4%	4%	4%	3%	

Solutions Exist

Solutions Being Pursued

No Known Solutions



Litho remains mostly unchanged



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Table 83a Lithography Metrology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Wafer gate CD control	13	10.8	9.0	8.1	7.2	6.3	5.9
Wafer dense line CD control	18	16.5	15	13	12	11	10
Wafer contact CD control	20	18.5	17	15	14.5	14	13
Wafer CD metrology tool precision* P/T=.2 for isolated lines**	2.6	2.2	1.8	1.6	1.4	1.3	1.2
Wafer CD metrology tool precision* P/T=.2 for dense lines**	3.6	3.3	3.0	2.6	2.4	2.2	2.0
Wafer CD metrology tool precision* P/T=.2 for contacts**	4.0	3.7	3.4	3.0	2.9	2.6	2.3
Wafer sidewall angle accuracy (in degrees) Depth of Focus ~ 1 μ m	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Maximum CD measurement bias (%)	10	10	10	10	10	10	10
Mask CD control isolated lines	16	14	12	10	9	8	7
Mask CD control dense lines	24	21	17	13	12	11	10
Mask contact area control Normalized to ρ of Area	24	21	17	14	13	12	11
Mask CD metrology tool precision* P/T=.2 for isolated lines**	3.2	2.8	2.4	2	1.8	1.6	1.4
Mask CD metrology tool precision* P/T=.2 for dense lines**	4.8	4.2	3.4	2.6	2.4	2.2	2
Mask area metrology tool precision for contact normalized to ρ of area- ρ of target for P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2
Wafer overlay control (nm)	65	58	52	45	42	38	35
Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	6.5	5.8	5.2	4.5	4.2	3.8	3.5
Final mask image placement	39	35	31	27	25	23	21
Mask image placement Metrology precision P/T=.1	3.9	3.5	3.1	2.7	2.5	2.3	2.1
Mask phase (in degrees)	2	2	2	2	2	2	2
Phase metrology precision P/T=.2 (in degrees)	.4	.4	.4	.4	.4	.4	.4
Variation in attenuated mask film transmission % of deviation from nominal (%)	4	4	4	4	4	4	4
Transmission metrology precision % of nominal attenuated psm transmission P/T=.2 (%)	.8	.8	.8	.8	.8	.8	.8

* All precision values are 3 sigma in nm and include metrology tool matching.

** Measurement tool performance needs to be independent of line shape, line materials, and density of lines.

Solutions Exist

Solutions Being Pursued

No Known Solutions



In-situ /on-line Particle Detection for Pure Water and Liquid Chemicals

First Year of Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Critical particle size (nm)	90	65	45	35	25	17
Particle detection limit (nm)	90	65	45	35	25	17

In-situ Film Thickness Measurement for Stacked Metal Layers (CMP End Point Monitor)

First Year of Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Metal layer Materials	CubARRIER metal film	Cu barrier metal film	Cu barrier metal film	single Cu	single Cu	single Cu
Thickness (nm)	350	274	225	176	137	109
Thickness control (nm, 3)	35	27	23	18	14	11
Measurement precision of film thickness (nm, 3 σ , P/T=0.1)	3.5	2.7	2.3	1.8	1.4	1.1
Response time for film thickness measurement ¹⁾ (s)	0.035	0.027	0.023	0.018	0.014	0.011
Linewidth of measured metal 1 line (nm) ²⁾	180	130	100	70	50	35

1) The response time requirements have been determined to be 1/10 of each process time required at a Cu CMP speed of 10 nm/s.

2) Film thickness measurements on metal wires are ideal, but if it is impossible the use of measurement patterns would be possible as the second choice. The measurement patterns should be located in the scribe area and have the minimum size of 60 m60 m.

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In-situ Wafer Surface Temperature Measurement for RTP and Plasma Process

First Year of Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
RTP for carrier activation Process temperature (°C) Temperature control (°C, 3σ)	600- 1100 1	600-1000 1	600-1000 1	600-900 1	600-900 1	600-900 1
Ramp speed of process temperature (°C /s)	150	200	250	>350	>350	>500
Measurement precision of wafer surface temperature (°C, 3σ)	0.3	0.3	0.3	0.3	0.3	0.3
Spatial resolution for temperature measurement (mm)	1	1	1	1	1	1
Time resolution for temperature measurement (ms) ¹	0.67	0.5	0.4	<0.29	<0.29	<0.2
Plasma process Process temperature (°C) Temperature control (°C, 3σ)	30-500 5	30-500 5	30-500 5	30-500 5	30-500 5	30-500 5
Ramp speed of process temperature (°C /s)	20	20	20	20	20	20
Measurement precision of wafer surface temperature (°C, 3σ)	1.5	1.5	1.5	1.5	1.5	1.5
Spatial resolution for temperature measurement (mm)	1	1	1	1	1	1
Time resolution for temperature measurement (ms) ¹	5	5	5	5	5	5

1) The time resolution requirements have been determined to be P/T=0.1 for each ramp time (s/°C).

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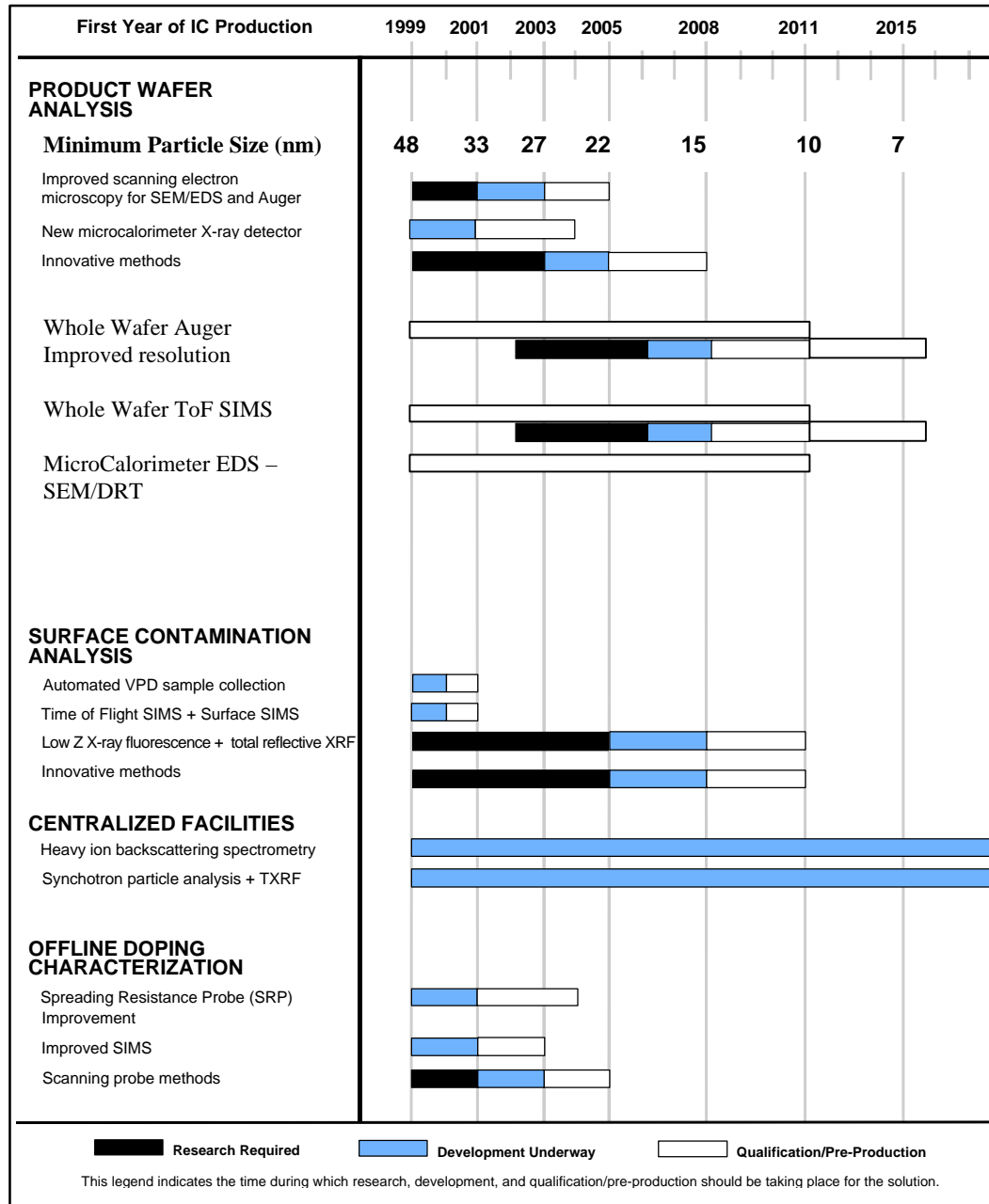


Table 85a Interconnect Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM 1/2 Pitch	180	165	150	130	120	110	100	
MPU Gate Length	140	120	100	85	80	70	65	
<i>Is</i> : MPU Gate Length	140	120	100	90	80	70	65	MPU gate
<i>New</i> : Final Physical Bottom Gate Length after etch (nm)	126	120	100	90	80	70	65	MPU ASIC
Planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) Measurement precision (nm)	25 × 32 250 ± 25	250	250	25 × 36 200 ±20	200	200	25 × 40 175 ±17	MPU
Measurement of deposited barrier layer at thickness (nm) / process range (± 3σ) precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	17/10% <0.06	16/10% 0.05	14/10% <0.05	13/10% 0.04	12/10% 0.04	11/10% <0.04	10/10% 0.03	MPU
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)								
<i>Was</i> : Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× local clock frequency (GHz) [B]	3.5–4.0 1.25	3.5–4.0	2.7–3.0	2.7 – 3.0 2.1	2.2–2.7	2.2–2.6	1.6–2.2 3.5	MPU
<i>Is</i> : Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× local clock frequency (GHz) [B]	2.9 1.25	2.9	2.7	2.7 2.1	2.0	2.0	1.3 3.5	MPU



Table 85b Interconnect Metrology Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Planarity requirements: lithography field (mm × mm)/ planarity for minimum interconnect CD (nm) / measurement precision	25 × 44 175 ±17	25 × 52 175 ±17	175 ±17	MPU
Was: Measurement of deposited barrier layer at Thickness (nm) / process range (± 3σ) Precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	0	0		MPU
Is: Measurement of deposited barrier layer At Thickness (nm)/process range (± 3σ) Precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	7/10% < 0.024	5/10% <0.017	4/10% < 0.013	MPU
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)	↑	↑	↑	MPU
Was: Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× clock frequency (GHz) [B]	< 1.5 6	< 1.5 10	< 1.5 17	MPU

