

Lithography ITWG Report for ITRS Roadmap Workshop

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International SEMATECH**

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San Francisco, California**



International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

Lithography ITWG Attending Members (July 10-11, 2000)

Europe Gerhard Gross, ISMT
 Mauro Visconi, STMicroelectronics

Japan Masaru Sasago, Matsushita

Korea Ki Ho Baik, Hyundai
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Lithography ITWG Report

OUTLINE

- **Key Concerns**
- **Lithography Requirements**
- **Potential Solutions**
- **Difficult Challenges**
- **Summary**



Key Concerns for 2000 ITRS Update

1) Review of technology node timing

2) SOC definition

3) ROI study (model)

4) SOC and MPU chip sizes

5) Technical issues

- Scanner reduction ratio
- Mask (MEF)
- Defect

6) New devices - requirements, etc.



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Technology Node Timing

- **Roadmap timing continues to be one of the major concerns for the Lithography TWG**
- **USA Lithography TWG agreed with ORTC group (Alan Allan, Bob Doering) to work the issue in parallel with other TWGs and other regions**
- **Formed a crosscut TWG group to study timing and chip size issues together; it is called the Technology Node/Chip Size (TNCS) Study Group**
- **TNCS SG has put together a survey with requested input from all regions**
- **Survey has 3 sections:**
 - Timing (same as 1999 LTWG)
 - Chip size
 - Assumptions, models



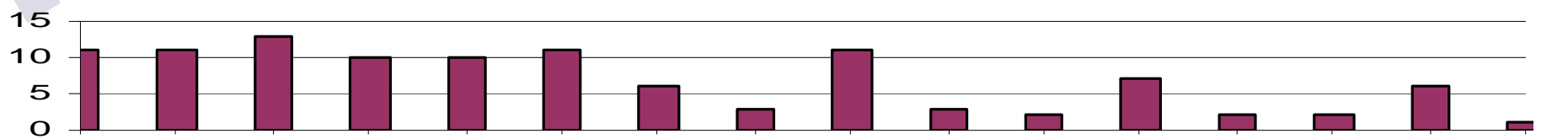
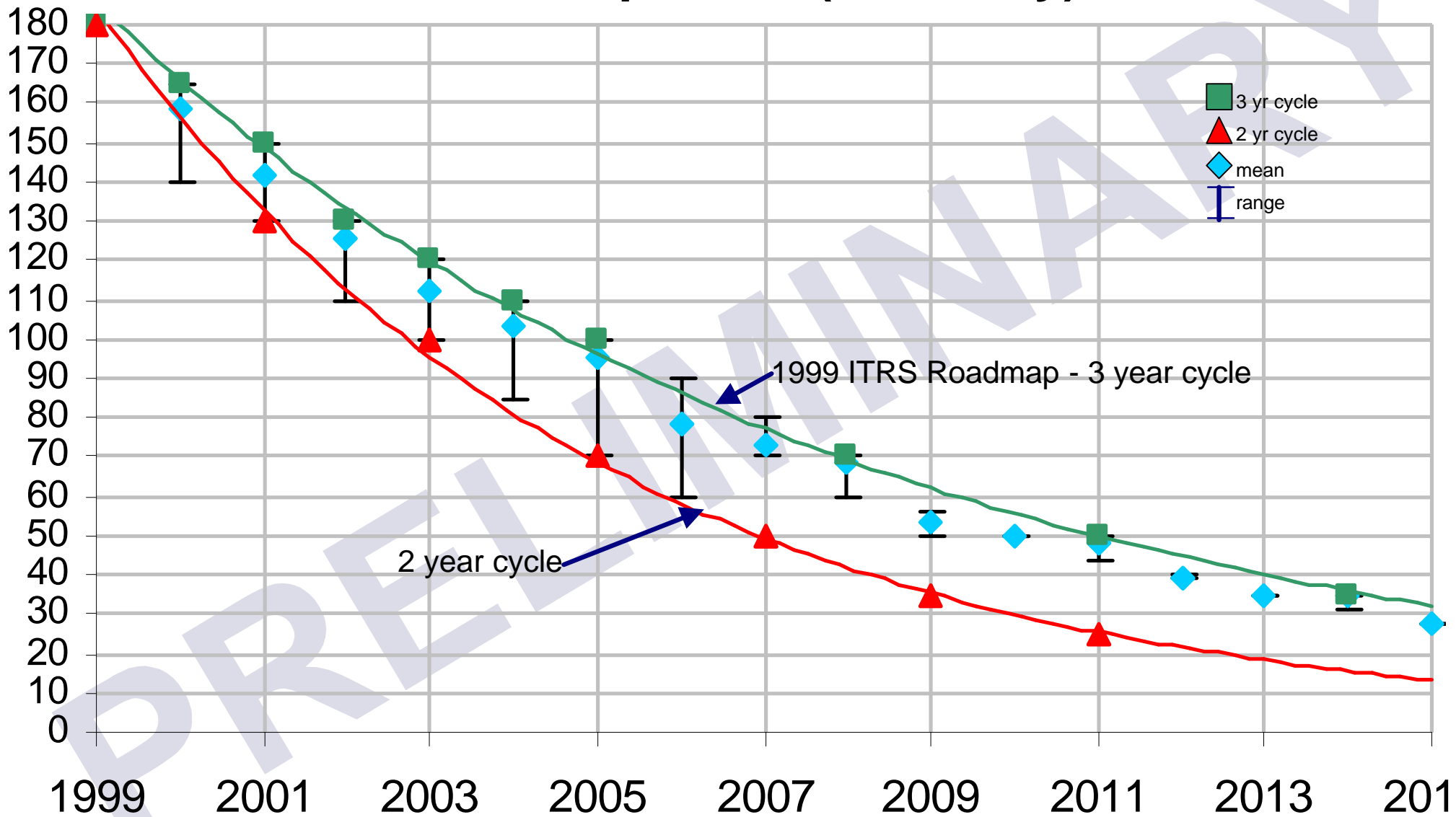
TNCS Study Group Members

LITHO:	John Canning	ISMT
	Pat Gardner	SISA
	George Gomba	IBM
	Harry Levinson	AMD
PIDS:	Peter Zeitzoff	ISMT
DESIGN:	Al Dunlop	Lucent
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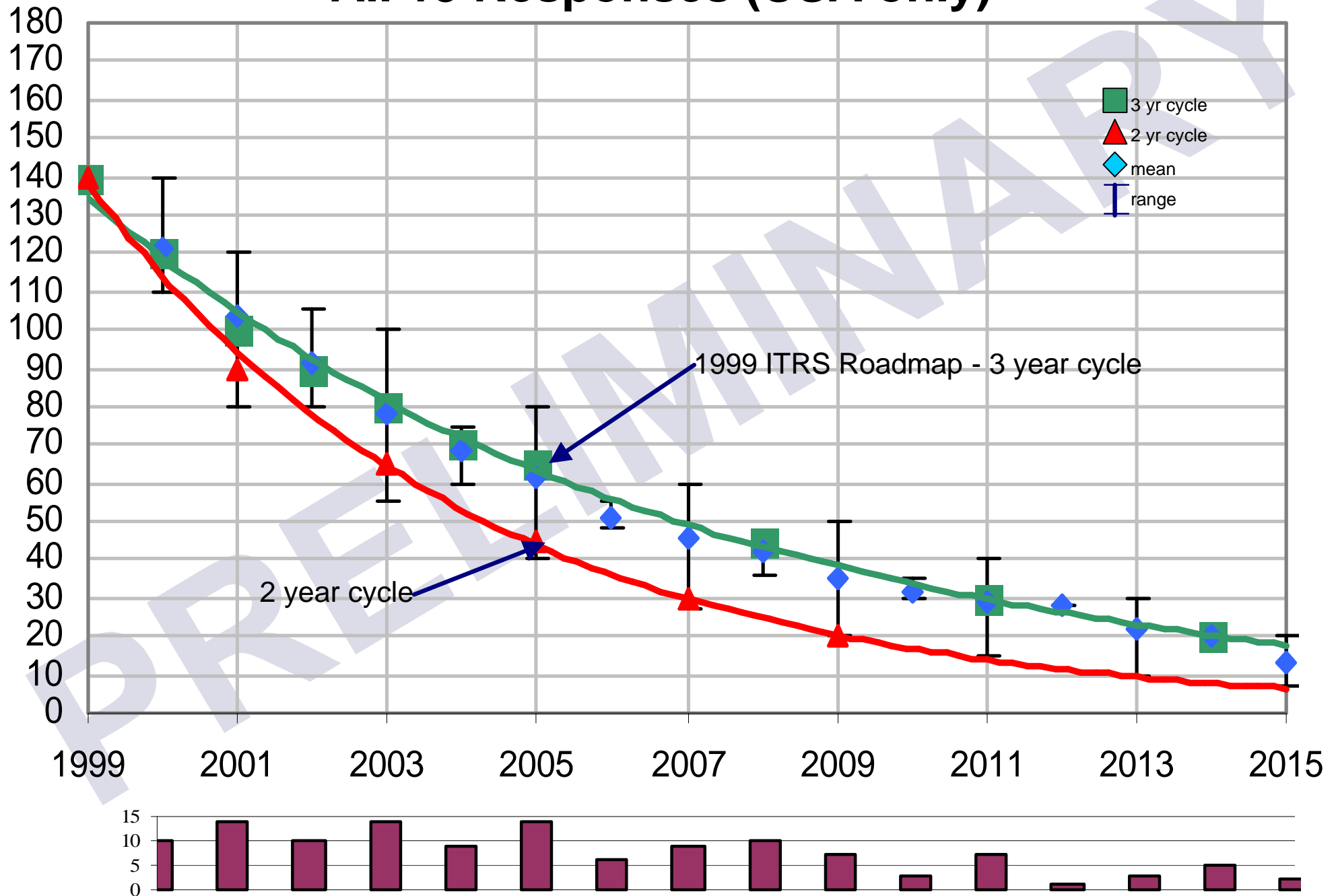


DRAM Half Pitch - 2000 Litho ITWG Survey

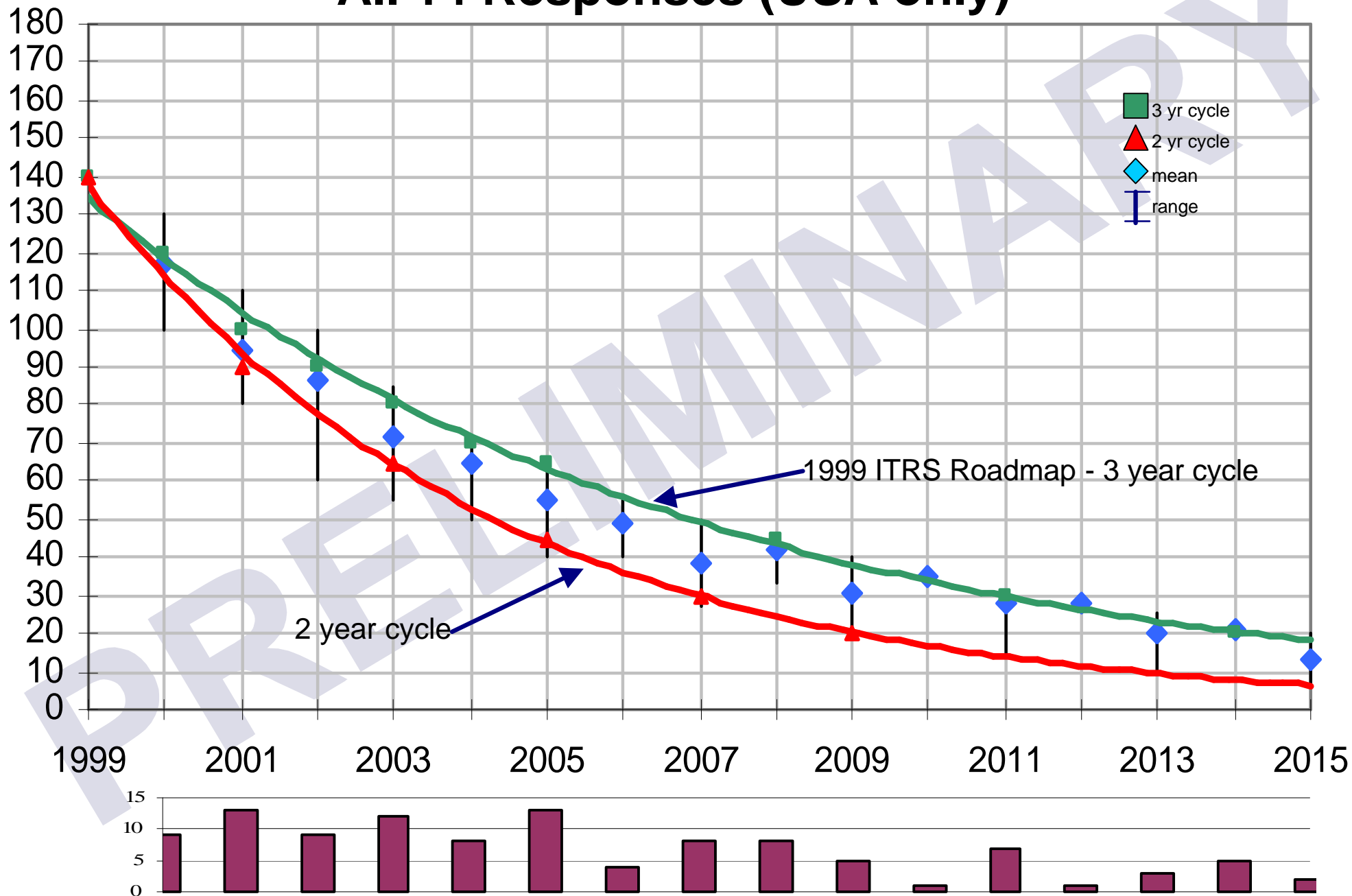
All 14 Responses (USA only)



MPU Gate Length in Resist - 2000 Litho ITWG Survey All 15 Responses (USA only)



MPU Gate Length Post Etch - 2000 Litho ITWG Survey All 14 Responses (USA only)



2000 ITRS Technology Node Timing Status

Lithography ITWG did not reach consensus on accelerating timing

Japan, Europe, and USA recommend staying with 1999 timing (3-year cycle for half-pitch)

USA recommends 1 year pull-in of MPU/ASIC gate length (post-etch)

Europe and Taiwan recommend 2-year cycle for ASIC down to 70nm node

Europe recommends 2-year cycle for DRAM down to 35nm node

Need input from industry and guidance from IRC for 2000 update

Possible solution is 3-year cycle with 2-year cycle “under consideration”

Need two sets of tables

Potential solutions may change



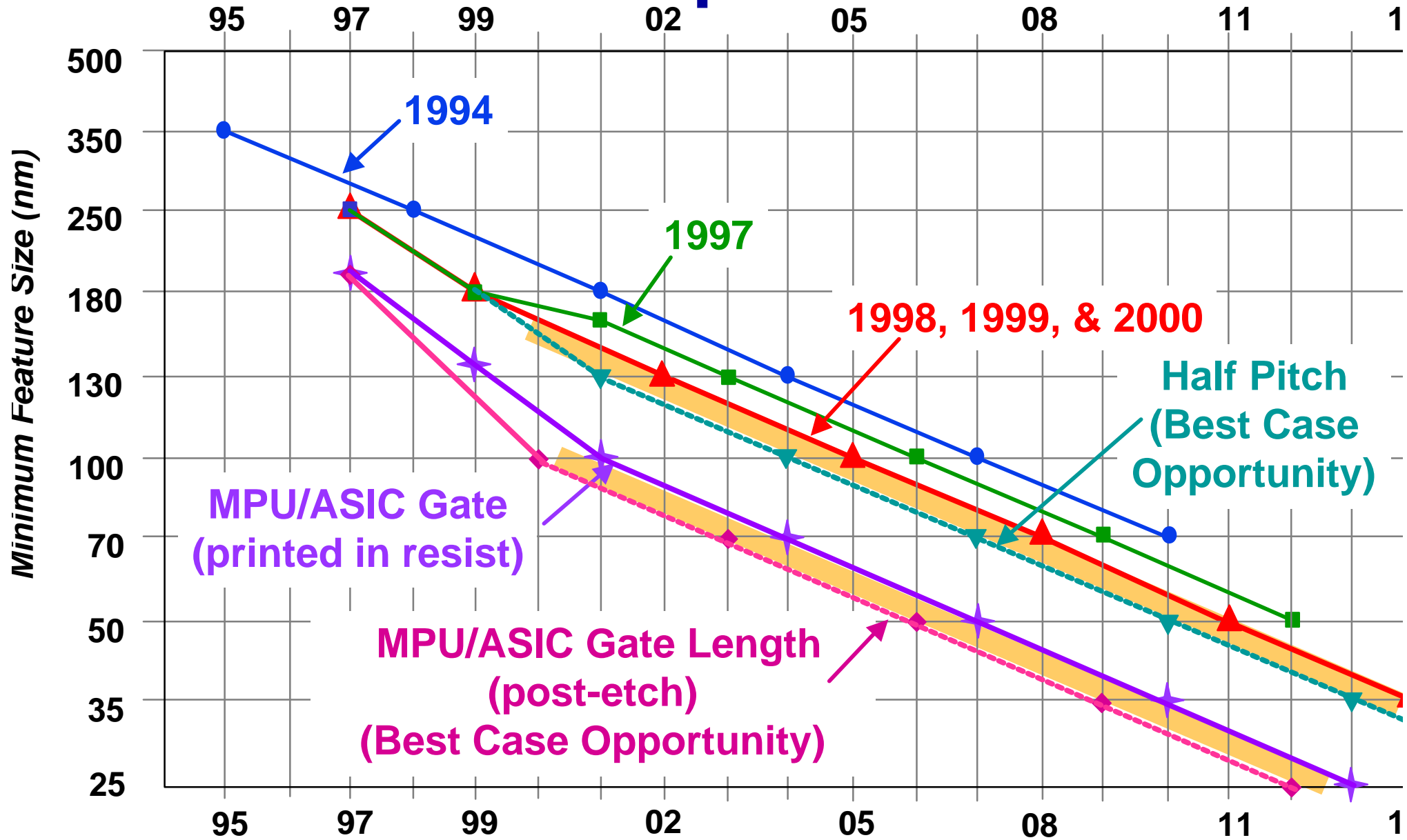
ITRS Technology Node Timing

- **Mask capability is a major limiter to progress**
 - Writers: Accuracy, **CD Control**, Feature Size, OPC, Data Volume, **MEF**, Image Placement
 - Inspection: Defect size, Actinic Capability and PSM
 - Repair: Lacking technology/supplier and PSM
 - Cost/Price: Rapid Escalation \$5k ➡ \$50k

➡ Needs major focus, paradigm shift, global collaboration!



ITRS Roadmap Acceleration



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Key Lithography Characteristics for ORTC

Year Technology Node (half pitch)	1999 180nm	2000	2001	2002 130nm	2003	2004	2005 100nm	2008 70nm	2011 50nm	2014 35nm
DRAM Half Pitch (nm)	180	165	150	130	120	110	100	70	50	35
MPU Half Pitch (nm)	230	210	180	160	145	130	115	80	55	40
MPU Gate Length (in resist, nm)	140	120	100	90	80	70	65	45	33	22
MPU Gate Length (post-etch, nm)*	120	100	90	80	70	65	60	40	30	20
ASIC Half Pitch (nm)	230	210	180	160	145	130	115	70	50	35
ASIC Gate Length (in resist, nm)*	140	120	100	90	80	70	65	45	33	22
ASIC Gate Length (post-etch, nm)	120	100	90	80	70	65	60	40	30	20

* Post-etch values should be used in all “linked” tables for other TWGs (FEP, Interconnect, PIDS, Design, etc.)

Solution Exists

Solution Being Pursued

No Known Solution

Proposed 2000 ITRS Update - 6/26/00 Work-in-Progress - Not for Publication



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2000 ITRS Chip & Field Size Status

High performance (HP) MPU drove maximum field size in 1999
Roadmap ($>800\text{mm}^2$ at 50nm node)

TNCS Study Group reviewed models and current chips in this market segment; 10 chips ranged from 83mm^2 to 477mm^2 with average of 206mm^2

Recommended changing model to cut on-chip cache in half (1M in 1999 and doubling every 2 years)

→ HP MPU size chip at 35nm node $\sim 600\text{mm}^2$

MPU designs can be very flexible, will be driven by economics, and *should not* be used to drive scanner field sizes

Also recommended that scanner field sizes should be driven by DRAM . . . 2 production chips/field



2000 ITRS Chip & Field Size Status

IRC agreed with TNCS SG recommendations at Leuven ITWG meeting

FEP ITWG raised issues with DRAM model, 'a' factor is too aggressive

Currently studying tradeoffs of chip size growth rates, density increase rates, 'a' factor, and scanner field sizes (800mm² @ 4X, and 572mm² @ 5X on 6-inch glass)

Preliminary results can be contained in 572mm² field size

Lithography TWG recommends staying at 6-inch glass for now and studying productivity benefits of 7-inch glass in the future



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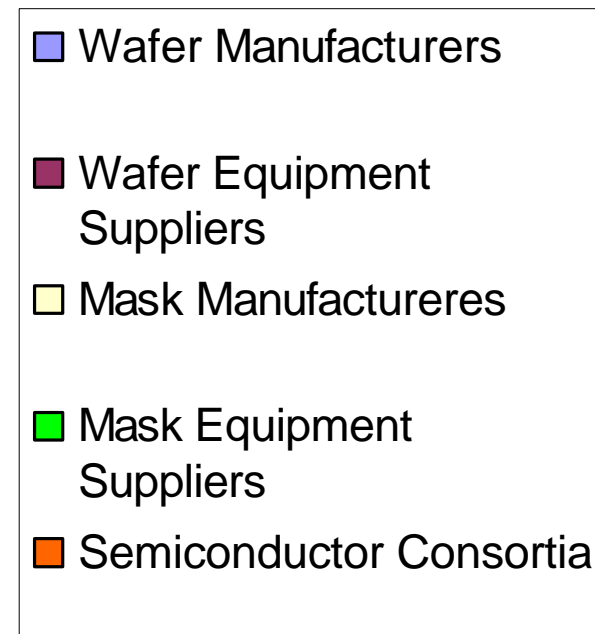
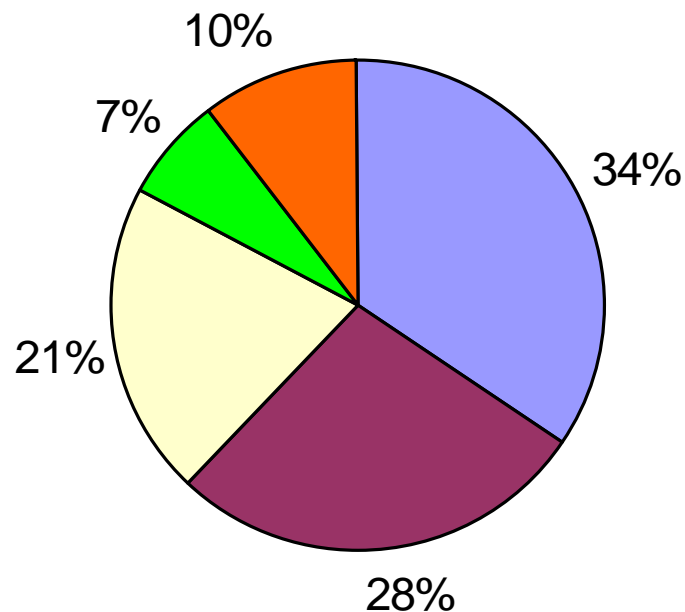
Scanner Reduction Ratio (SRR) Status

- ITWG recommends following issues be addressed at May 8 SRR Workshop organized by ISMT
 - 1) What is the timing? Node, year, wavelength?
 - 2) Comprehensive cost analysis
 - Impact of throughput reduction
 - Impact on mask industry; what real benefit do they get?
 - Does it help accelerate the Roadmap?
 - 3) Complications of 4X, 5X/6X on leading edge mask making?
 - 4) Do all scanner suppliers have to agree? What if they don't?
 - 5) Impact on NGL? Must they follow? Especially EPL?



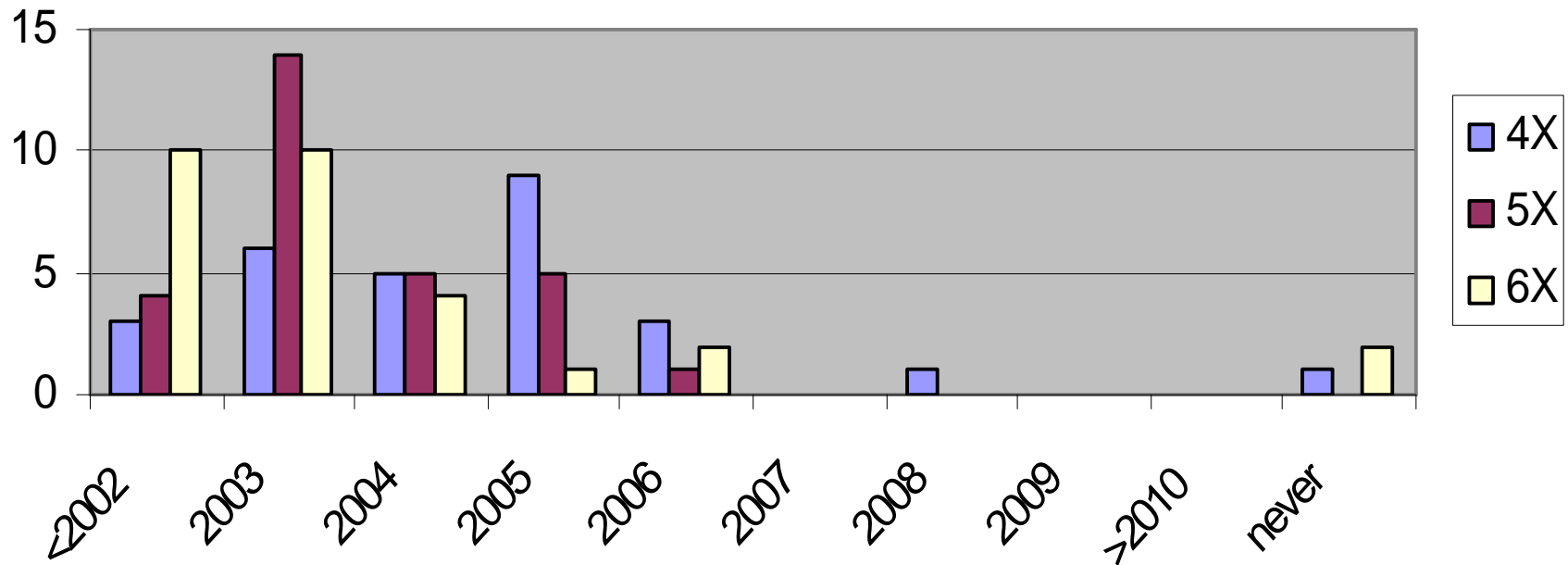
SRR Workshop Attendance (May 8, 2000)

- The 62 attendees represented a broad cross-section of the industry
- Voting restricted to one response per company represented
 - One exception is allowed; “captive mask manufacturers” are asked to vote separately from their respective wafer lines



Mask Availability by Magnification

- **Participants believed that the 100nm node mask availability could be improved by 2 years if magnification increased above 4X**

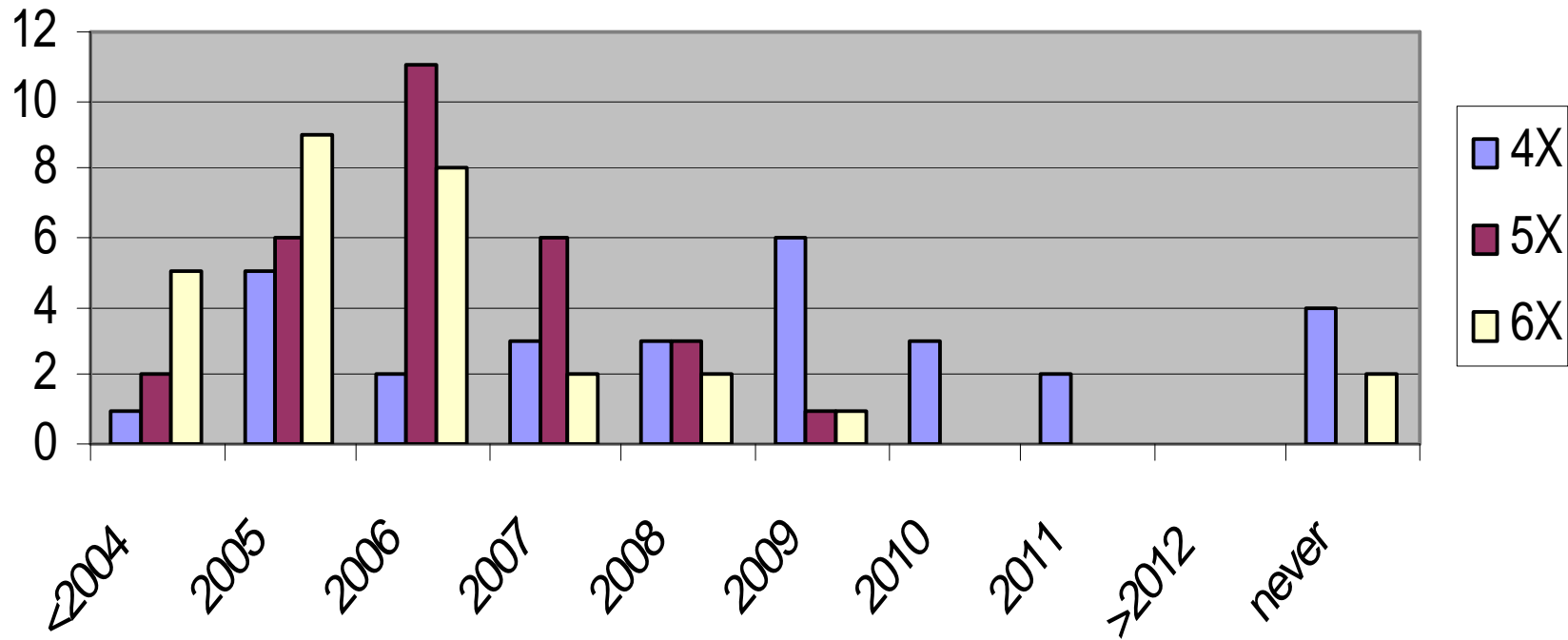


In what year you think mask industry will meet the needs (cost and technology) of the 100nm node?



Mask Availability by Magnification

- **The 70nm node data shows a mixed result for 4X but clear improvement with 5X and 6X.**



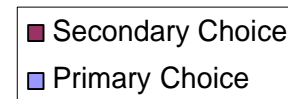
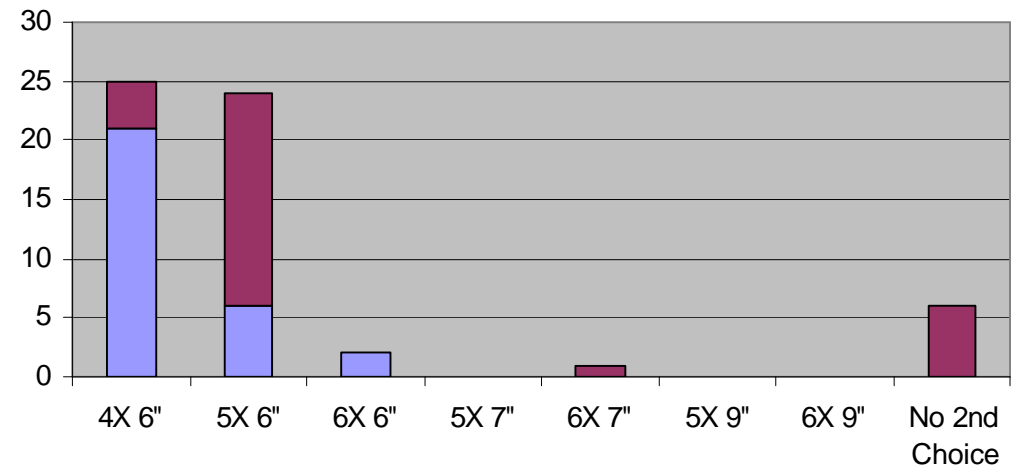
In what year do you think the mask industry will meet the needs (cost and technology) of the 70nm node?



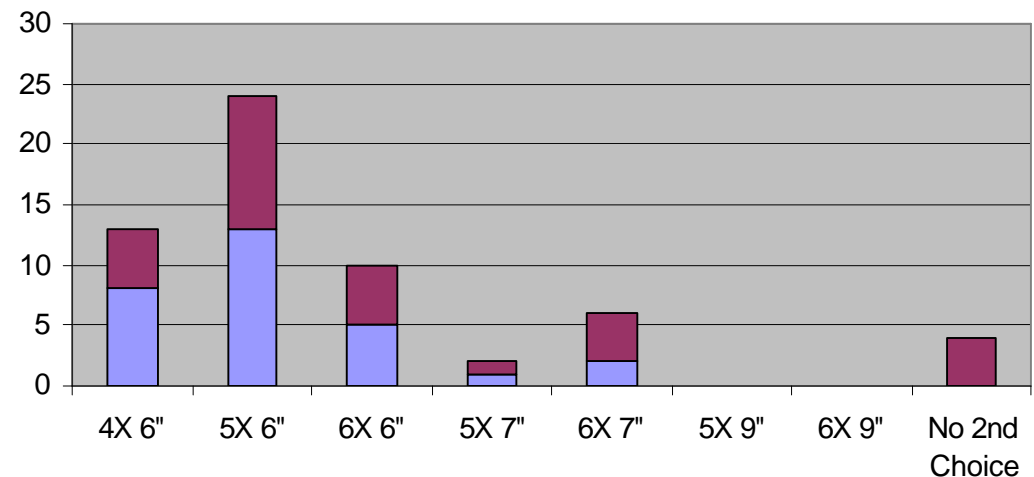
Optical Reticle Size Choice - 193nm

- Stay at 6"
- “Controlled” move to 5X
 - 4X for 100nm node primary choice
 - 5X for 70nm node primary choice
 - 5X secondary choice at 100nm

100nm Node - 193nm



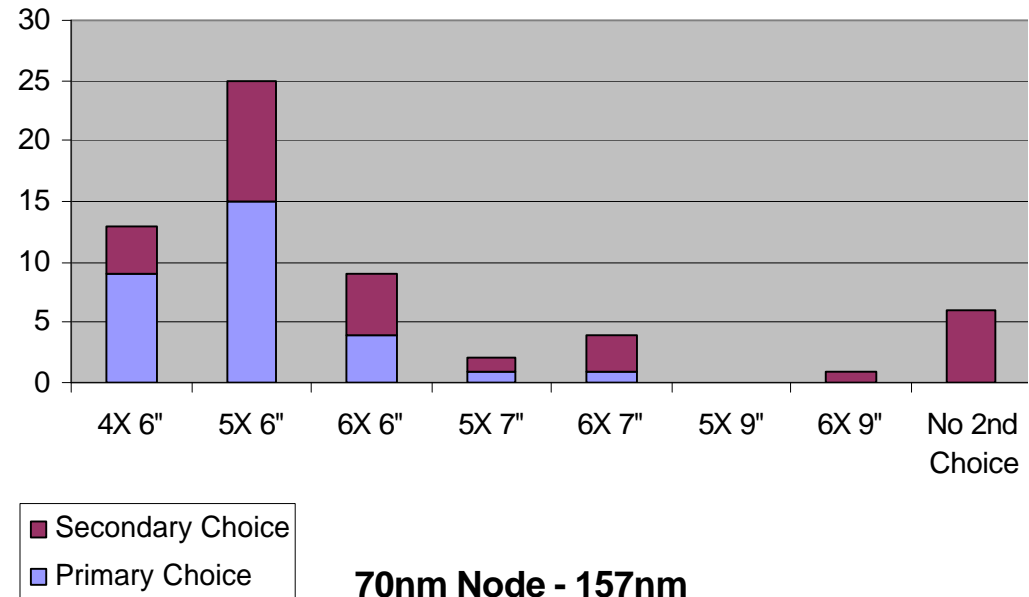
70nm Node - 193nm



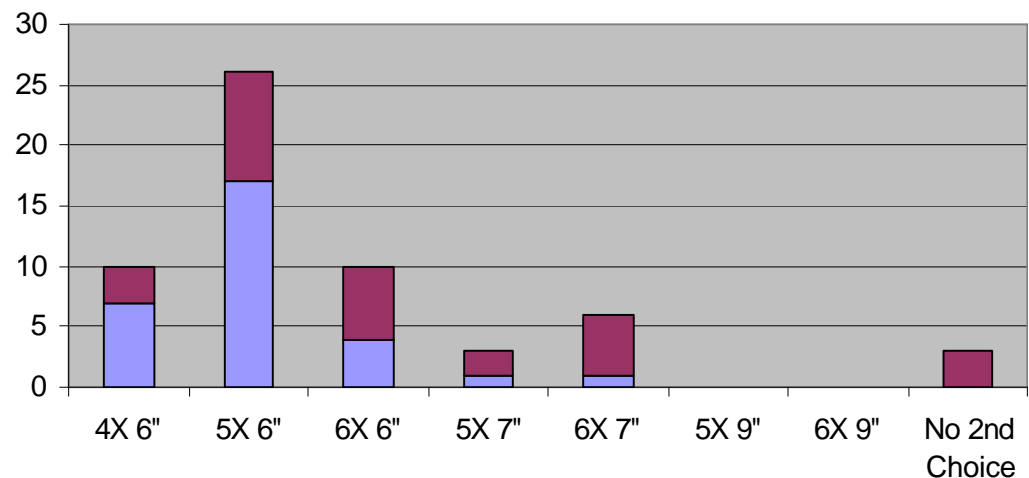
Optical Reticle Size Choice - 157nm

- Stay at 6"
 - Minimal support for larger reticles
 - More support for 7" than 9"
- Introduce 157nm with 5X
- Secondary choice mixed
 - 6X has more votes than 4X

100nm Node - 157nm



70nm Node - 157nm

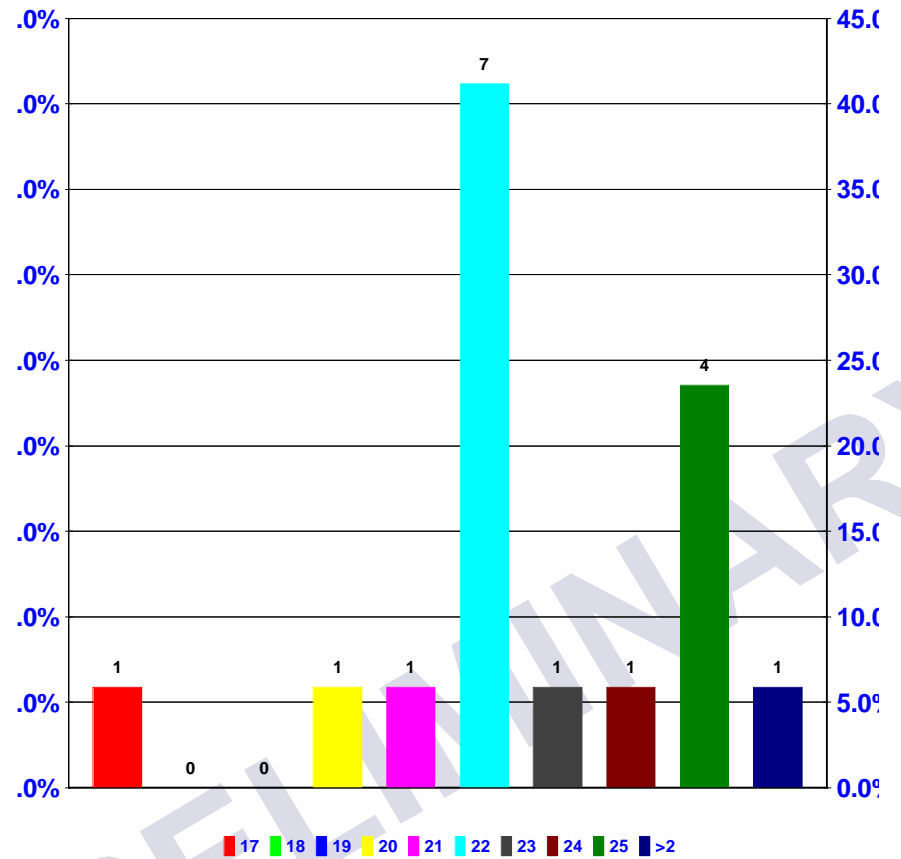
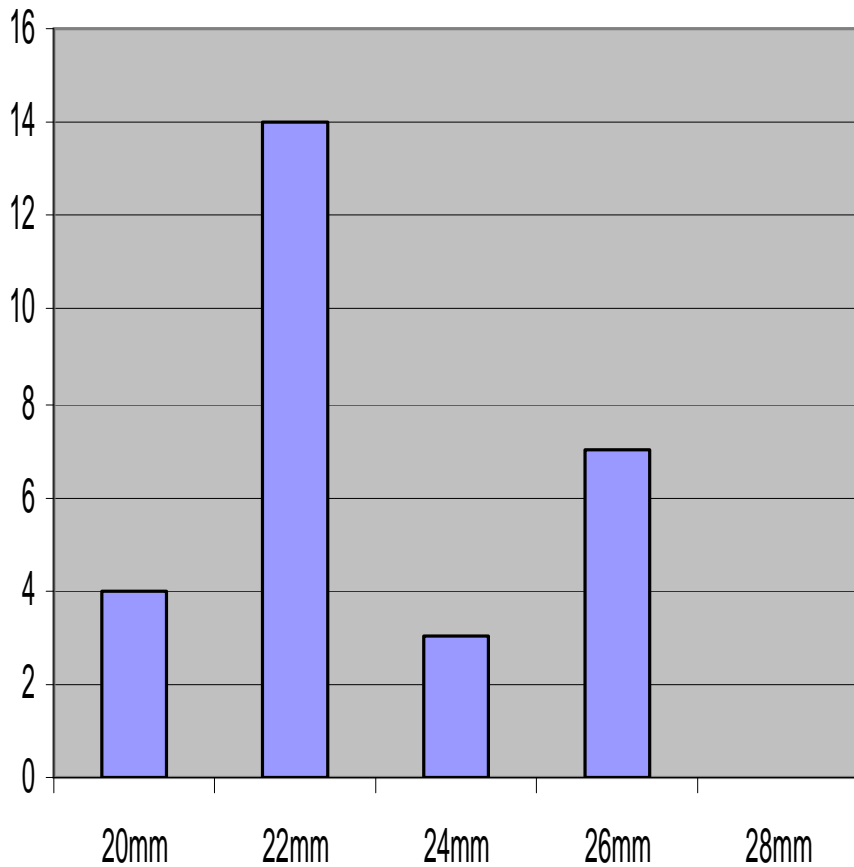


Scanner Slit Height

The slit height is limited by the reticle size and magnification. Majority needs 22mm.

2000

1999



Recommendations of Tool Suppliers (157nm Technology)

	<u>Primary</u>	<u>Secondary</u>
• ASML	5X 6"	
• Canon	6X 7"	5X 6"
• Nikon	4X 6"	(5X 6") *
• SVGL	4X 6"	

* However: If reticle accuracy can not be satisfied in the future, Nikon accepts changing to 5X for 157nm under the conditions of....

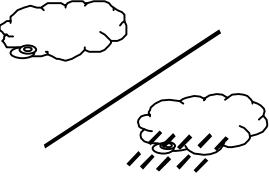
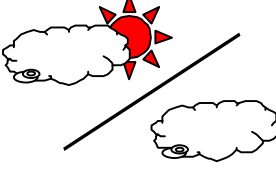
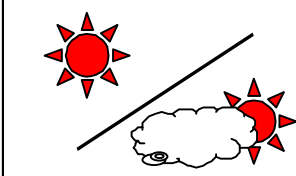
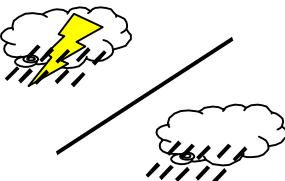
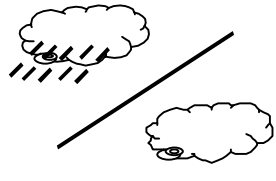
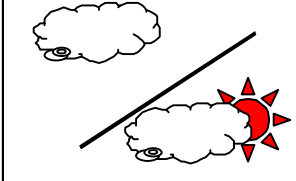
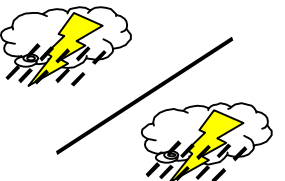
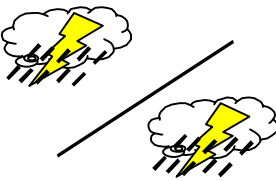
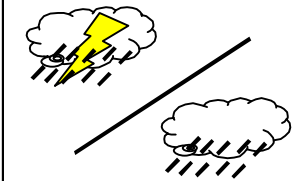
Accepting lower throughput.

Firmly standardizing optical reduction ratio.

Accepting difficulties in mix & match between 4X & 5X.

DNP's "Reticle Weather Forecast"

100nm @ 2003 / 70nm @ 2005

	4x	5x	6x
6"			
7"			
9"			



SRR Workshop Summary

- The majority choice for 157nm & 70nm node:
 - **Mask magnification** **5X**
 - **Slit height** **22mm**
 - **Substrate** **6-inch**



Key Concerns for 2000 ITRS Update

• Mask Error Factor (MEF) and Specifications

- Gil Shelden organized proposals through Optical Extensions & MASC groups for June review
- Mask Error Factor (MEF) is the relation between changes in the pattern found on the mask and the corresponding pattern on the wafer:

$$\text{MEF} = \frac{\partial \text{CD wafer}}{\partial (\text{CD reticle}/M)}$$

where M is the scanner reduction ratio

- Ideally MEF = 1.0. In practice, process variables can significantly increase the MEF as the image fidelity of the scanner deteriorates.



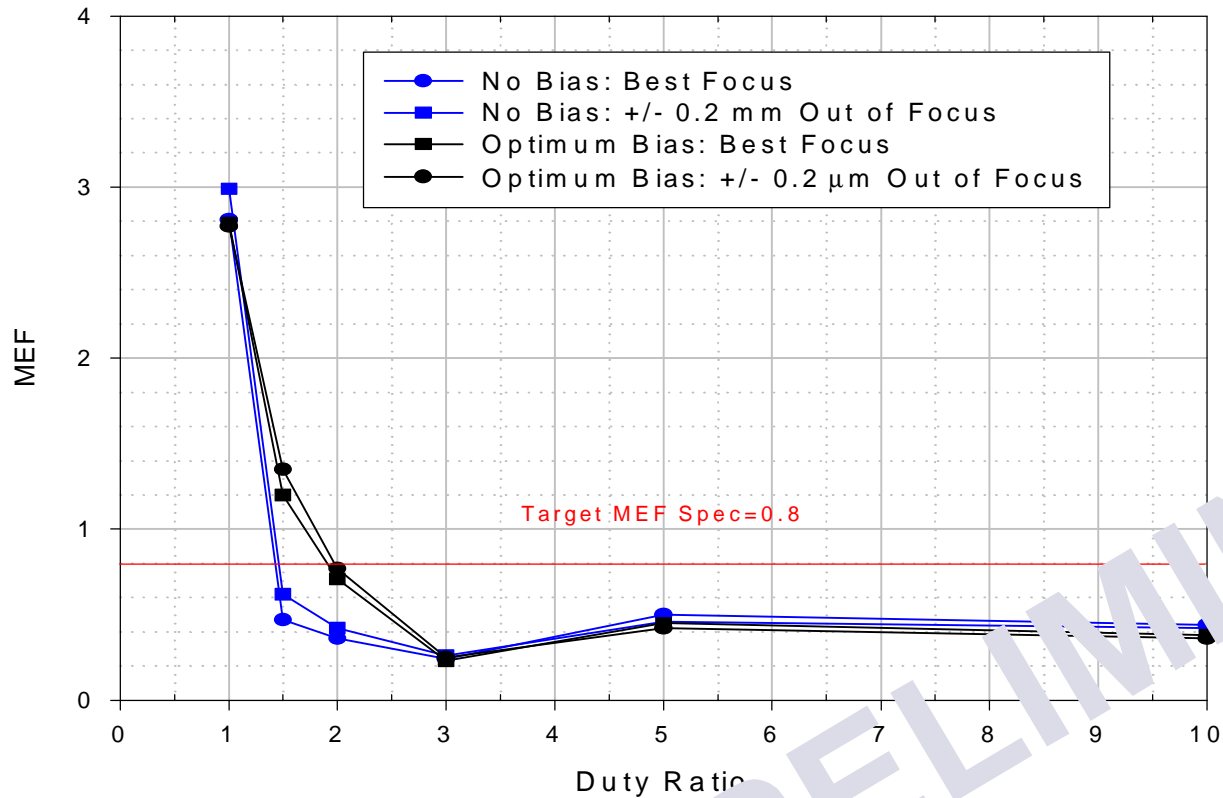
Key Concerns for 2000 ITRS Update

- Mask Error Factor (MEF) and Specifications
 - ISMT contracted with IMEC to study MEF (modeling vs. experimental)
 - Results show MEF increases very rapidly at duty ratio below 1:1.5; alternating PSM technology does NOT solve this issue
 - Mask specifications for dense lines must be much tighter (The 1999 relaxation was shown to be unwarranted)
 - *Recommend same CD uniformity specification for alternating PSM as for binary mask; requires more study in 2001*



MEF As A Function of Pitch for 100nm Lines

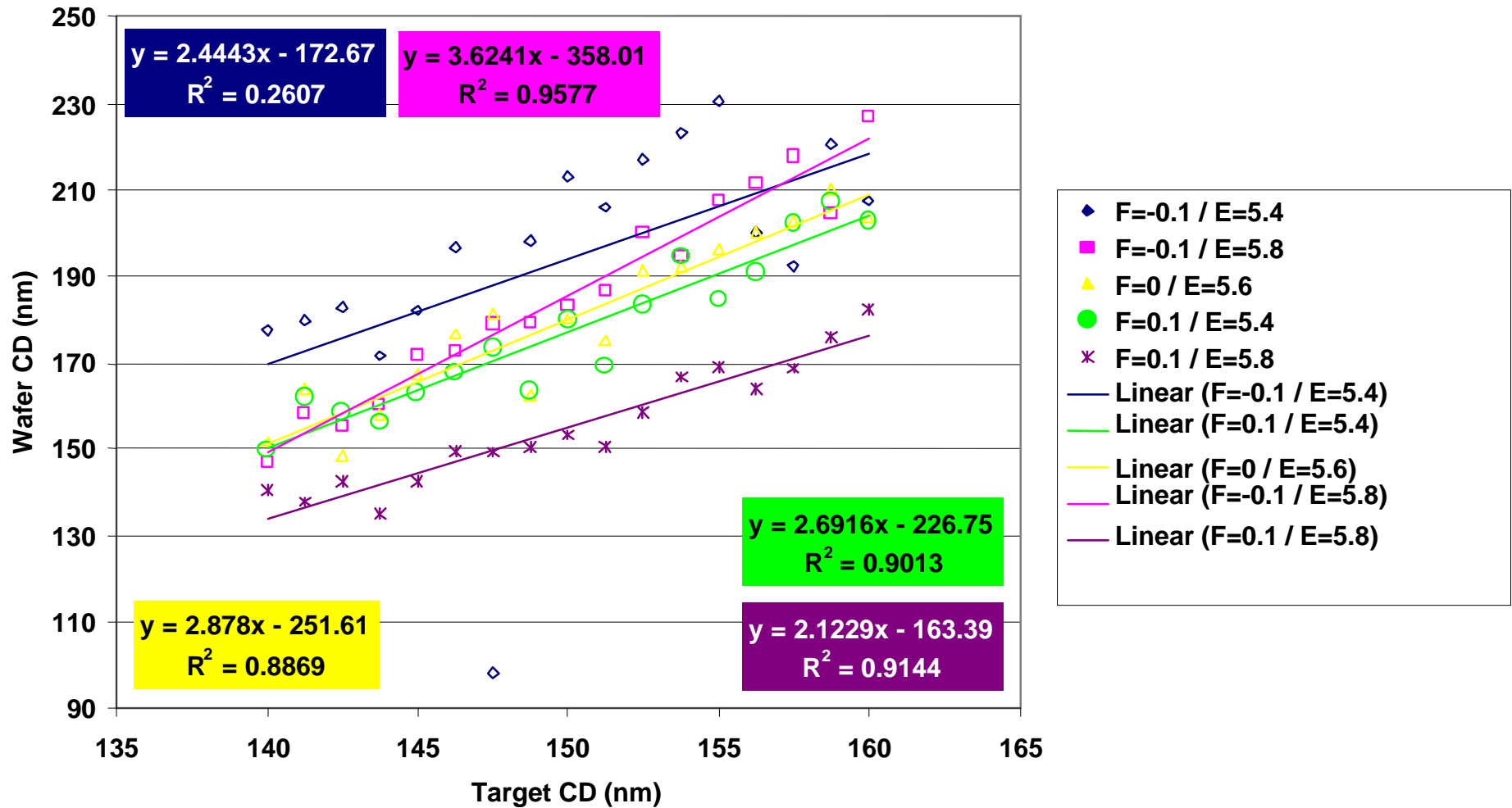
MEF as a Function of Pitch for 100 nm Lines
Sensitivity to Focus
Alternating Phase-Shift Mask, $\lambda=193$ nm, NA=0.55, $\sigma=0.3$



CMG, 3-Feb-2000



Experimental Measurement of MEF



MEF Conclusions

- With proper care, MEF can be measured with a precision of 5% to 10%
- Very good CD uniformity has been measured for 130 nm lines (1X) in a binary and alternating phase shift reticle but the CD uniformity as a function of pitch is a concern, particularly for the alternating phase shift reticle. This concern increases if different features are included on the same reticle.
- When operating near the Rayleigh resolution limit, simulations predict that MEF stays flat and relatively low at high duty ratios but increases very rapidly as the duty ratio decreases below 1:1.5
- Experimental data confirms this trend
- Much higher MEF values for dense lines will be a significant challenge to reticle makers. Given the options available within the next 3 years, careful attention is required to strike a balance between design rules and process capabilities.



Lithography Requirements

- Exposure Tools - Table 39
 - Continuous improvements in 248nm tools and processes have demonstrated solutions for DRAM and MPU down to 150nm half pitch, including CD control of 10nm
 - MFS for development has been demonstrated down to 70nm with 193nm + PSM
 - CD control solutions are being pursued down to 6nm by engineering analysis of error sources (mask, process, tool)
- Resists - Table 40
 - Resist thickness solutions now exist down to 0.33 - 0.44 μm
 - PEB solutions exist at 3nm / $^{\circ}\text{C}$ with 248nm resists
 - Resist sensitivity solutions exist for all resists except 157nm; solutions are being pursued at MIT/LL and suppliers for 157nm at 5-10 mJ/cm^2
- Masks - Table 41
 - Based on development of 50KeV e-beam writers, solutions now exist for mask minimum image size and OPC feature size to 200nm, image placement to 27nm, CD uniformity to 15nm, and linearity to 20nm
 - CD uniformity for dense lines with alternating PSM must be much tighter due to better understanding of MEF



Lithography Requirements - Overview

Year of Introduction	1999	2002	2005	2008	2011	2014
Dense Lines (nm) (DRAM half pitch)	180	130	100	70	50	35
Isolated Lines (nm) (gate length, printed in resist)	140	90	65	45	33	22
Isolated Lines (nm) (gate length, post-etch)	120	80	60	40	30	20
Gate CD Control (nm) (3 sigma post-etch)	12	8	6	4	3	2
Overlay (nm) (mean + 3 sigma)	65	45	35	25	20	15
Minimum Field Area (mm ²) (driven by DRAM) (2 production chips/field)	262	376	462	444	394	450
Mask Blank Size (mm) (square) (diameter)	152	152	152 200	152 200	152 200	152 200

Solution Exists

Solution Being Pursued

No Known Solution

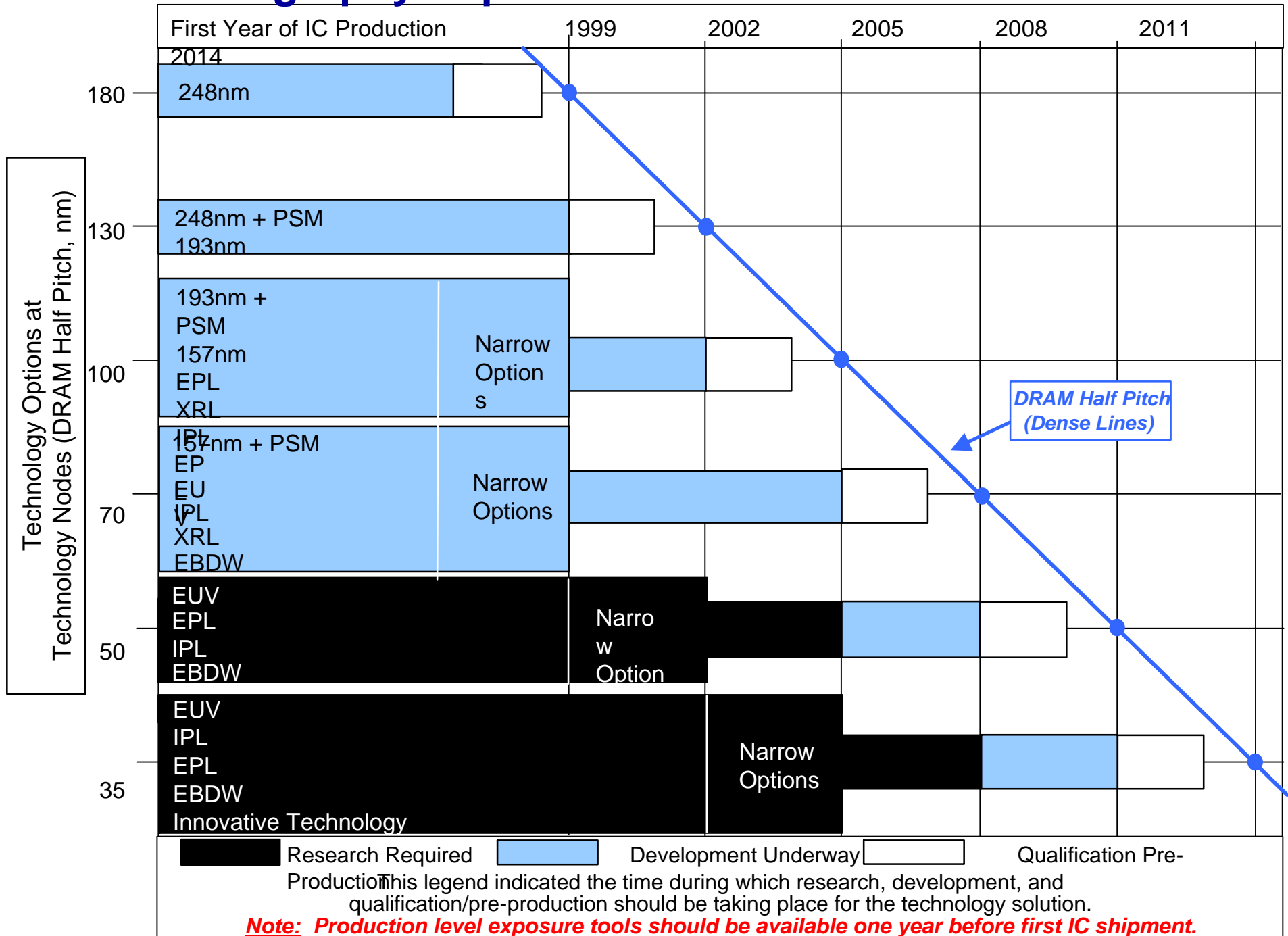
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Lithography Exposure Tool Potential Solutions



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Lithography Difficult Challenges - Before 2005

<i>Five Difficult Challenges ³ 100 nm Before 2005</i>	<i>Summary of Issues</i>
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., 157nm substrates and films; defect free multi-layer substrate or membranes). Development of equipment infrastructure (writers, inspection, repair) for relatively small market.
Lithography technology consensus (193nm + RET, 157nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes. Achieving global consensus among technology developers and chip manufacturers.
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, i.e. low cost masks. Achieving ROI for industry (chipmakers, E+M suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma.
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option.

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Lithography Difficult Challenges - Beyond 2005

<i>Five Difficult Challenges < 100nm Beyond 2005</i>	<i>Summary of Issues</i>
Mask fabrication and process control	<p>Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., 157nm substrates and films; defect free multi-layer substrate or membranes)</p> <p>Development of equipment infrastructure (writers, inspection, repair) for relatively small market</p> <p>Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes</p>
Metrology and defect inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection for defects < 40nm.
Cost control and return on investment (ROI)	<p>Development of innovative technologies, tools, and materials to maintain historic productivity improvements</p> <p>Achieving constant/improved throughput with post-optical technologies</p> <p>Achieving ROI for industry (chipmakers, E+M suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100nm and below.</p>
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option



Lithography ITWG Report - Summary

- **Technology node timing is biggest challenge / issue for Lithography**
 - *Mask capability is key limiter to progress*
- **Lithography ITWG has not reached consensus on timing for 2000 update**
 - *Need input from industry and guidance from IRC*
- **DRAM & MPU chip size proposals offer significant relief for lithography tools and masks**
 - Field size $<550\text{mm}^2$ allows 5X reduction on 6-inch glass option
 - *Recommend field size be driven by DRAM ... 2 production chips/field*
 - *Recommend staying at 6-inch glass for now*



Lithography ITWG Report - Summary

- **Optical mask requirements for dense lines are much tighter based on latest understanding of mask error function (MEF)**
 - *Recommend same CD uniformity specification for alternating PSM as for binary masks*
- **Increased scanner reduction ratio offers some relief for mask specifications**
 - *Recommend adding 5X as an option at 100nm and 70nm nodes*
- **Cost control and ROI continue to be major concerns for acceleration at 100nm - 50nm nodes (single node solutions)**



Lithography ITWG Report

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Taiwan

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Anthony Yen

USA

George Gomba

Gil Shelden



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