ITRS/ Design TWG Update 2000

System on Chip, Design Productivity, Low Power, Deep Submicron Design requirements, Future role of Design, Living Roadmap

ITRS 2000 Update

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International Technology Roadmap for Semiconductors

Model for SOC Design
(a reasonable scenario)

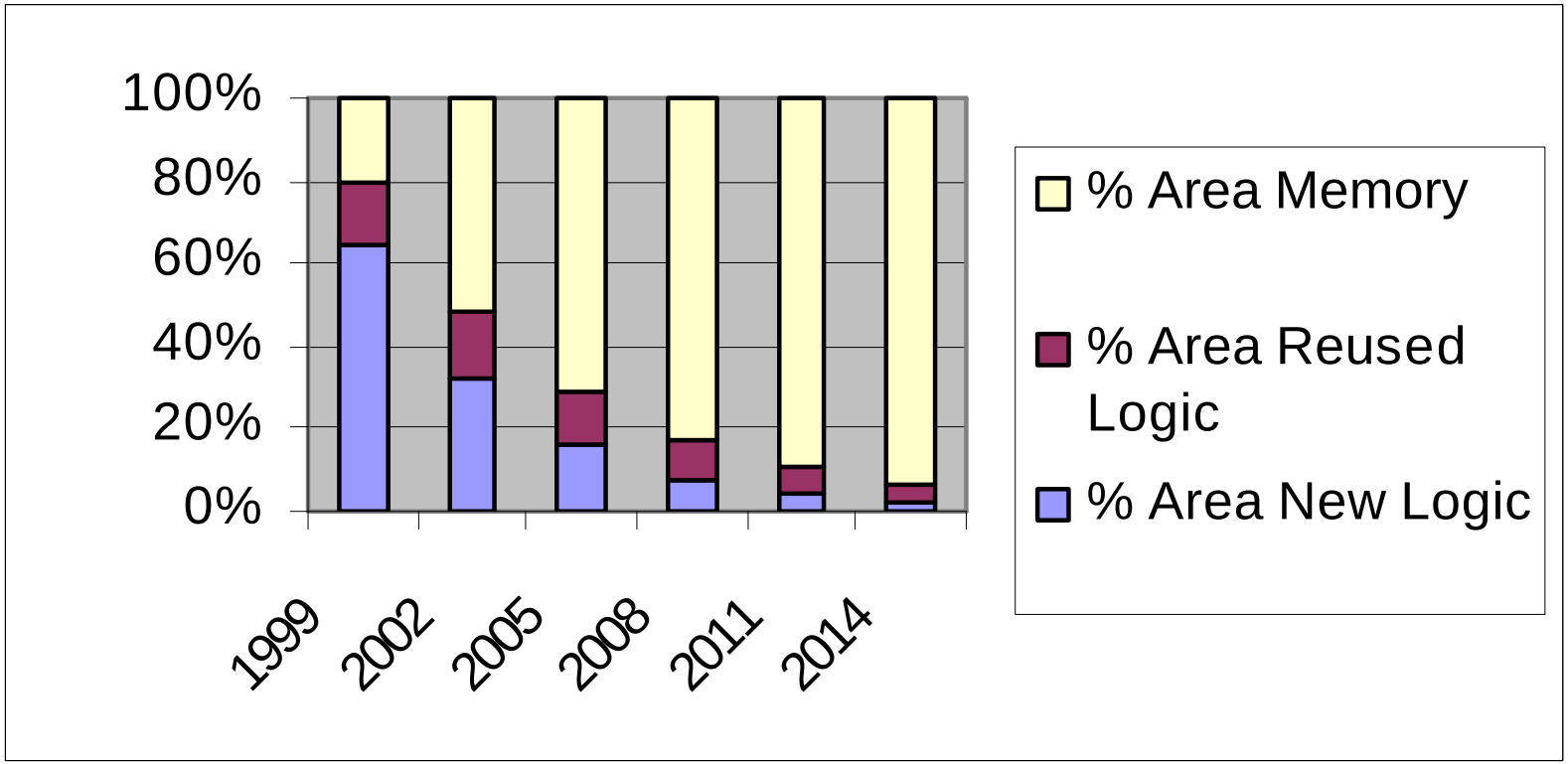
- Design effort = constant (small design team, short time to product)
- New design productivity (logic) : + 30%/yr
- (Reuse design productivity) / (New design productivity) = 2 (constant)
- Memory is free
- Chip size is up to 1 cm^2
  - ➡ use up to max die size "for free"

Result:
up to 94 % of die occupied by memory, or smaller die

Scenario for SoC Productivity

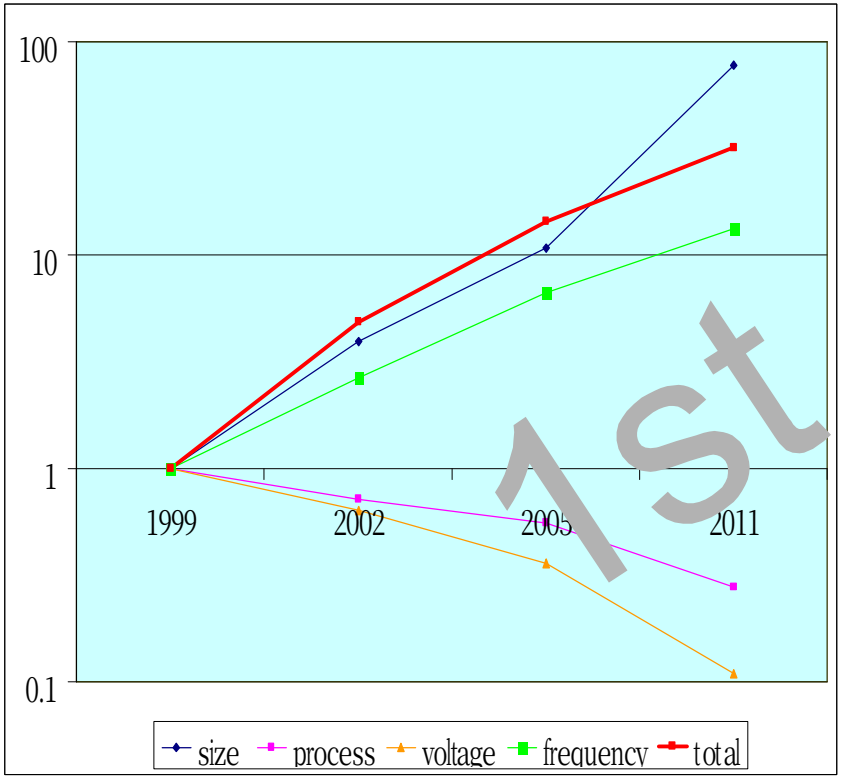
Year	1999	2002	2005	2008	2011	2014
Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
% Area New Logic	64%	32%	16%	8%	4%	2%
% Area Reused Logic	16%	16%	13%	9%	6%	4%
% Area Memory	20%	52%	71%	83%	90%	94%
Transistor Logic Density (Mtrans/cm2)	20	54	133	328	811	2000
New Logic Productivity (Mtrans/PY)	1,4	2,1	2,9	4,2	6,0	8,6
Reused Logic Productivity (Mtrans/PY)	2,9	4,1	5,9	8,4	12,0	17,1
Target Design Resource (PY)	10,0	10,5	10,1	9,9	9,7	9,6

Scenario: major increase in memory content

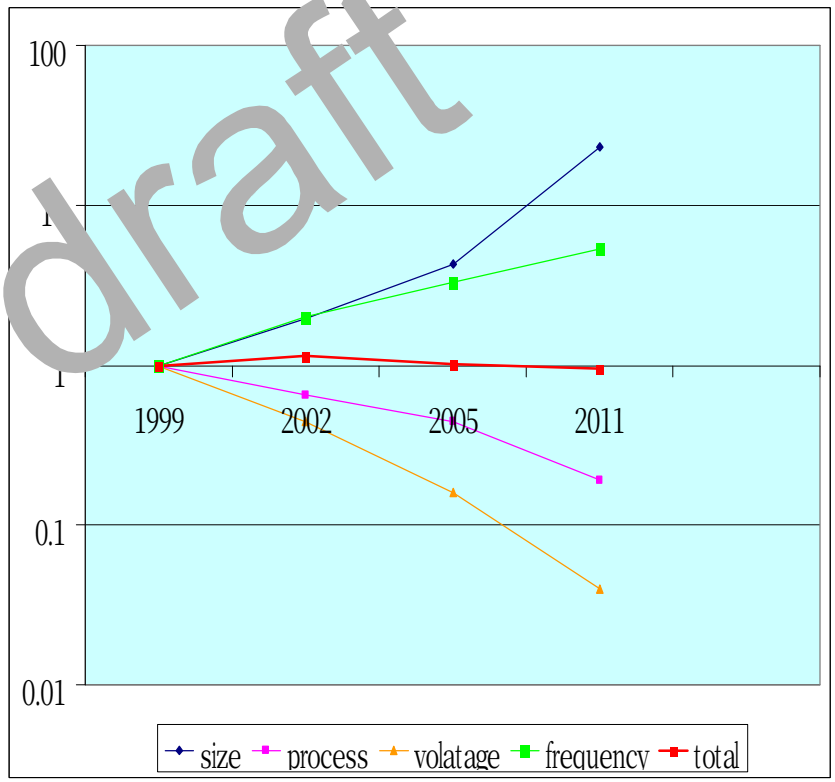


SOC Low Power

Total Power Trend with
No Low Power Solution



Total Power Trend with
Low Power Solution Scenario
to keep 3W



ITRS, meeting in Leuven

An overall DSM requirements table

(table 2-1-4-1) DSM requirements

			unit	1999	2002	2005	2011	Reference
Base data/Condition		Technology node	nm	180	130	100	50	
		Nominal Ion [25c,NMOS,low power]	uA/um	490	490	490	490	ITRS99 Table28
		Nominal Ion [25c,PMOS,low power]	uA/um	230	230	230	230	ITRS99 Table28
		Voltage	V	1.5	1.2	0.9	0.6	STRJ-WG1/LP-SWG
		Frequency	MHz	150	400	1000	2000	STRJ-WG1/LP-SWG
		Die size	cm?	1	1	1	1	STRJ-WG1/LP-SWG
		Metal height/width aspect		2	2.1	1.7	2.1	STRJ -WG4
		Metal effective resistivity	? O-cm	2.2	2.2	2.2	<1.8	STRJ -WG4
		Maximum metal current	mA	2.16	1.56	1.2	0.6	STRJ -WG4
DSM Category								
Signal Integrity	**Crosstalk noise** Required	Required parallel interconnect maximum allowable length which considers parastic capacitence effect	mm	1.08	0.78	0.60	0.30	⬅(*a) Next Page
	Estimated	Estimated parallel interconnect maximum allowable length which considers parastic capacitence effect	mm	2.70	0.21	0.00	0.00	⬅ See tab.2-1-4-2
	RC delay Required	Required interconnect maximum allowable length which considers resistence	mm	10	10	10	10	⬅(*b) Next Page
	Estimated	Estimated interconnect maximum allowable length which considers resistence	mm	289	67	12	2	⬅ See tab.2-1-4-3
	Inductance	Interconnect Inductance Effect				CP1 (*1)	CP2 (*2)	
	EMI Allowed	Allowable EMI by FCCclassB (at a distance of 3.0m)	uV/m	150	200	500	500	⬅(*c) Next Page
	Estimated	Estimated EMI by a chip (observation point =3.0m)	uV/m	11	22	43	43	⬅ See tab.2-1-4-4
Reliability	**IR drop** Required	Required maximum allowable number of FF which is driven by power line without failure due to IR Drop.		20	20	20	20	⬅(*d) Next Page
	Estimated	Estimated maximum allowable number of FF which is driven by power line without failure due to IR Drop.		34	21	10	5	⬅ See tab.2-1-4-5
	ElectroMigration	Number of Power Pads (High Performance)		**342**	**472**	**800**	**1,066**	
		Number of Power Pads (Battery/Hand-Held)		**6**	**9**	**16**	**16**	⬅ See tab.2-1-4-6
		Number of Power Pads (Target of LP-SWG)		**2**	**2**	**3**	**4**	
Manufacture	OPE	Optical Proximity Correction				CP	CP	

CP1(1st Crisis Point): Interconnect effects becomes critical in high speed blocks(1GHz).
CP2(2nd Crisis Point): Interconnect effects becomes major delay in high speed blocks(2GHz).

Role of Design in ITRS

- **Before 1999:**
  - **Addressed primarily hardware design and test tool issues and technologies**
  - **Largely ignored**

- **1999**
  - **Highlighted SoC trends and requirements**
  - **Received many requests from other TWGS**

Role of Design in ITRS (cont'd)

- **2001 and Beyond**
  - **Needs to be involved in crosscut issues with other TWGs**
    - **E.g., proposed crosscut panel on interconnect systems and optimization (including design, interconnect, packaging, PIDS, etc.)**
    - **More bidirectional interactions with other TWGs**
  - **Needs to expand into new and important areas:**
    - **Applications**
    - **Architectures**
    - **Optimized uses of process technology**
    - **Analog/mixed signal and other technologies**

Proposal: A Living Roadmap

- **Areas for improvement in the ITRS**
  - Documentation and transparency
    - internal calculations, calibration data, assumptions, best-guesses
  - Flexibility
    - Currently, only a single “hard-wired” Roadmap
    - Need facilities to explore alternative modeling choices, check self-consistency, perform extrapolations and parameter optimizations, …
  - Quality and adoptability
    - Best available data, models in all aspects; movable behind firewalls
- **Internal roadmaps : incomplete, not interoperable w/ITRS**
- **Proposal : living, open ITRS**
  - First step: Excel spreadsheets complete, fully documented, integrated
  - Initialization + support : ITRS TWGs + IRC, MARCO GSRC

The World of the Living Roadmap

ITRS

Technology Models

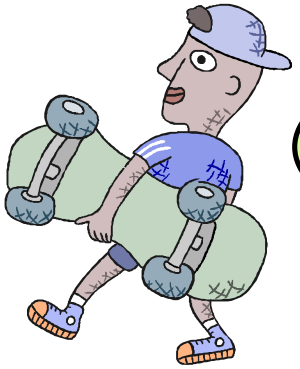
Firewall

Proprietary Models

The Internet

Sematech, GSRC

"The Golden Copy"



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