

## Proposal to ITRS2000

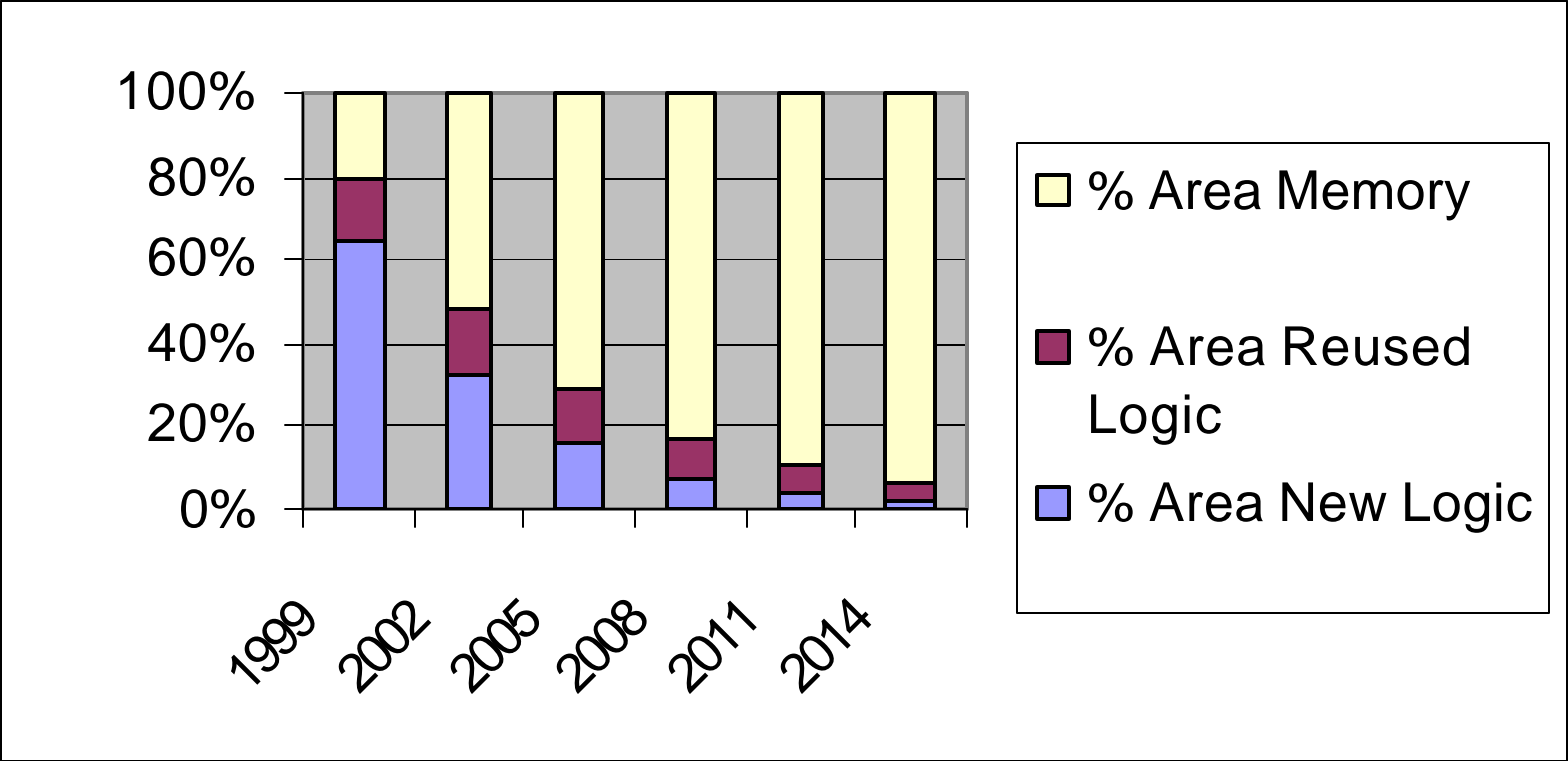
- Design Prediction Tables are needed  
More quantitative description needed

→ Put some design prediction tables, such as STRJ developed Design Productivity, Low Power and DSM tables

# Scenario for SoC Productivity

Year	1999	2002	2005	2008	2011	2014
Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
% Area New Logic	64%	32%	16%	8%	4%	2%
% Area Reused Logic	16%	16%	13%	9%	6%	4%
% Area Memory	20%	52%	71%	83%	90%	94%
Transistor Logic Density (Mtrans/cm <sup>2</sup> )	20	54	133	328	811	2000
New Logic Productivity (Mtrans/PY)	1,4	2,1	2,9	4,2	6,0	8,6
Reused Logic Productivity (Mtrans/PY)	2,9	4,1	5,9	8,4	12,0	17,1
Target Design Resource (PY)	10,0	10,5	10,1	9,9	9,7	9,6

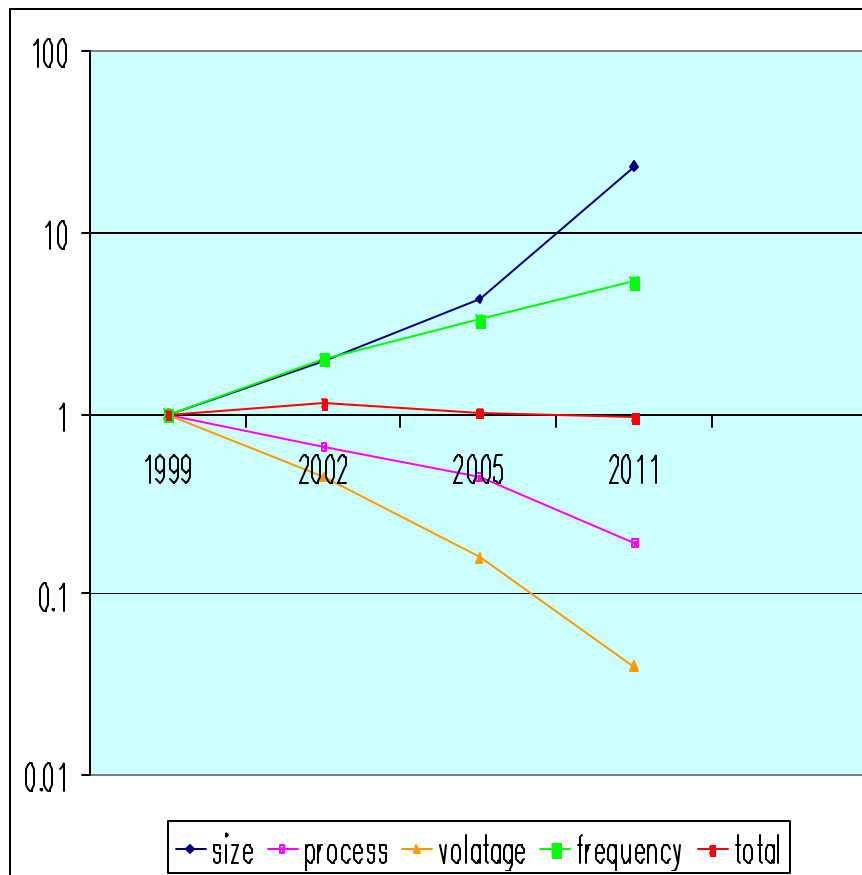
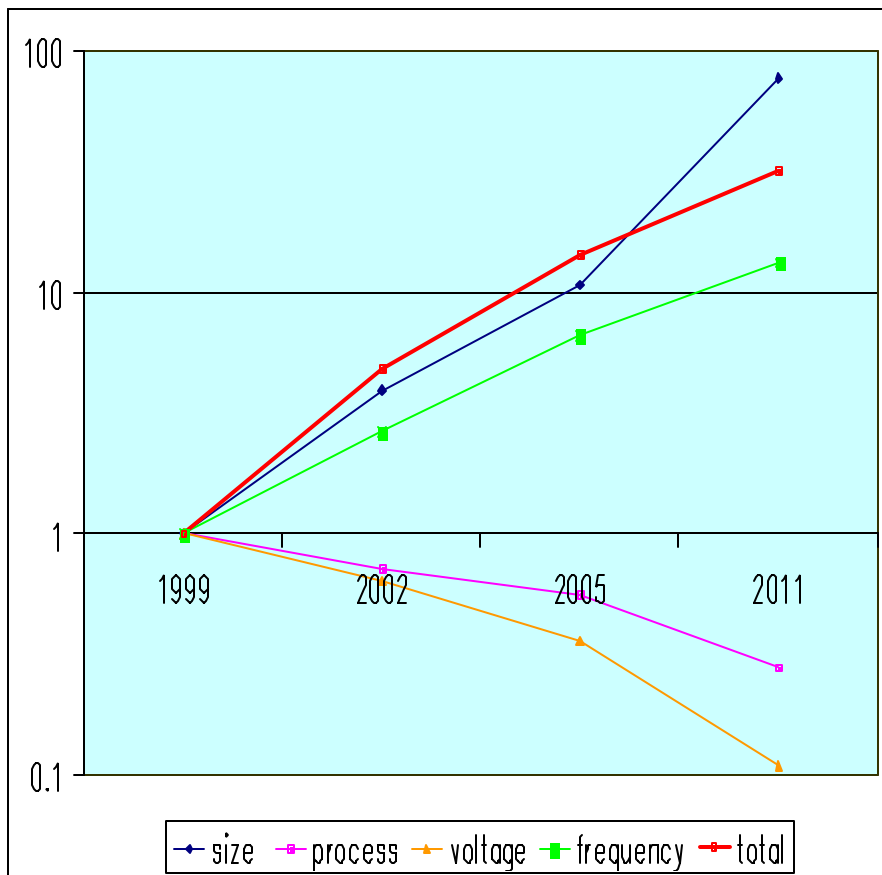
**ITRS, meeting in Leuven**



# SOC Low Power (cont.)

Total Power Trend with No Low Power Solution

Total Power Trend with Low Power Solution Scenario to keep 3W



ITRS, meeting in Leuven

# An overall DSM requirements table

(table 2-1-4-1) DSM requirements

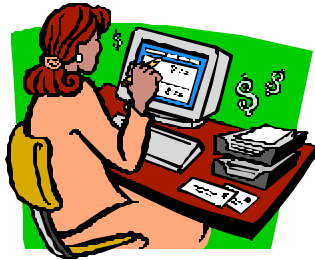
Base data/Condition			unit	1999	2002	2005	2011	Reference	
		Technology node	nm	180	130	100	50		
Nominal Ion [25c,NMOS,low power]		uA/um	490	490	490	490		ITRS99 Table28	
Nominal Ion [25c,PMOS,low power]		uA/um	230	230	230	230		ITRS99 Table28	
Voltage		V	1.5	1.2	0.9	0.6		STRJ-WG1/LP-SWG	
Frequency		MHz	150	400	1000	2000		STRJ-WG1/LP-SWG	
Die size		cm <sup>2</sup>	1	1	1	1		STRJ-WG1/LP-SWG	
Metal height/width aspect			2	2.1	1.7	2.1		STRJ -WG4	
Metal effective resistivity		$\frac{\mu\Omega}{cm}$	2.2	2.2	2.2	<1.8		STRJ -WG4	
Maximum metal current		mA	2.16	1.56	1.2	0.6		STRJ -WG4	
DSM Category									
Signal Integrity	Crosstalk noise Required	Required parallel interconnect maximum allowable length which considers parasitic capacitance effect	mm	1.08	0.78	0.60	0.30	←(*a) Next Page	See
		Estimated parallel interconnect maximum allowable length which considers parasitic capacitance effect	mm	2.70	0.21	0.00	0.00	←	tab.2-1-4-2
	RC delay Required	Required interconnect maximum allowable length which considers resistance	mm	10	10	10	10	←(*b) Next Page	See
		Estimated interconnect maximum allowable length which considers resistance	mm	289	67	12	2	←	tab.2-1-4-3
	Inductance	Interconnect Inductance Effect				CP1 (*1)	CP2 (*2)		
	EMI Allowed	Allowable EMI by FCCclassB (at a distance of 3.0m )	uV/m	150	200	500	500	←(*c) Next Page	See
Estimated EMI by a chip (observation point =3.0m)		uV/m	11	22	43	43	←	tab.2-1-4-4	
Reliability	IR drop Required	Required maximum allowable number of FF which is driven by power line without failure due to IR Drop.		20	20	20	20	←(*d) Next Page	See
		Estimated maximum allowable number of FF which is driven by power line without failure due to IR Drop.		34	21	10	5	←	tab.2-1-4-5
	ElectroMigration	Number of Power Pads (High Performance)		342	472	800	1,066		See
		Number of Power Pads (Battery/Hand-Held)		6	9	16	16	←	tab.2-1-4-6
Number of Power Pads (Target of LP-SWG)			2	2	3	4			
Manufac ture	OPE	Optical Proximity Correction				CP	CP		

CP1(1st Crisis Point): Interconnect effects becomes critical in high speed blocks(1GHz).  
 CP2(2nd Crisis Point): Interconnect effects becomes major delay in high speed blocks(2GHz).

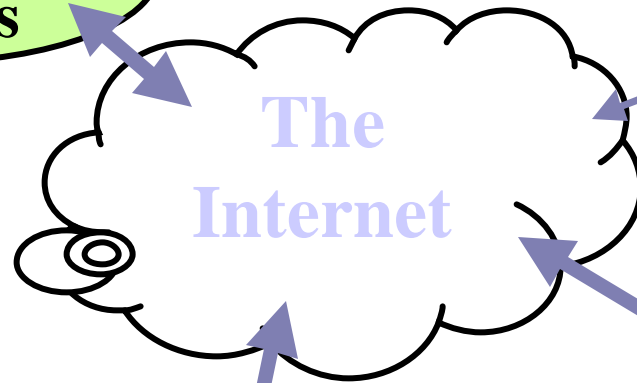
- Values in tables are not clear; where are values coming from?

→ Add remarks to key values

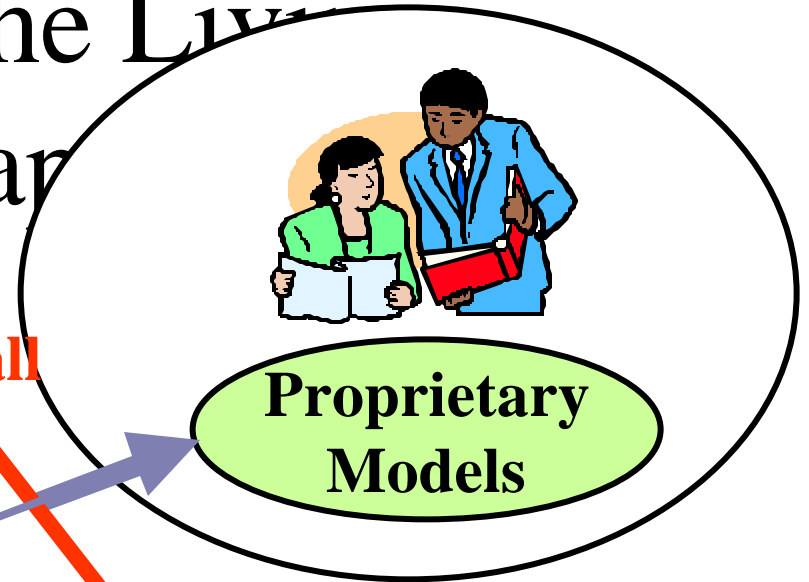
# The World of the Living Roadmap



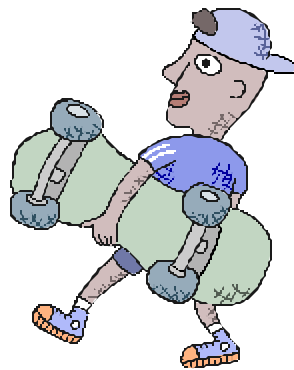
**Technology  
Models**



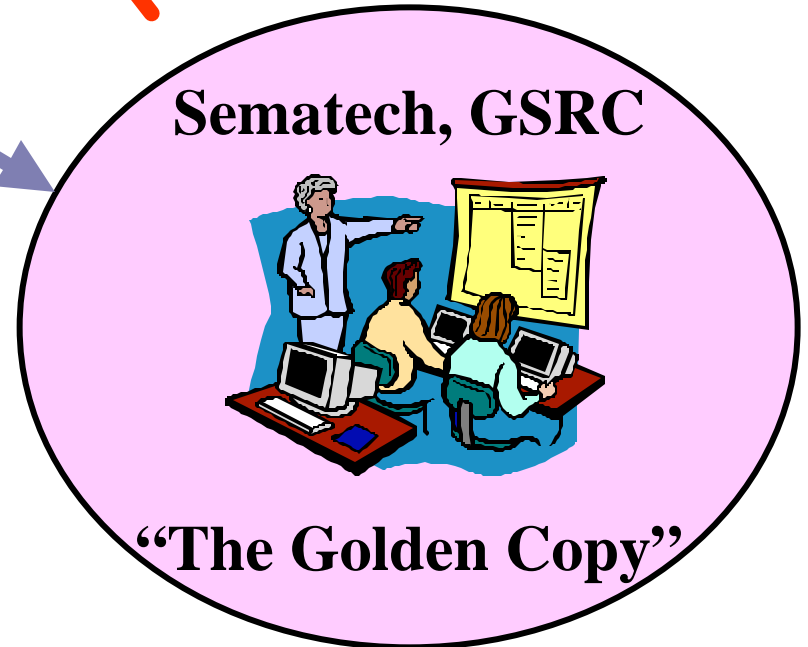
**Firewall**



**Proprietary  
Models**



**University  
Researchers**



**Sematech, GSRC**

**"The Golden Copy"**

**- Missing feedbacks from 4 regions**



**Make more active international communications**

This meeting: 4 of 5 regions present  
Europe and Korea work to establish regional  
committees to work on ITRS issues

**ITRS, meeting in Leuven**

## **Proposal or Concern on ITRS2000 and beyond**

- **Definition of scope for “Design”**
  - **Does it mainly address hardware implementation technologies ?**
  - **It needs to include system integration, software technologies and embedded blocks (RF, analog, MEMS,, )**
- **Need “Design technology nodes” in addition design technology turning-points, for example**
  - **IP design**
  - **DSM related technologies**
  - **Power supply scheme**

# Questions addressed in consultations with other TWGs

## Meeting with PIDs:

- Agreement to work together on numbers for power saving, gate leakage spec, benchmark circuits (analog and matching)

## Meeting with interconnect TWG:

- Agreement to cooperate on task force on parameter improvements for contact resistances (tungsten?), metal resistivities (copper?), and intermetal dielectric constants

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## **Questions addressed in consultations with other TWGs (cont'd)**

### **Meeting with Test TWG, Assembly and Packaging:**

- Design will review the frequency numbers in the tables based on inputs from Japanese roadmap



SOFT SHOULDER  
BLIND CURVES  
STEEP GRADE  
BIG TRUCKS  
GOOD LUCK!