Modeling and Simulation TWG

Norihiko Kotani, Mitsubishi

International TWG Members:

I. Bork, Infineon

N. Kotani, Mitsubishi

P. Leon, Intel

H. Ma, Episil

K. Nishi, Selete

H. Jaouen, STMicroelectronics

D. Wolleson, AMD

S.-C. Wong, Winbond

Modeling and Simulation TWG: Scope

Topical Area

- Equipment/Topography Modeling
- Lithography Modeling
- Front End Process Modeling
- Numerical Device Modeling
- Circuit Element Modeling
- Package Modeling
- Numerical Methods and Algorithms

Developer

- Universities
- Laboratories (Companies, Government)
- CAD Vendors

Strategy

Adequate research funds for universities and laboratories are indispensable because new modeling capability requires long-range research.

Key Messages

- High frequency circuit and interconnect models
- Models to reduce cross-die variation (equipment modeling, CMP)
- Model alternative lithography technologies
- Reliability models for circuit design and technology development
- Atomistic process modeling
- Goals for cost reduction due to TCAD

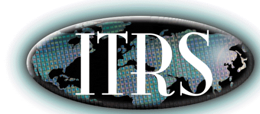
Difficult Challenges(≧100nm/Through 2005):

High frequency circuit modeling (>1GHz)

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Efficient simulation of full-chip interconnect delay
- Accurate 3-D interconnect model; inductance effects
- High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects

- Efficient, accurate interconnect modeling critical for future high speed circuits



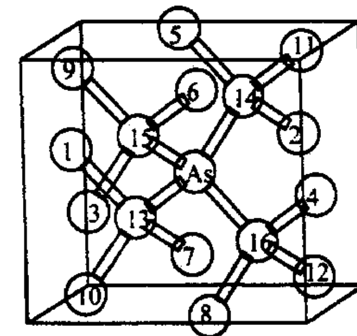
Difficult Challenges(≧100nm/Through 2005):

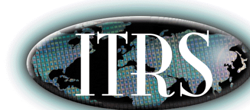
Modeling of ultra-shallow junctions

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge
- Interface effects on point defects and dopants
- Activation models (In, As, B); metastable states
- Implant damage, amorphization, re- crystallization

- Significant progress recently using <u>quantum calculations</u> for diffusion parameters
- <u>Interface</u> interactions dominate
  - ➢Shallow junctions: all dopants are next to surface
- <u>Activation</u> issues become important
  - ➢ Scaled devices need low resistivity source/drain





Difficult Challenges(≧100nm/Through 2005):

Model thin film and etch control across die/wafer

(Equipment/topography modeling)

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Reaction paths and rate constants
- Plasma models; linked equipment/feature models
- CMP (full wafer and die level)
- Pattern dependent effects (CMP)

- Future litho has <u>reduced depth of focus</u>, increasingly tight cross-die layer uniformity requirements
- <u>Within-die variation</u> becoming key performance limiter; reduction is a source of performance gain
- <u>300mm wafer</u> transition imminent

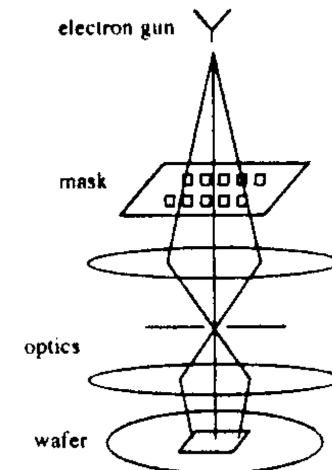
Difficult Challenges(≧100nm/Through 2005):

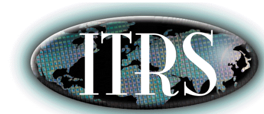
Model alternative lithography technologies

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Resolution enhancement effects and mask synthesis (e.g., OPC, PSM)
- Predictive resist models
- 248 vs 193 vs157 evaluation and tradeoffs
- Next-generation lithograph SCALPEL s

- Near term: resolution enhancement techniques, wavelength tradeoffs;
- Near term: layout compensation (e.g. OPC)
- Long term: early evaluation of competing Next Generation Litho approaches





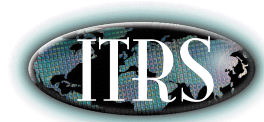
Difficult Challenges(≧100nm/Through 2005):

Reliability models for circuit design and technology development

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Circuit and device level transistor reliability: oxide TDDB, SER, hot carrier, electromigration
- NVM reliability
- ESD, latchup

- <u>Device level</u>: need predictive models for transistor reliability issues
- <u>Circuit level</u>: empirical models to guard-band designs



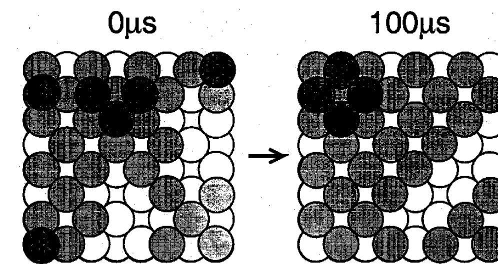
Difficult Challenges(<100nm/Beyond 2005):

Atomistic process modeling

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Develop models to model processing steps at the atomic scale with atomic scale accuracy

- Whatever direction technology takes, manipulation of atomic layer dimensions needed near end of the roadmap.
- Development of <u>theoretical, simulation and instrumental infrastructure</u> should start now



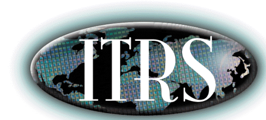
Cu diffusion (A. Voter, LANL)

Technology Requirements:

Cost Reduction

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
OVERALL TECHNOLOGY COST REDUCTION TARGET (DUE TO TCAD)	**20%**			**25%**			**35%**	

- Goal of TCAD Technology Requirements: overall development cost reduction
- Successful application to family processes
- For devices of new technology node,
  more efforts needed for predictive modeling
- Still at its infancy level for back end process modeling

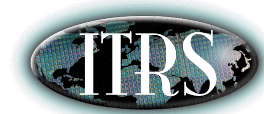


Technology Requirements:

Front End Process Modeling (Accuracy)

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
Vertical and lateral junction depth simulation accuracy	18 NM (10%)			13 NM (10%)			10 NM (10%)	
Total source/drain series resistance (accuracy)	20%			20%			20%	
Long-channel V_t (accuracy)	5% (75–90mV)			4% (48–60mV)			3% (27–36mV)	

- Thermal process of lower temperature and shorter time
- Classical but still important issues in TCAD
- Improved evaluation method are required, especially for dopant profiles
- Effective use achieved after proper calibration



Technology Requirements:

Front End Process Modeling (Capabilities)

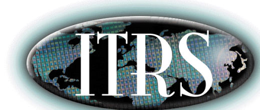
Short Term

YEAR OF INTRODUCTION	1999 180 NM	2000	2001	2002 130 NM	2003	2004	2005 100 NM
Gate Stack: evaluate materials		Model alternate dielectrics			Model metal vs. poly gate		
Diffusion and activation coefficients		Kinetics of diffusion and activation			Interface interactions with point defects and dopants		
Stress/extended defects		Front end stress model			Extended defects and disloactions		

Long Term

YEAR TECHNOLOGY NODE	2008 70 NM	2011 50 NM	2014 35 NM
Advanced process models	Metastable activation (>solid solubility)	Alternative materials (such as SiGe)	Atomistic process model
Advanced doping models	Solid source		

- **Atomistic-level models required for new gate materials**
- **Point-defects issues still important**
- **Extended defects to be modeled properly in view of mechanical stresses and generation /recombination of point defects**



Technology Requirements:

Device Modeling(Accuracy)

YEAR TECHNOLOGY NODE	*1999* *180* nm	*2000*	*2001*	*2002* *130* nm	*2003*	*2004*	*2005* *100* nm	*Driver*
Accuracy of f_t at given f_t (% of maximum chip frequency)	**10%**			**10%**			**10%**	
Gate leakage current accuracy(%) (decreases due to increase of I_g/I_d)	**100%**			**70%**			**40%**	
I_{off} accuracy	**100%**			**70%**			**40%**	
V_t rolloff accuracy (mV)	**25mV**			**20mV**			**20mV**	

- Increasing importance of leakage/off current modeling and cut-off frequency modeling
- Ever-lasting importance of Vt rolloff modeling

Technology Requirements:

Device Modeling (Capabilities)

Short Term

YEAR OF INTRODUCTION	1999 180 NM	2000	2001	2002 130 NM	2003	2004	2005 100 NM
Gate stack models		Gate current tunneling models			Full quantum gate stack models		
Reliability models		Transistor reliability models (gate oxide)			Interconnect reliability models (electromig., stress)		
Noise/variation		Dopant fluctuation			Noise models		

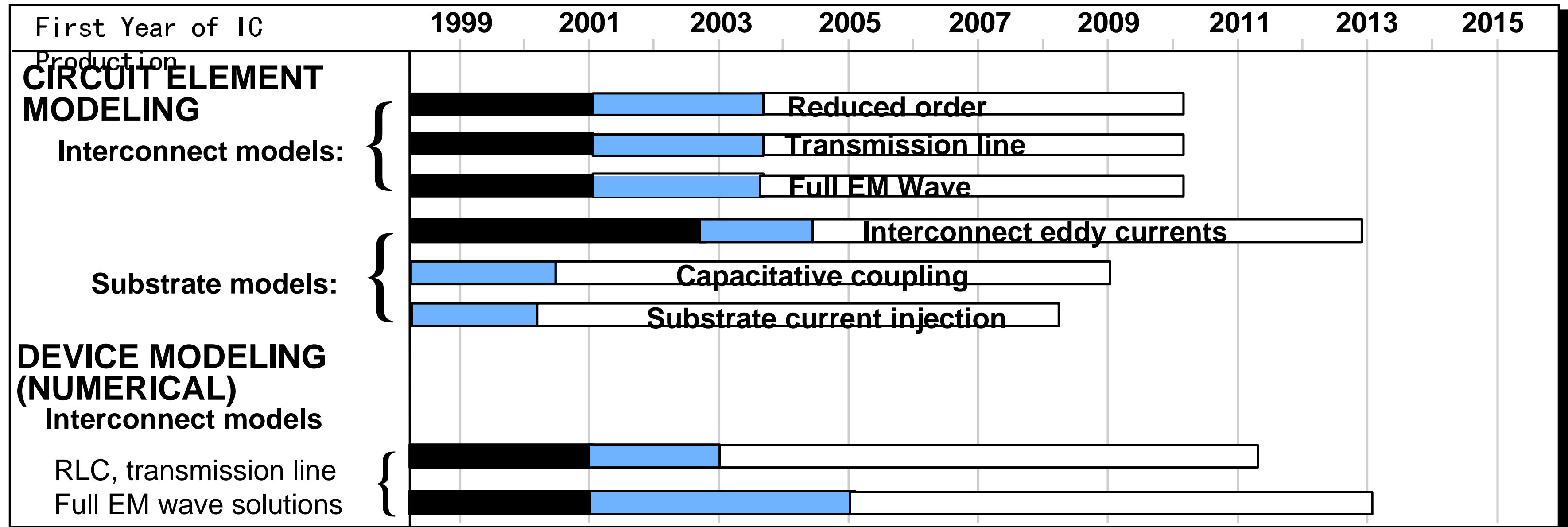
Long Term

YEAR TECHNOLOGY NODE	2008 70 NM	2011 50 NM	2014 35 NM
Alternative device models	2D quantum models for MOS	Single electron transistor	Quantum effect devices

- **Quantum models needed for new gate stack materials**
- **Predictive models needed for reliability issues: gate oxide (thinner oxide, new gate materials…), interconnects (electro/stress migration…)**
- **Smaller devices more susceptible to EMS**

Potential Solutions:

Interconnect models

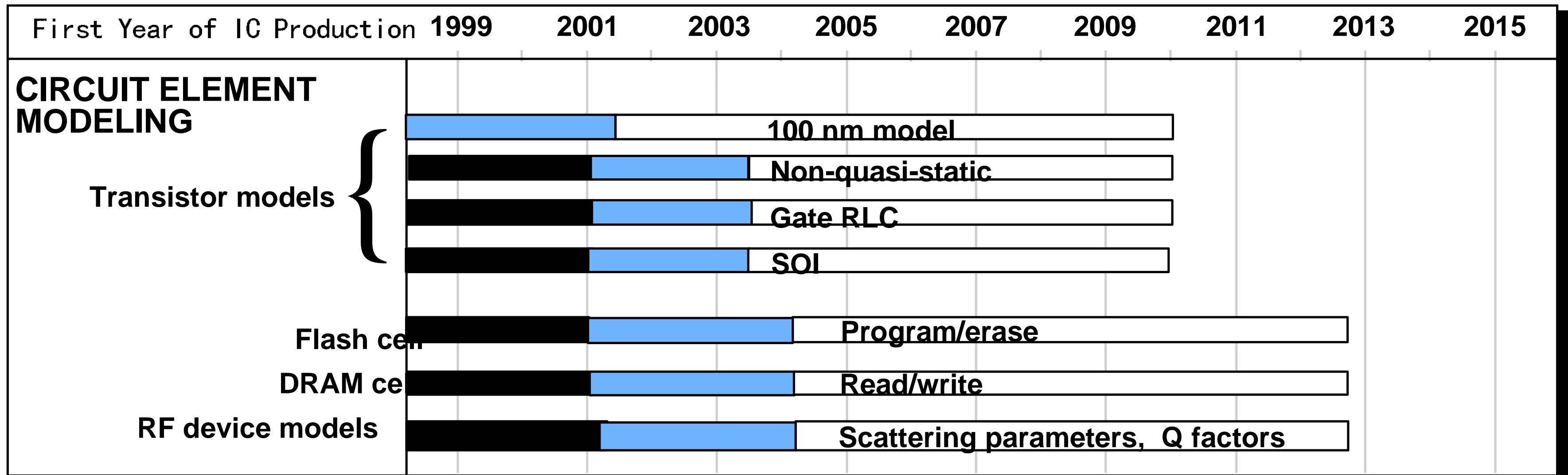


More accurate interconnect parasitic models are critical for high frequency design:

- **Improved analytic capacitance models**
  - **2D and 3D**
  - **cross-talk**
- **On-chip inductance modeling**
  - **substrate models**
- **Transmission line; full EM wave solvers**

Potential Solutions:

Circuit models: Transistor, Device



- 100nm transistor model
- SOI models (floating body effect)
- Flash (program/erase)
- DRAM (read/write)
- RF device models:
  - active devices, passive devices

Potential Solutions:

Reliability modeling

First Year of IC Production	1999	2001	2003	2005	2007	2009	2011	2013	2015
Reliability modeling:									
Oxide TDDB Hot carrier Electromigration ESD, latchup	**Oxide tunneling** **Monte Carlo, quantum effect** **Metal reliability**								

- Gate dielectric degradation (circuit, numerical)
- Electromigration (circuit)
- ESD, Latchup (circuit, numerical)
- SER (circuit, numerical)
  - DRAM and logic
  - alpha and neutrons

Summary

- **Next two generations (130nm, 100nm) provide many modeling challenges:**
  - High frequency circuit and interconnect models (RLC, transistor)
  - Model cross-die variation due to etch, thin film (e.g., CMP, equipment modeling)
  - Model lithography technology tradeoffs (resolution enhancement techniques, wavelength, OPC, PSM)
  - Goals for cost reduction due to TCAD
- **Beyond 100nm, basic theoretical research needed:**
  - Gate stack process and electrical model (atomic level)
  - Limits of MOS devices, innovative MOS devices and beyond
- **Adequate research funds for universities and laboratories**