

# Front End Process TWG Report

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## International TWG Members:

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Bernd Vollmer, Infineon

J. Wortman, NCSU

H.H. Tsai, Winbond

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International Technology Roadmap for Semiconductors  
Tokyo, Japan; November 1999



# STRJ FEP TWG Members

**Leader:** S.Kawamura(Fujitsu)

**Sub-leader:** M.Niwa(Matsushita)

**Members:** K.Ikeda(NEC)

M.Matsumoto(Oki)

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S.Ikeda(Hitachi)

M.Kubota(Sony)

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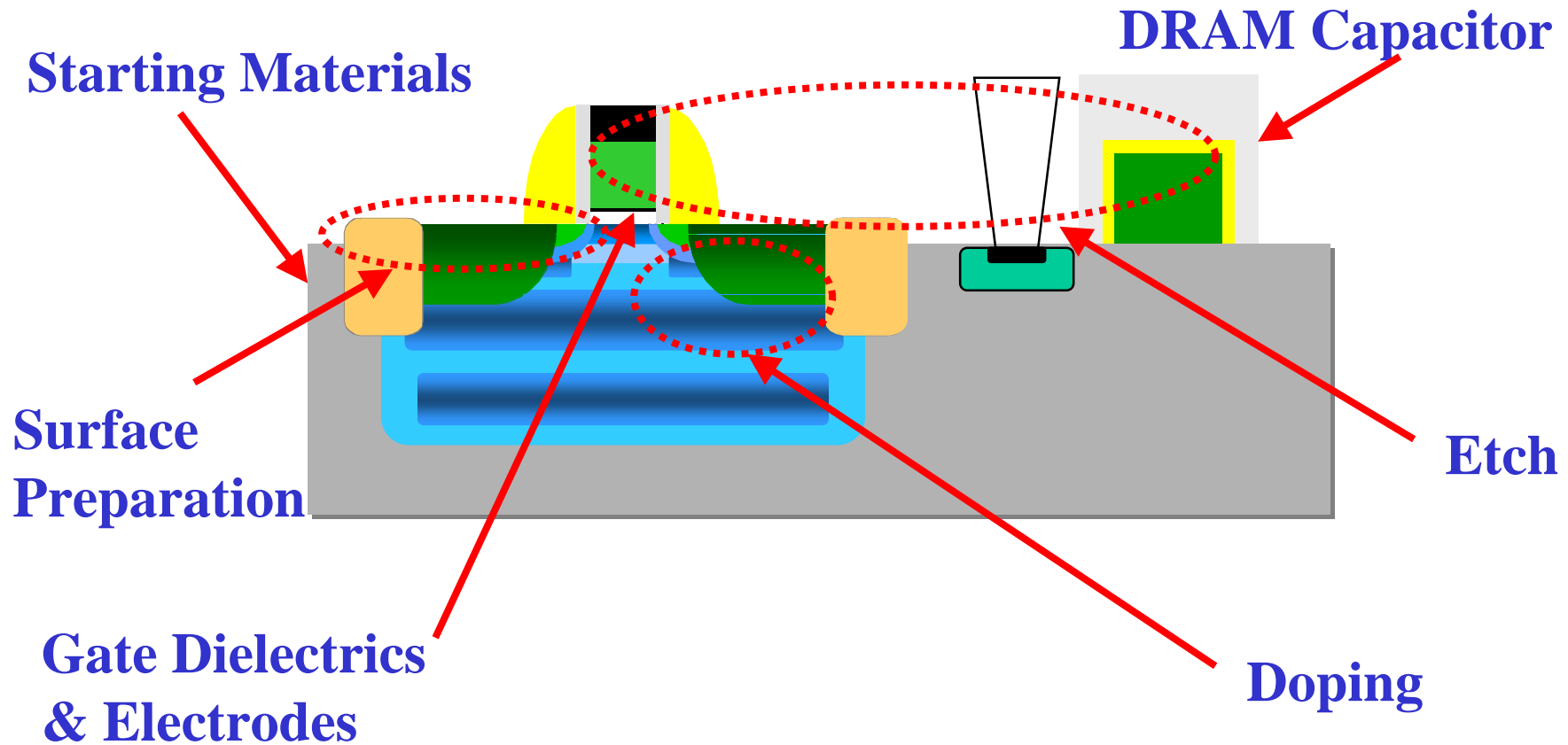
Y.Kunii(KE)



# Scope of FEP TWG Activities

- Focus on requirements for high performance transistors & storage capacitors for logic and memory products
- Purpose is to define comprehensive, integrated solutions needs for the key technology areas in the front-end-of-line (FEOL) wafer fabrication processing of LSIs
- Covers starting Si material through contact silicidation & storage capacitor formation processes

# *FEP Roadmap Scope*



International Technology Roadmap for Semiconductors  
Tokyo, Japan; November 1999



# Thrusts & Sub-TWG Organization

- **Starting Materials**
- **Surface Preparation**
- **Etch**
- **Doping**
- **Thermal/Thin Films**
- **Memory Capacitor Films**



# Sub-TWG Tasks

- **Using an evolutionary approach, address the following issues:**
  - Establish evolutionary technical requirements through model-based or physical-based extrapolation
  - Identify where barriers exist to evolutionary technology extensions
  - Identify if work is ongoing to address these barriers (color code yellow)
  - Identify if there is no known solution to these barriers (color code red)
  - Identify those known potential solutions which are in R&D or pilot production
  - Prepare roadmap documentation
  - Collaborate with other sub-TWG's re selection of FEP Difficult Challenges

# Sub-TWG Roadmap Documentation

- **Color-coded Technical Requirements Tables**
  - Yellow means barriers exists but are being addressed in R&D
  - Red means barriers exist and no known solutions have been identified
- **Color-coded Potential Solutions Figures**
  - Black identifies research is required
  - Blue identifies development is underway
  - White identifies work is in pre-production
- **Table of Difficult Challenges**
- **Text**
- **Crosscut Issues**



# TWG Membership Affiliations

- **Universities**
- **Government Agencies**
- **Semiconductor Manufacturers**
- **Semiconductor Equipment Manufacturers**
- **Materials Suppliers**
- **Consultants**



# Starting Materials

## Basic Concept ( Model Based Analysis) Yield-Defect Density Model

$$\text{Yield } Y = \exp(-\text{Defect Density} \times \text{Kill Ratio } R \times \text{Critical Area}) = 0.99$$

Table's Requirement

<b>Critical Area</b>	DRAM ; Bits/Chip $\times (CD)^2 \times (W/L) \times (\text{Cell Area Factor } A)$ MPU ; Tr.s/Chip $\times (CD)^2 \times (W/L) \times (\delta)$
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*new*

Kill Ratio R ; depend on defects type

Bits or Tr.s/Chip; '97 ES

'99 **Production**

Particle & Metal ;  $\times 2$ (assumption:min. cleaning efficiency is 50%)

# Difference ;1999 vs. 1997

1999

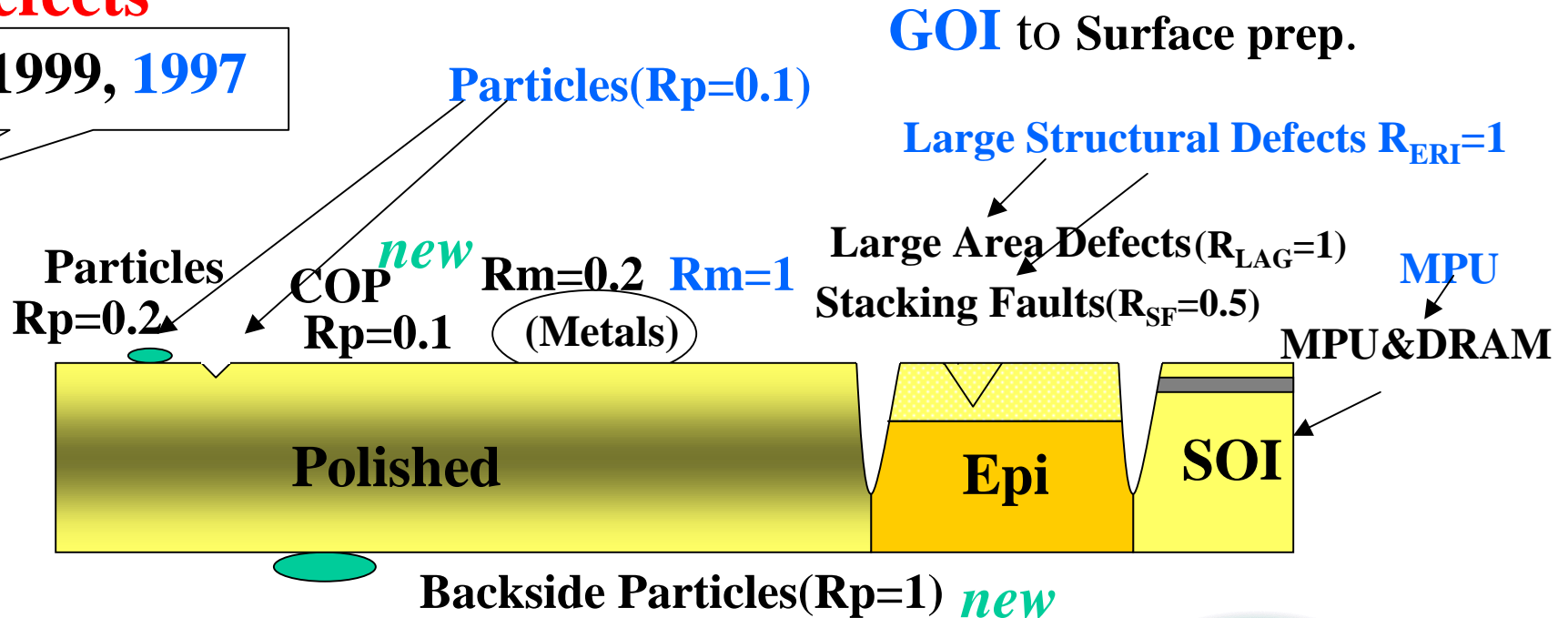
1997

## General Characteristics

Wafer Size	2000 / 2014	1999 / 2009
300/450 <sub>(node)</sub>	(130nm) (35nm)	(180nm) (70nm)
Edge Exclusion	2000(1mm)	1999(2mm)→2006(1mm)
Site Flatness	site size 25 × 32mm <sup>2</sup> constant	increase depending on node

## Defects

1999, 1997



# *Surface Preparation Technology Requirements*

**1 Adjusted to new chip size model : Critical Area, GOI D0, Light scatter of front side & Back side, Critical surface metals, Mobil ions**

**2 New Requirements : Light scatter for back side, Mobil ions, Surface roughness, Water marks, Corrosion resistance**

**3 Back side particles : Size :  $D=(2/0.6)*CD-T$  (T=100nm)**

**4 Particle size of BEOL : Equal to CD (1997 Road Map: CD/2)**

**5 Organics/polymers, Oxide residue :**

	<b>1999(180nm)</b>	<b>2005(100nm)</b>
<b>Organics/polymers</b>	<b><math>7.3 \times 10^{13}</math> (10% C-atoms cover on Si)</b>	<b><math>4.1 \times 10^{13}</math></b>
<b>Oxide residue</b>	<b><math>1 \times 10^{14}</math> (O-conc. of HF last process)</b>	<b><math>1 \times 10^{12}</math> (For LowTemp EPI)</b>

# Surface Preparation Difficult Challenges and Potential Solutions

Before 100nm

100nm and after

Chemical and DI-water usage reduction

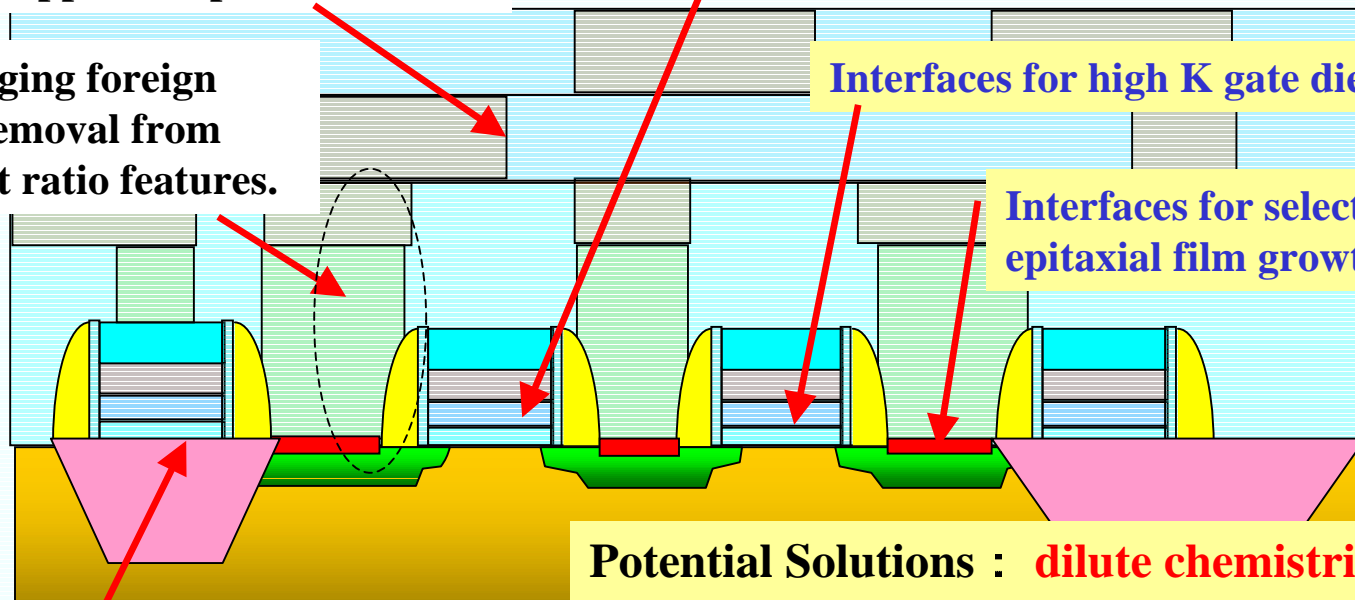
High K and metal gate cleans.

Low K & copper compatible cleans.

Non-damaging foreign material removal from high aspect ratio features.

Interfaces for high K gate dielectrics.

Interfaces for selective epitaxial film growth.

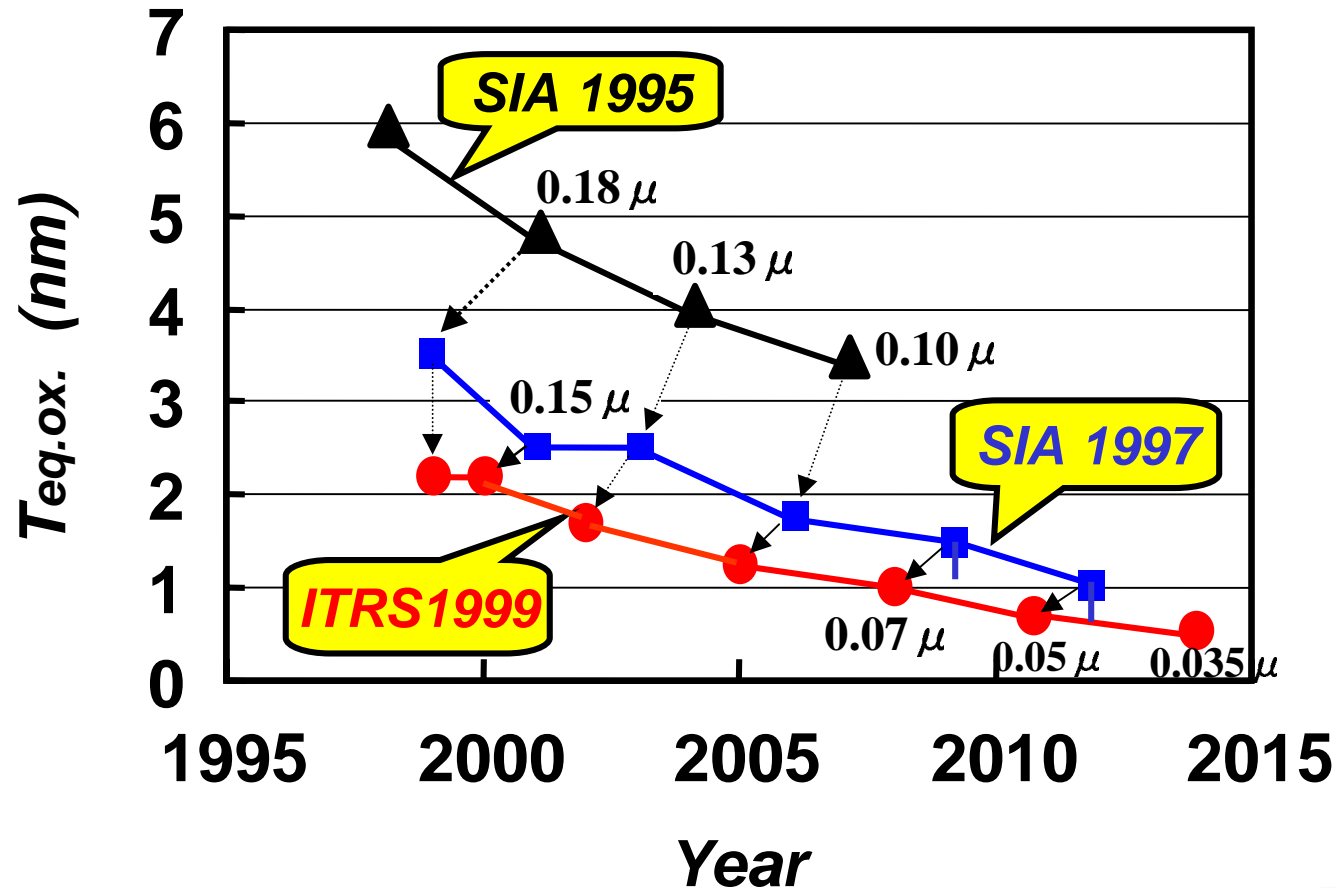


Interfacial oxide thickness control

Potential Solutions : dilute chemistries, alternative chemistries, dry cleaning, cryogenic aerosol, laser cleaning

# Gate Dielectrics & Electrodes

**Drastic Reduction of the *effective oxide thickness* !**



# Grand Challenge

## Moving beyond the Silicon Dioxide era

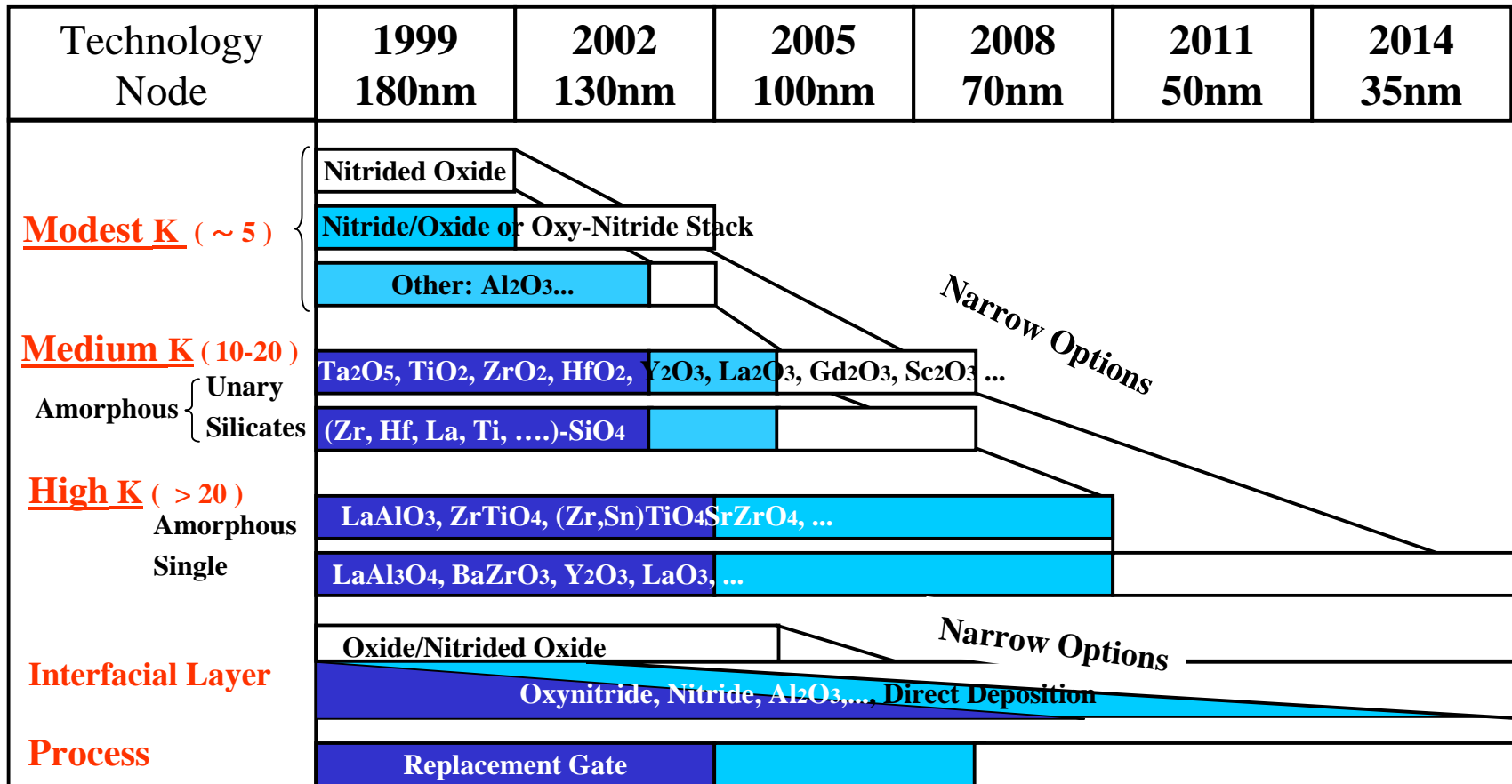
- **Drastic Reduction of the effective oxide thickness**
- **Achievement of acceptably low electrical leakage**
- **Measurement of ultra-thin physical thickness**

Technology Node		1999 180nm	2002 130nm	2005 100nm	2008 70nm	2011 50nm	2014 35nm
Equivalent physical oxide thickness Teq.ox (nm)	SIA 97	3 - 4 (1999)	2 - 3 (2003)	1.5 - 2.0 (2006)	< 1.5 (2009)	< 1.0 (2012)	
	ITRS 99	1.9 - 2.5	1.5 - 1.9	1.0 - 1.5	0.8 - 1.2	0.6 - 0.8	0.5 - 0.6
Gate dielectric leakage@100C (nA/um) H.P.		5	10	20	40	80	160
Gate dielectric leakage@100C (pA/um) L.P.		5	10	20	40	80	160

H.P. : High Performance, L.P. : Low Power

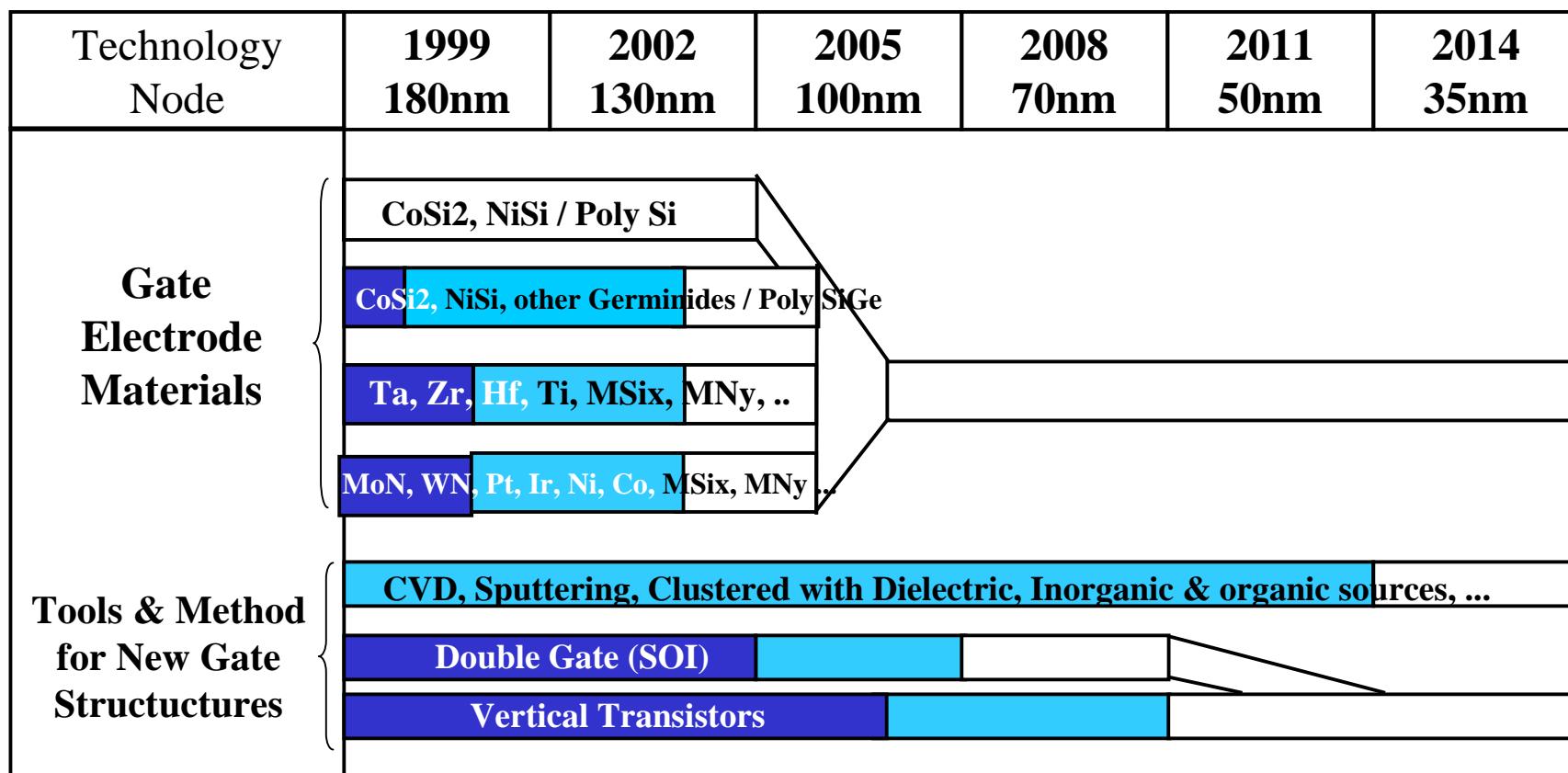
# Moving beyond the $\text{SiO}_2/\text{Poly Si}$ gate

~ *New materials for the Gate Dielectrics* ~

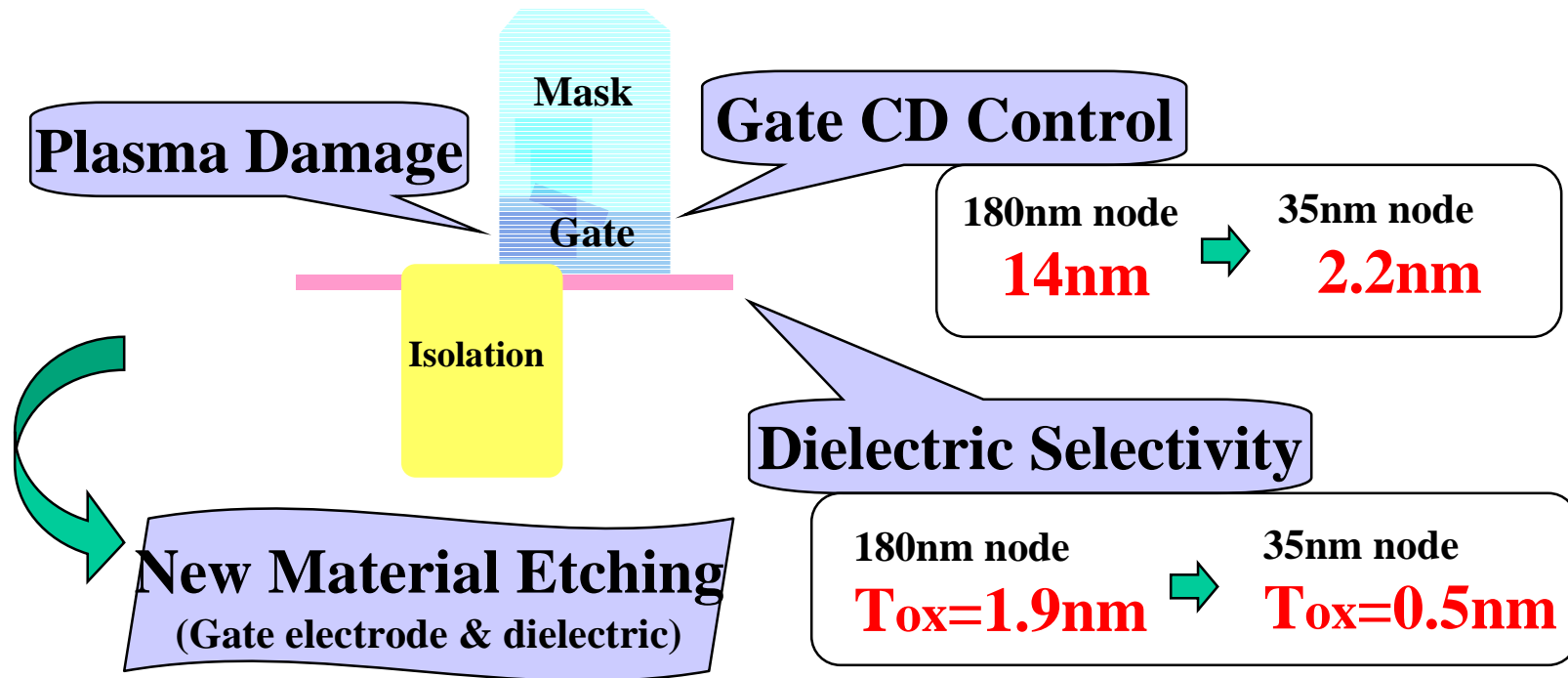


# Moving beyond the SiO<sub>2</sub>/Poly Si gate

~ *New materials for the Gate Electrode* ~



# Etch Process



**Potential Solutions** : New Etch Chemistries (High Density Plasma).  
Neutral Stream or CDE\* (Future Etches).

\* Chemical Downstream Etching

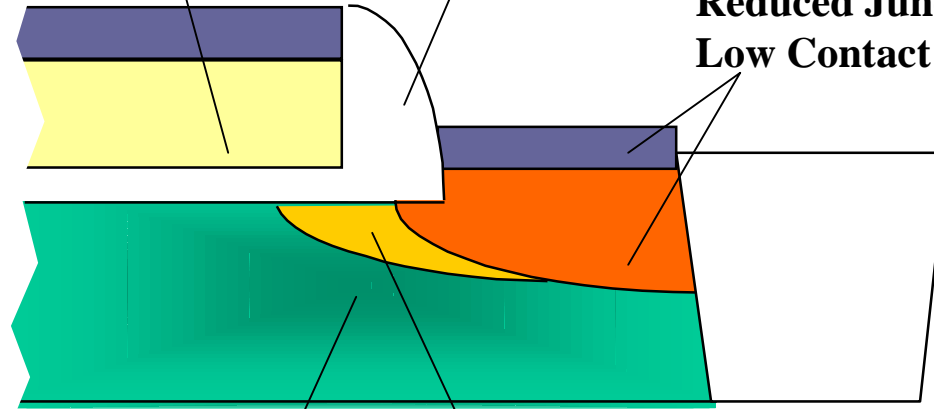
# ***DOPING TECHNOLOGY***

## **REQUIREMENTS**

**Reduced Gate Depletion  
High Level Gate Doping  
Gate Insulator Integrity**

**Low Parasitic Capacitance**

**Low Resistivity Diffusion  
Reduced Junction Leakage  
Low Contact Resistivity**



**Optimized HALO Doping  
Avoiding Short Channel Effects**

**Shallow / Low resistance Extension  
Lateral Abruptness  
Parasitic Resistance < 10% of R<sub>device</sub>**

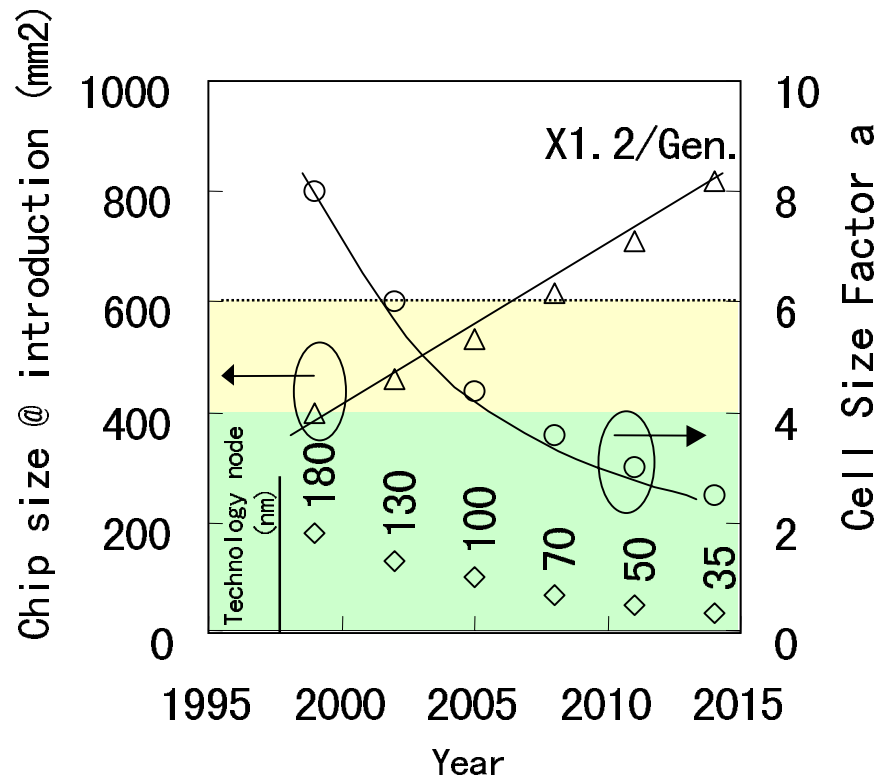
## *Near-Term (~2005) Difficult Challenges and Potential Solutions*

- Ultra Shallow junction using standard processing.
- Shallow junction depth / low parasitic resistance.
- High gate doping level avoiding gate depletion.
- Reduced Silicide/Diffusion contact resistivity.
- Substrate doping profile for short channel effect immunity and acceptable off current.
- Ultra low energy ion implantation; <1keV.
- Highly ramp-up/down RTA.
- Managing transient enhanced diffusion(TED).
- Super steep retrograded channel profile / Optimized HALO doping with angled ion implantation.
- Heavy atom ion implantation.

## *Long-Term (2005 ~) Difficult Challenges and Potential Solutions*

- Ultra Shallow junction with precise process control and structural approach or new materials.
- Compatible with High-k dielectrics and metal gate materials.
- Extreme abruptness in extension / contact junctions.
- Substitutive structure for self-aligned silicide.
- Extreme abruptness of channel doping profile.
- Laser anneal.
- Plasma doping or other gas / solid phase doping.
- Elevated(Raised) source and drain using selective epitaxy.
- Self-aligned silicide with sacrificial layer / selective deposition of silicide or metal for contact diffusion.
- Abruptly doped Epi-channel.

# *DRAM cell size: Accelerated scaling down*



$$\text{Cell size} = a * F^2$$

a : Cell Size Factor

a = ~8 Folded bitline cell

a = ~6 Open bitline cell

..... smallest cell size of STC .....

a = ~4 Cross point cell

..... smallest cell size of TRC .....

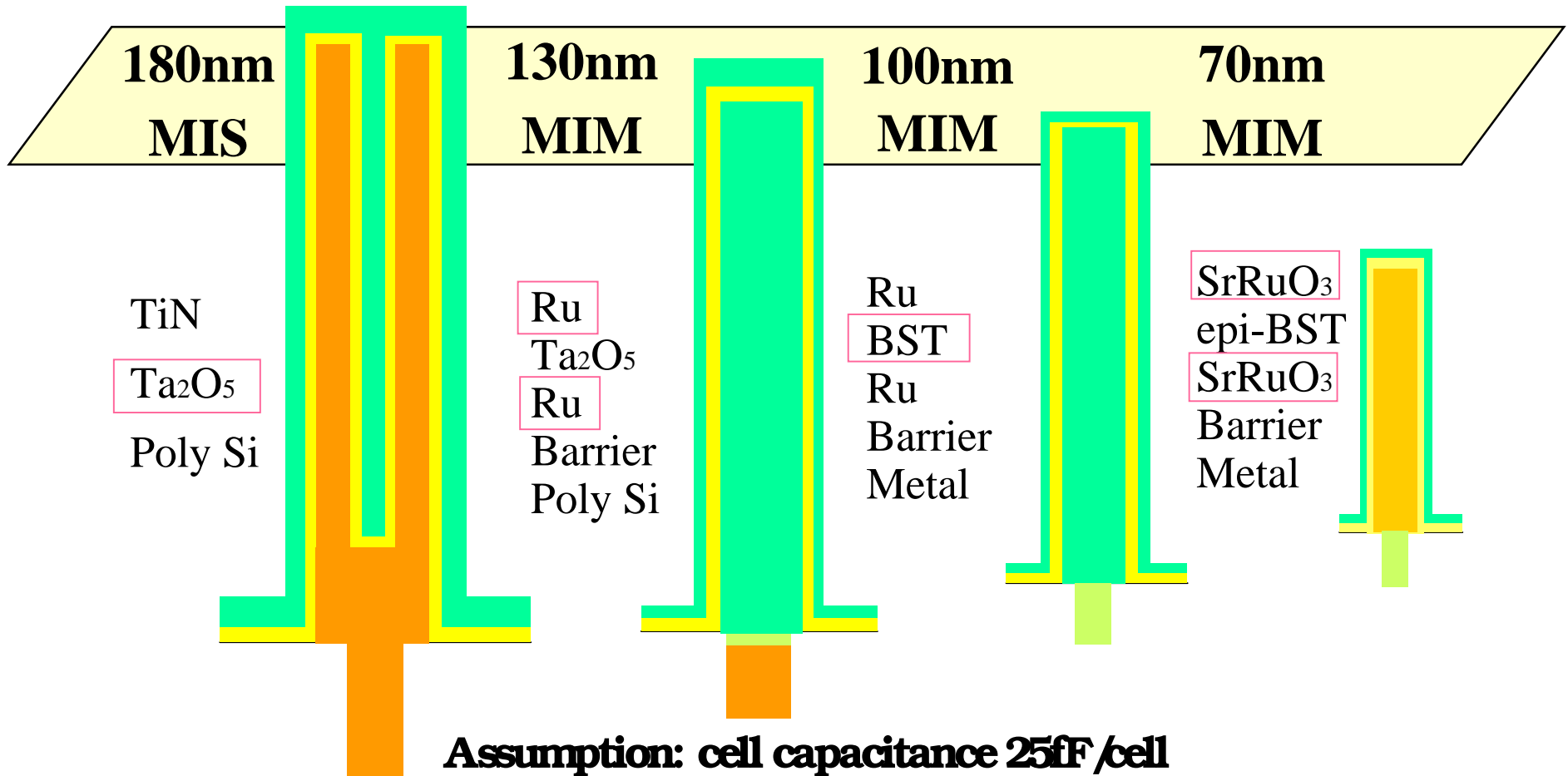
a < 4 Multi-valued cell

STC : Stacked capacitor

TRC : Trench capacitor

The trend of DRAM chip size and cell size factor

# Possible capacitor structure and materials



# *DRAM Capacitor Difficult Challenges*

- High-k capacitor dielectrics
- Metal electrode for MIM
- Etching of SN and electrode
- Etching of high aspect ratio contact hole
- Reducing film deposition /anneal temperature

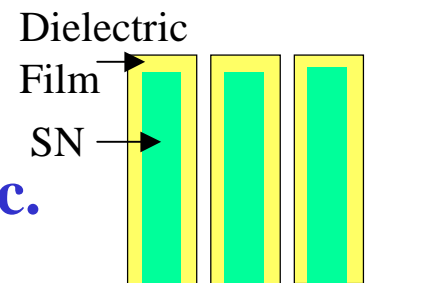
## *Beyond the 100nm node (~8Gb DRAM)*

- Cell size  $< 6F^2$  (the smallest cell size with open-bit line architecture)
- High aspect ratio storage node (for Upper Electrode depo.)  $> \sim 16$

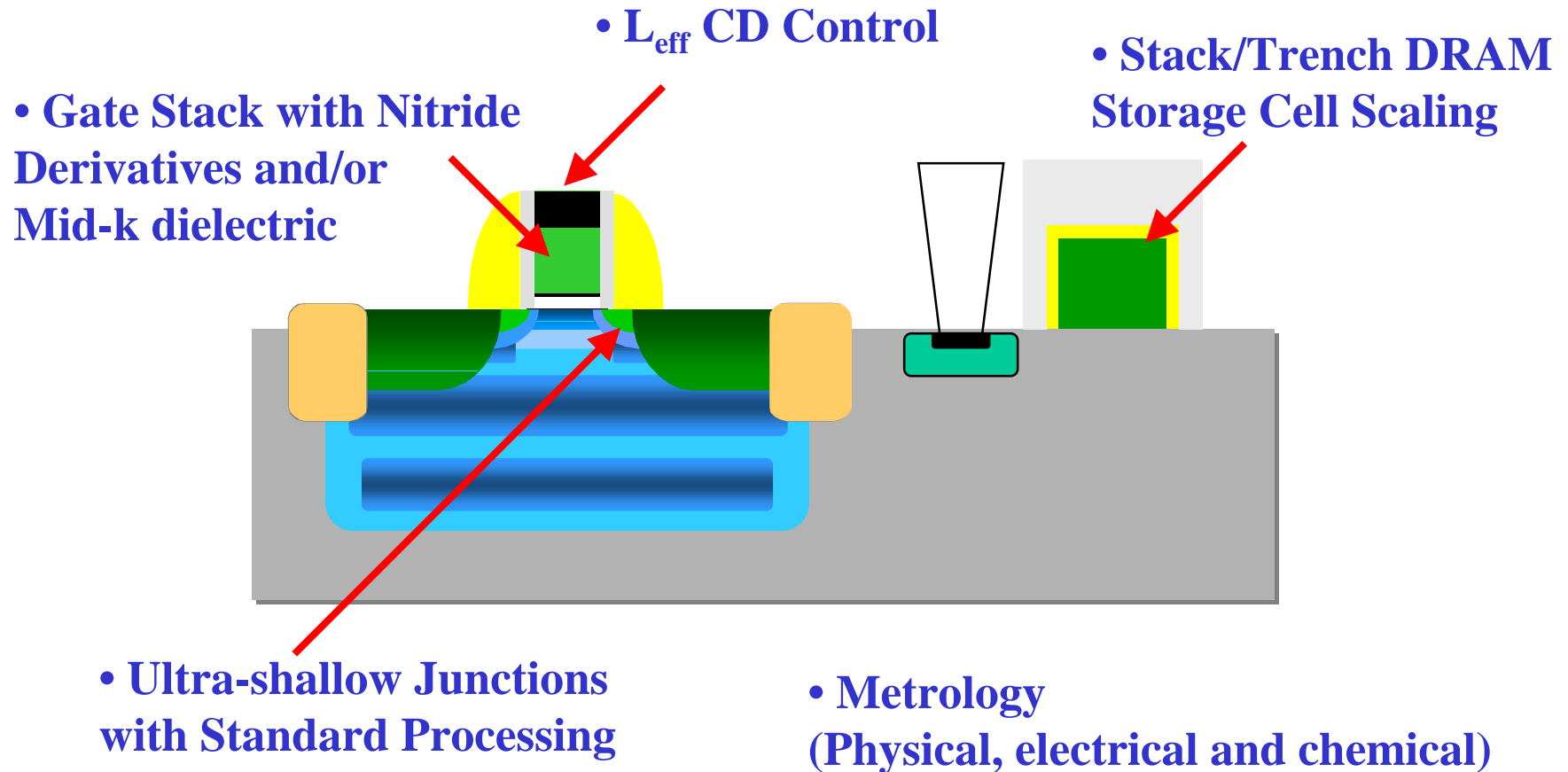
New cell architecture required

---- cross-point, multi-valued cell etc.

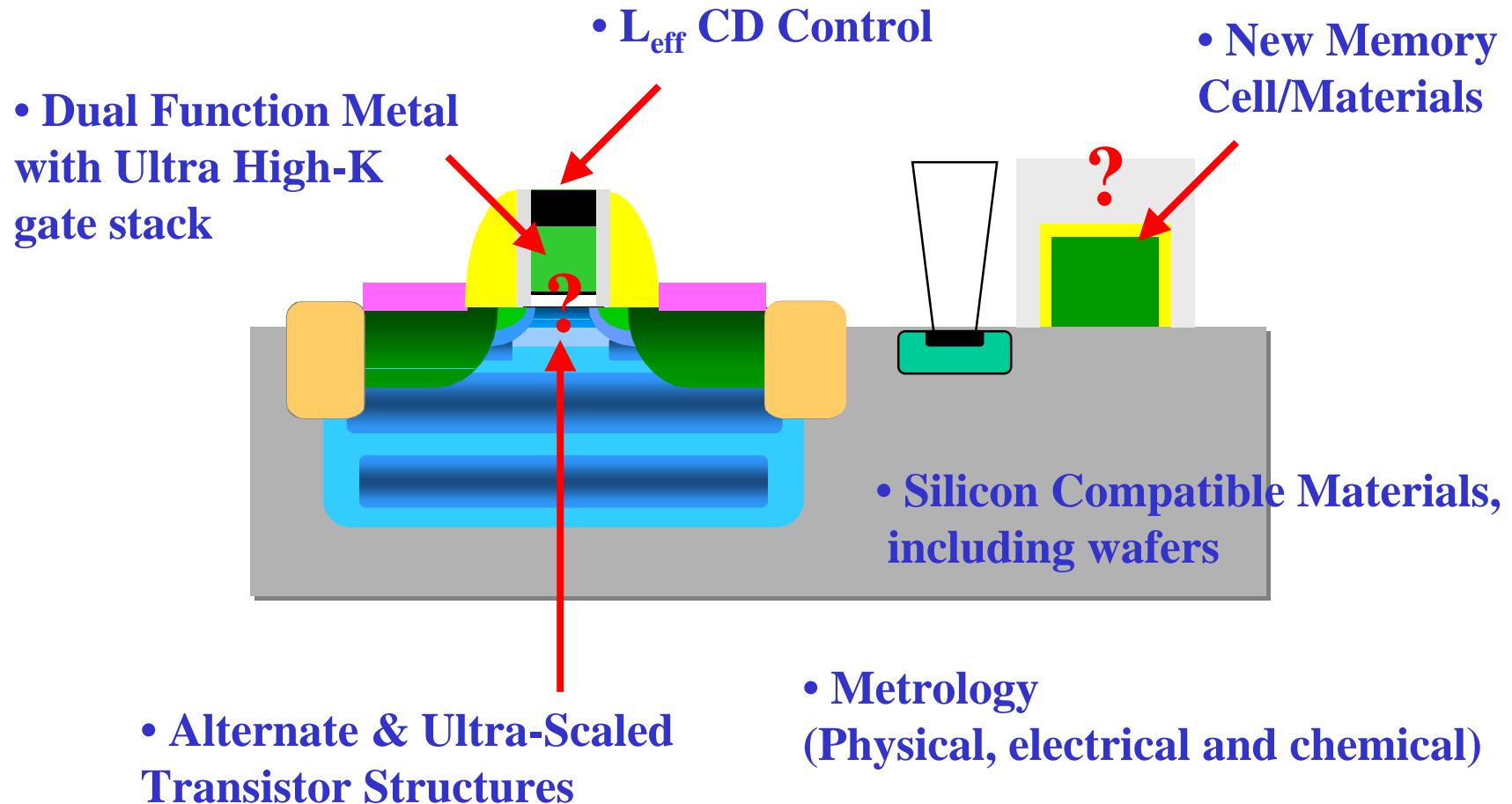
New concept memory cell: gain cell, FeRAM, etc.



# *FEP Difficult Challenges before 2005*



# *FEP Difficult Challenges beyond 2005*



# Summary & Messages

- **FEP/ITRS99 has identified the end of CMOS unless new materials and devices are introduced on an aggressive time scale!!!**
- **High-risk approaches needs to be combined with evolutionary approaches and new knowledge to meet the challenge**
- **This will require a partnership between the industry, universities and research institutes on an international scale**

