

# **International Technology Roadmap for Semiconductors (ITRS 1999)**

## **Assembly & Packaging**

**International Technical Working Group**

**Co-Chair:**

**Bob Werner & Chi Shih Chang**

**SEMATECH Inc., Austin, TX U.S.A.**

**International Technology Roadmap for Semiconductors**

**Tokyo, Japan; November 1999**



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# Introduction and Difficult Challenges

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# 1999 Overview

## UPDATED

- Market sectors aligned with NEMI
- Expanded discussion on wafer level packaging
- Expanded reliability section
- Thermal management
- High density substrates
- RF and mixed signal packaging
- Multi-chip packaging/modules

## ADDED

- System on chip (SOC) & System in a Package (SiP)
- Electro-migration limits of eutectic flip chip bumps

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# Challenges

- Major categories maintained
- Additions
  - Packaging of Cu/low  $\kappa$  IC
  - Thermal
  - Design for high density digital/mixed signal packaging
  - Manufacturability/reliability of large body packages

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*Table 58 Assembly & Packaging Difficult Challenges*

<p><b><i>FIVE DIFFICULT CHALLENGES</i></b>  <i>≥ 100 nm / THROUGH 2005</i></p>	<p><b><i>SUMMARY OF ISSUES</i></b></p>
<p>Improved organic substrates for high I/O area array flip chip</p>	<p><math>T_{\text{eg}}</math> compatible with Pb free solder processing  <math>\epsilon_r</math> approaching 2.0                      Improved area array escape wireability at low cost                      Lower CTE* approaching 6.0 ppm/°C                      Low moisture absorption                      High density substrate test</p>
<p>Improved underfills for high I/O area array flip chip                      Reliability limits of flip chip on organic substrates</p>	<p>Improved manufacturability (fast dispense/cure), better interface adhesion, lower moisture absorption, flow for dense bump pitch                      Reliability up to 170°C for automotive                      Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump**)</p>

System reliability impact of Cu/low $\kappa$ on packaging	Bump and underfill technology to assure low $\kappa$ dielectric integrity Mechanical strength of dielectrics Interfacial adhesion
Cost effective cooling for cost-performance and high- performance sectors	Meeting 40°C above ambient temperature Localized on-chip power density

\* *CTE*—*coefficient of thermal expansion*

\*\* *UBM*—*under bump metallurgy*

† *EMI*—*electromagnetic interference*

‡ *EDA*—*electronic design automation*

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<b><i>DIFFICULT CHALLENGES</i></b> <i>&lt; 100 nm / BEYOND 2005</i>	
Close the gap between the substrate technology and the chip	Low-loss, low $\epsilon_r$ materials Cost/unit area constant (cost/layer decreasing) Interconnect density scaled to silicon System level solution that optimizes reliability and cost
“System level” view of integrated chip, package, and substrate needs	Commercial EDA supplier support
Ultra high frequency design for high density digital and mixed-signal packaging	Efficient design and simulation tools Integrated analog to digital design tools
Manufacturability and reliability of large body packages	Substrate flatness Co-planarity of chip-to-package and package-to-board

\* *CTE*—coefficient of thermal expansion

\*\* *UBM*—under bump metallurgy

† *EMI*—electromagnetic interference

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# Assembly & Packaging Technology Requirements

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# Requirements

- Cost
  - Widespread use of PBGA creates cost pressure on QFP & CBGA
  - 20-30% reduction
- Chip size
  - High performance, Cost performance, and Memory reduced substantially
- Increased chip to board frequency
  - Realization of PC133 BUS
- Moderate change to pin count
- Removed pad count
  - Large power/ground connections available with area array
- Overall package profile replaces package thickness

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# Table 59A/B. Technology Requirements

<i>Year of First Product Shipment Technology Generation</i>	<i>1999</i> <i>180nm</i>	<i>2000</i>	<i>2001</i>	<i>2002</i> <i>130nm</i>	<i>2003</i>	<i>2004</i>	<i>2005</i> <i>100nm</i>	<i>2008</i> <i>70nm</i>	<i>2011</i> <i>50nm</i>	<i>2014</i> <i>35nm</i>
<b>Cost (Cents/Pin)</b>										
Low cost	0.40–0.90	0.38–0.86	0.36–0.81	0.34–0.77	0.33–0.73	0.31–0.70	0.29–0.66	0.25–0.57	0.22–0.49	0.19–0.42
Hand-held	0.50–1.30	0.48–1.24	0.45–1.17	0.43–1.11	0.41–1.06	0.39–1.01	0.37–0.96	0.32–0.82	0.27–0.70	0.23–0.60
Cost-performance	0.90–1.90	0.86–1.81	0.81–1.71	0.77–1.63	0.73–1.55	0.70–1.47	0.66–1.40	0.57–1.20	0.49–1.03	0.42–0.88
High-performance	3.10	2.95	2.80	2.66	2.52	2.40	2.28	1.95	1.68	1.44
Harsh	0.50–1.00	0.48–0.95	0.45–0.90	0.43–0.86	0.41–0.81	0.39–0.77	0.37–0.74	0.32–0.63	0.27–0.54	0.23–0.46
Memory	0.40–1.90	0.38–1.71	0.36–1.54	0.34–1.39	0.33–1.25	0.31–1.12	0.29–1.01	0.25–0.74	0.22–0.54	0.19–0.39
<b>Chip Size (mm<sup>2</sup>)</b>										
Low cost	53	55	57	59	61	63	65	72	81	90
Hand-held	53	55	57	59	61	63	65	72	81	90
Cost-performance	170	170	170	191	214	225	235	270	308	351
High-performance	450	450	450	509	567	595	622	713	817	937
Harsh	53	55	57	59	61	63	65	72	81	90
Memory	132	139	145	152	159	167	174	200	229	262

*Solutions Exist*

*Solutions Being Pursued*

*No Known Solutions*

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# Table 59A/B (con't.)

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100nm</i>	<i>2008 70nm</i>	<i>2011 50nm</i>	<i>2014 35nm</i>
<b><i>Power : Single-Chip Package (watts)</i></b>										
<b>Low cost</b>	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
<b>Hand-held</b>	1.4	1.6	1.8	2.0	2.2	2.3	2.4	2.0	2.2	2.4
<b>Cost-performance</b>	48	54	61	75	81	88	96	104	109	115
<b>High-performance</b>	88	100	115	130	140	150	160	170	174	183
<b>Harsh</b>	14	14	14	14	14	14	14	14	14	14
<b>Memory</b>	0.8	1.0	1.2	1.4	1.6	1.8	2	2.5	3.0	3.5
<b><i>Core Voltage (volts)</i></b>										
<b>Low cost</b>	1.8	1.8	1.8	1.5	1.5	1.2	1.2	0.9	0.6	0.5-0.6
<b>Hand-held</b>	1.5-1.8	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2	0.6-0.9	0.5-0.6	0.3-0.6
<b>Cost-performance</b>	1.8	1.8	1.8	1.5	1.5	1.2	1.2	0.9	0.6	0.5-0.6
<b>High-performance</b>	1.8	1.8	1.8	1.5	1.5	1.2	1.2	0.9	0.6	0.5-0.6
<b>Harsh</b>	5.0	3.3	3.3	2.5	2.5	2.5	2.5	2.5	2.5	2.5
<b>Memory</b>	1.8	1.8	1.8	1.5	1.5	1.2	1.2	0.9	0.6-0.9	0.5-0.6

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*No Known Solutions*



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<b><i>Package Pin Count</i></b>										
Low cost	80-290	86-313	90-338	101-365	109-395	118-426	127-460	160-580	201-730	254-920
Hand-held	128-368	138-397	149-429	161-464	174-501	188-541	203-584	256-736	322-927	406-1167
Cost-performance	370-740	400-821	432-912	466-1012	503-1123	544-1247	587-1384	740-1893	932-2589	1174-3541
High-performance	1600	1792	2007	2248	2518	2820	3158	4437	6234	8758
Harsh	40-240	40-259	40-280	40-302	40-327	40-353	40-381	40-480	40-604	40-761
Memory	44-128	44-128	44-128	44-144	44-144	48-160	48-160	48-182	48-200	48-220
<b><i>Overall Package Profile (mm)</i></b>										
Low cost	1.7	1.7	1.2	1.2	1.2	1.0	1.0	1.0	1.0	1.0
Hand-held	1.2	1.2	1.0	1.0	1.0	0.8	0.8	0.65	0.65	0.5
Cost-performance	1.2 - 1.7	1.2-1.7	1.0 - 1.2	1.0 - 1.2	1.0 - 1.2	0.8 - 1.0	0.8 - 1.0	0.65 - 0.8	0.65 - 0.8	0.5 - 0.65
High-performance	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Harsh	1.4	1.4	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Memory	1.2	1.2	1.0	1.0	1.0	0.8	0.8	0.65	0.65	0.5

*Solutions Exist*

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\* Red - To meet package profile -> smaller ball -> coplanarity problem

\*\* .65mm ball pitch

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<b><i>Performance : On-Chip (MHz)</i></b>										
Low cost	300	350	415	460	510	570	633	840	1044	1250
Hand-held	300	350	415	460	510	570	633	840	1044	1250
Cost-performance	600	660	727	800	890	989	1100	1400	1800	2200
High-performance	1200	1321	1454	1600	1724	1857	2000	2500	3000	3600
Harsh	25	40	60	60	60	60	60	100	100	100
Memory(D/SRAM)	133/300	133/330	150/362	150/400	150/445	150/495	150/550	175/700	200/900	225/1100
<b><i>Performance : Chip-to-Board for Peripheral Buses (MHz)</i></b>										
Low cost	75	75	100	100	100	100	100	125	125	150
Hand-held	75	75	100	100	100	100	100	125	125	150
Cost-performance	133/300	133/330	150/362	150/400	150/445	150/495	150/550	175/700	200/900	225/1100
High-performance	600	660	727	800	862	928	1000	1250	1500	1800
Harsh	25	40	60	60	60	60	60	100	100	125
Memory(D/SRAM)	133/300	133/330	150/362	150/400	150/445	150/495	150/550	175/700	200/900	225/1100

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<b><i>Junction Temperature Maximum (°C)</i></b>										
Low cost	125	125	125	125	125	125	125	125	125	125
Hand-held	115	115	115	115	115	115	115	115	115	115
Cost-performance	100	95	90	85	85	85	85	85	85	85
High-performance	100	95	90	85	85	85	85	85	85	85
Harsh	155	155	155	155	155	155	175	185	185	185
Memory	100	100	100	100	100	100	100	100	100	100
<b><i>Operating Temperature Maximum : Ambient (°C)</i></b>										
Low cost	55	55	55	55	55	55	55	55	55	55
Hand-held	55	55	55	55	55	55	55	55	55	55
Cost-performance	45	45	45	45	45	45	45	45	45	45
High-performance	45	45	45	45	45	45	45	45	45	45
Harsh	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 170	-40 to 180	-40 to 180	-40 to 180
Memory	55	55	55	55	55	55	55	55	55	55

*Solutions Exist*

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## Notes for Table 59 for Assembly and Packaging Requirements

- [A] All costs do not include silicon, heat sinks, or test; substrate cost should not exceed 30–50% of total cost.
- [B] Solutions are being pursued for cost-performance ? 65 W and for high-performance ? 110 W due to cost-driven thermal management issues. Cost-performance data is for desktop applications; notebook applications are limited to 14 W maximum in 1999 The memory power is for the SRAM chip.
- [C] Reflects package/substrate cost issues. RAMBUS and other serialized memories are not addressed.
- [D] The high-performance IC may be classified into two categories. The application-specific integrated circuit (ASIC) has a high number of signal I/O pins. The total number of voltage/ground pins is about one half of the number of signal I/O pins. The microprocessor has signal I/O pins much less than that of the ASIC; however, the power consumption of the microprocessor is much higher than that of the ASIC. Even with such a high number of voltage/ground pins, the effective overall inductance is still very high. On-chip de-coupling capacitance is needed. Ideally, one may want to place an on-chip de-coupling capacitance,  $C(\text{de-coupling}) \approx 9 \text{ Power} / \{f(\text{on-chip}) \times [\text{Core Voltage}]^2\}$ . Such consideration also applies to many of the high power cost-performance applications.
- [E] > 450 MHz reflects need for improved impedance control.
- [F] xx/yyy refers to system memory and peripheral bus speed (xx) and to processor cache memory data transfer (yyy) for high end of cost-performance category. Memory performance must match the requirements of processor buses and may require new architectures at the device or array level, such as reduced-width multiplexed buses that run at the on-chip frequency.
- [G] > 1000 MHz reflects need for improved impedance control.
- [H] Uncertain materials solutions. Reflects package/substrate cost issues.

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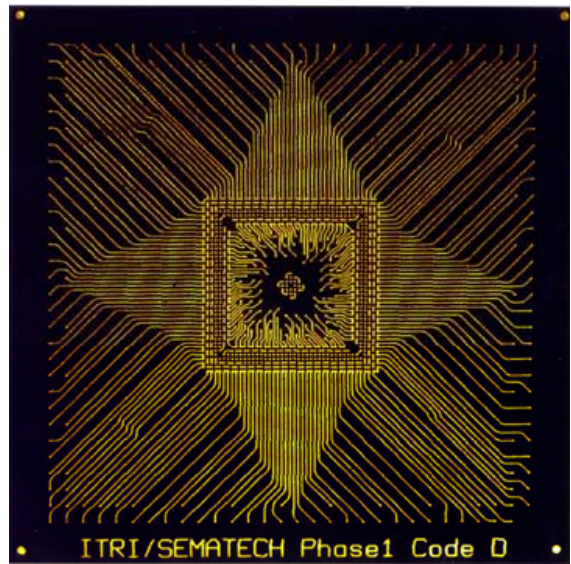
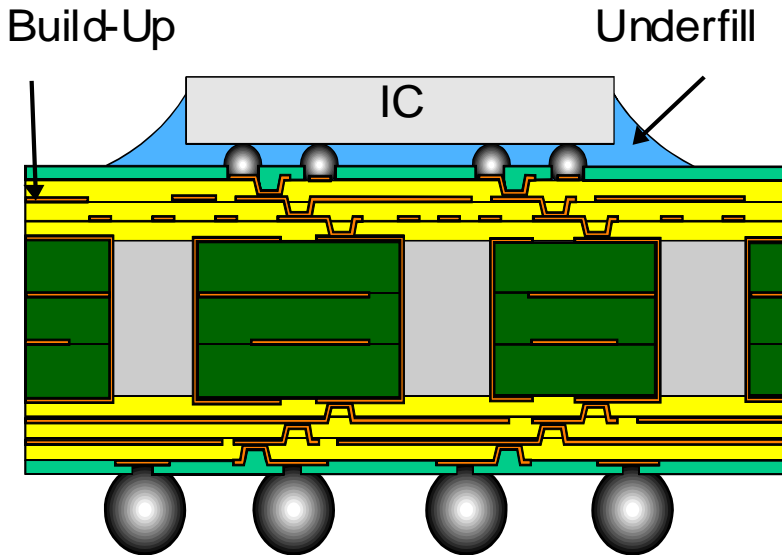


Wafer bumping  
Electromigration  
Wafer level packaging  
Chip-to-next level interconnect

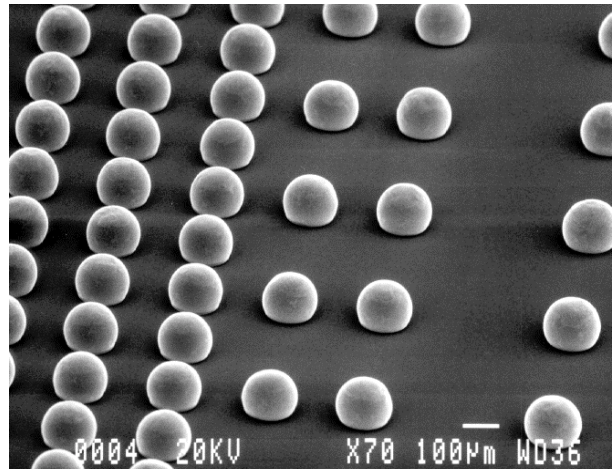
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Thin film build-up using 75  $\mu\text{m}$  vias



# Current Limits of 63Sn/37Pb Flip Chip Solder Bumps & Ramification

Bump pitch	Passivation opening	100° C	90° C	80° C
250μm	85μm	75mA	110mA	165mA
200μm	80μm	66mA	97mA	145mA
150μm	65μm	45mA	65mA	95mA

Conclusions:

For a given current, **four times of pads** will be needed, if the **bump pitch is cut in half**.

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# Wafer level Packaging

- All of IC packaging performed at wafer level
- Constant percentage of total wafer cost
- Compatible with chip size shrink in later years
- Low I/O ( $\leq 100$ )
- Need wafer level test & burn-in



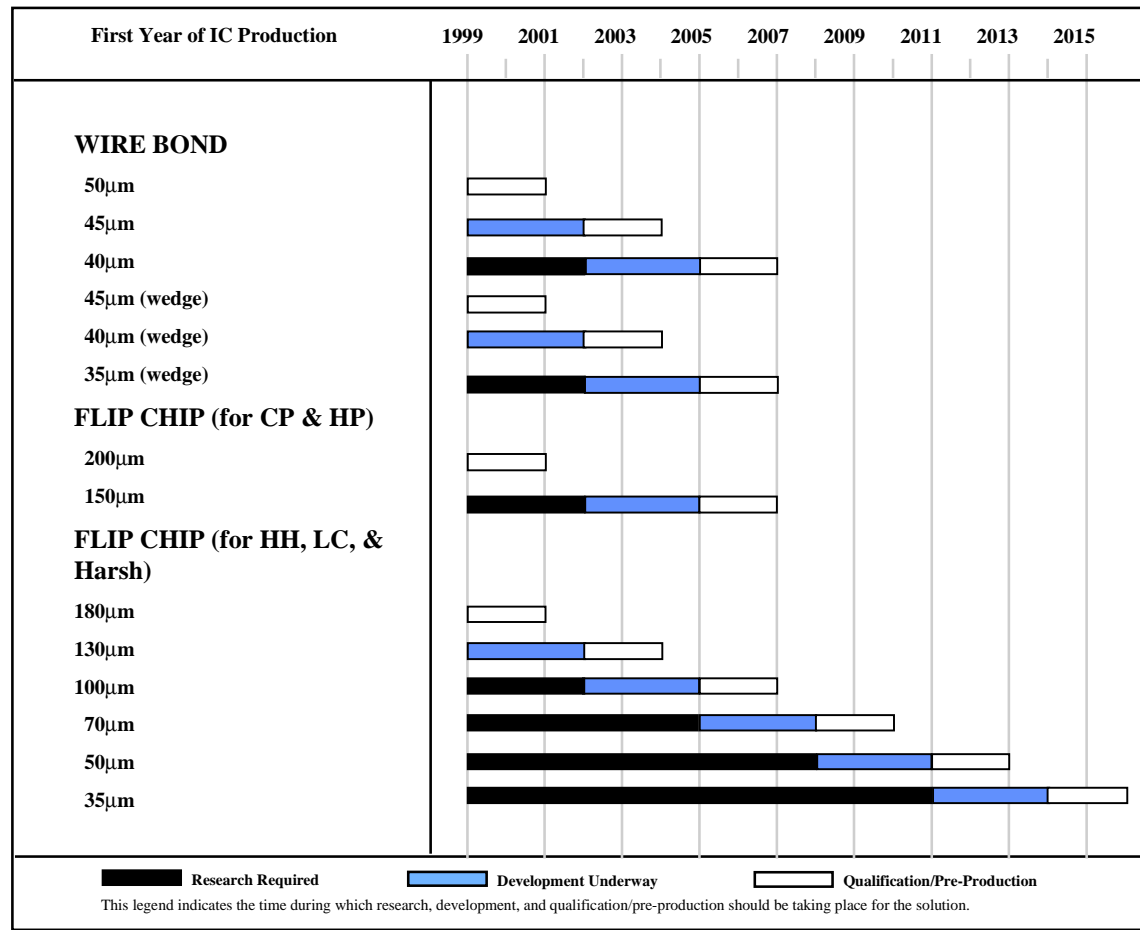
**Table 61A. Chip-to-Next Level Interconnect Needs - Near Term**

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>
<i>Chip Interconnect Pitch (<math>\mu\text{m}</math>)</i>							
Wire bond—ball	<b>50</b>	<b>49</b>	<b>47</b>	<b>45</b>	<b>42</b>	<b>41</b>	<b>40</b>
Wire bond—wedge	<b>45</b>	<b>44</b>	<b>42</b>	<b>40</b>	<b>37</b>	<b>36</b>	<b>35</b>
TAB*	<b>50</b>	<b>50</b>	<b>40</b>	<b>40</b>	<b>40</b>	<b>40</b>	<b>30</b>
<b>Flip chip (area array) for C/P &amp; H/P</b>	<b>200</b>	<b>200</b>	<b>200</b>	<b>200</b>	<b>200</b>	<b>200</b>	<b>150</b>
Flip chip for HH, LC & Harsh	<b>180</b>	<b>165</b>	<b>150</b>	<b>130</b>	<b>120</b>	<b>110</b>	<b>100</b>

**Table 61B. Chip-to-Next Level Interconnect Needs - Long Term**

<i>Year of First Product Shipment Technology Generation</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
<i>Chip Interconnect Pitch (<math>\mu\text{m}</math>)</i>			
Wire bond—ball	<b>40</b>	<b>40</b>	<b>40</b>
Wire bond—wedge	<b>35</b>	<b>35</b>	<b>35</b>
TAB*	<b>30</b>	<b>30</b>	<b>30</b>
<b>Flip chip (area array) for C/P &amp; H/P</b>	<b>150</b>	<b>150</b>	<b>150</b>
<b>Flip chip for HH, LC &amp; Harsh</b>	<b>70</b>	<b>50</b>	<b>35</b>
* TAB—tape automated bonding			

# Figure 45. Chip-to-Next Level Interconnect Potential Solutions



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# Fine pitch BGA and Chip Scale Packages

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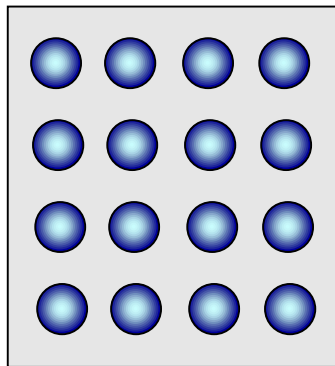
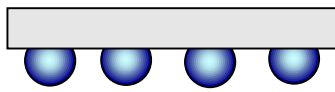


# What is FBGA ?

- \* FBGA is an IC with dimensions equal to or slightly larger than those of the silicon die it contains.
- Specifically, a package with size (L x W) equal to the size of the chip is called a Real Chip Size Package.

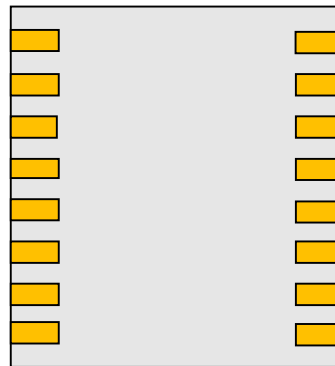
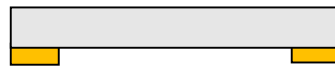
# CSP vs. Very Small Size Package

- “CSP” is a general naming for the package with size equal to or slightly larger than a real chip size.



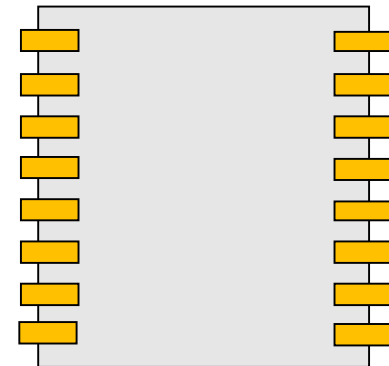
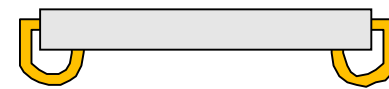
Area Array CSP

**FBGA**  
**FLGA**



Peripheral CSP

**SON**  
**QFN**



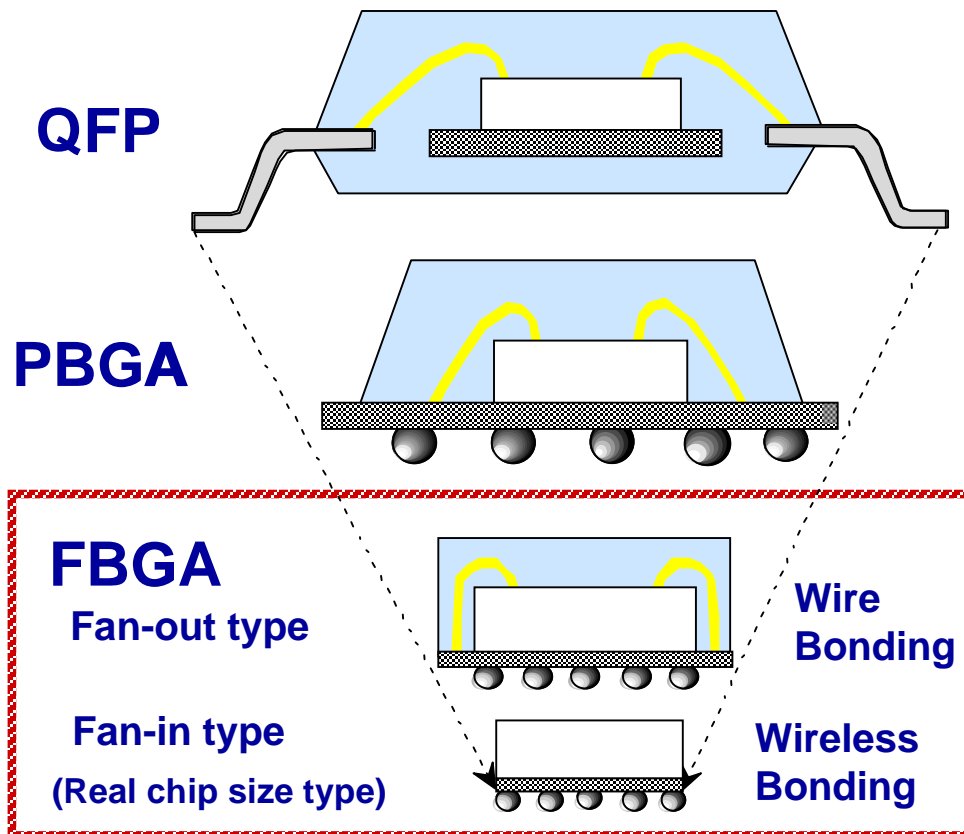
Very Small Size Package (leaded)

**TSOJ**  
**SOC**

# What is a FBGA ?

(Chip size / Scale package)

- **FBGA** is the **BGA type** of **CSP packages** which include FBGA, FLGA, SON & QFN
- **Size of Package** : **Equal to or Less than 21mm**
- **Solder Ball Pad Pitch** : **Equal to or Less than 0.8mm**



Company	Nick name
TI	$\mu$ Star BGA™
NEC	D <sup>2</sup> BGA™
Tessera	$\mu$ BGA™

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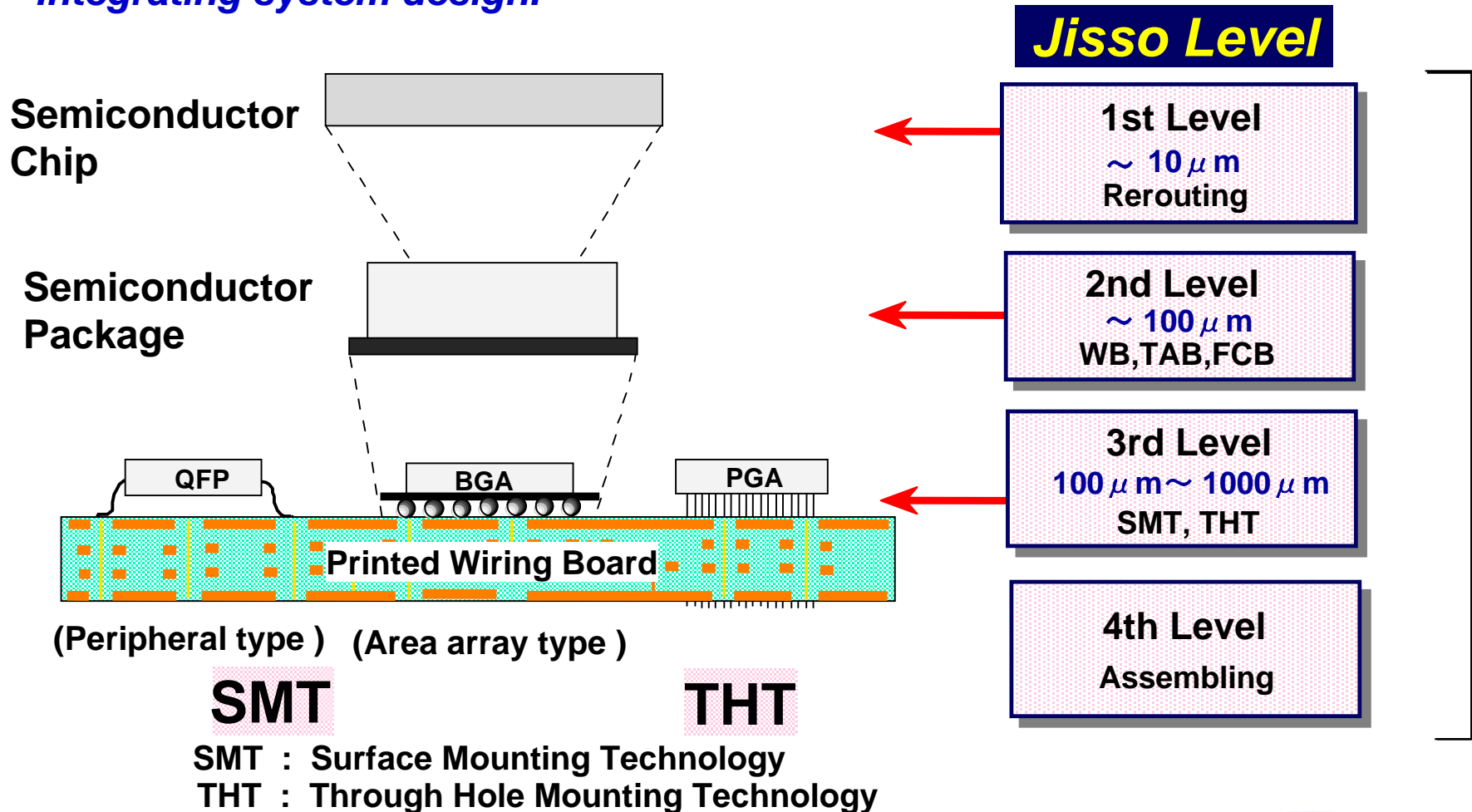


# **FBGA Definition by EIAJ**

- **FBGA is the BGA type of CSP packages which include FBGA, FLGA, SON & QFN**
- **Size of Package: Equal to or Less than 21 mm**
- **Solder Ball Pad Pitch: Equal to or Less than 0.8 mm**
- **“CSP” is a general naming for package with size equal to or slightly larger than chip size**

# The Concept of 実装 (Jisso) ?

Total solution for Interconnecting, Assembling, Packaging, Mounting and Integrating system design.



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**Table 62A/B. Single Chip Packages  
Ball Grid Array Packages - Near Term**

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100nm</i>	<i>2008 70nm</i>	<i>2011 50nm</i>	<i>2014 35nm</i>
<b><i>BGA SolderBall pitch (mm)</i></b>										
<b>Low cost</b>	<b>1.27</b>	<b>1.27</b>	<b>1.27</b>	<b>1.27</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>0.8</b>	<b>0.8</b>
<b>Hand-held</b>	<b>1.27</b>	<b>1.27</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>0.8</b>	<b>0.8</b>	<b>0.65</b>
<b>Cost-performance</b>	<b>1.27</b>	<b>1.27</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>0.8</b>	<b>0.8</b>	<b>0.65</b>
<b>High-performance</b>	<b>1.00</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.80</b>	<b>0.65</b>	<b>0.65</b>	<b>0.5</b>	<b>0.5</b>
<b>Harsh</b>	<b>1.27</b>	<b>1.27</b>	<b>1.27</b>	<b>1.27</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>1.00</b>	<b>0.8</b>	<b>0.8</b>
<b><i>BGA Possible Pin Count</i></b>										
<b>Low cost</b>	<b>312</b>	<b>312</b>	<b>392</b>	<b>392</b>	<b>420</b>	<b>512</b>	<b>512</b>	<b>684</b>	<b>800</b>	<b>968</b>
<b>Hand-held</b>	<b>392</b>	<b>420</b>	<b>512</b>	<b>512</b>	<b>512</b>	<b>576</b>	<b>684</b>	<b>800</b>	<b>968</b>	<b>1200</b>
<b>Cost-performance</b>	<b>840</b>	<b>840</b>	<b>1012</b>	<b>1012</b>	<b>1200</b>	<b>1352</b>	<b>1568</b>	<b>2112</b>	<b>2664</b>	<b>3612</b>
<b>High-performance</b>	<b>1680</b>	<b>1860</b>	<b>2112</b>	<b>2380</b>	<b>2664</b>	<b>2964</b>	<b>3280</b>	<b>3612</b>	<b>6844</b>	<b>8448 *</b>
<b>Harsh</b>	<b>312</b>	<b>312</b>	<b>392</b>	<b>392</b>	<b>420</b>	<b>512</b>	<b>512</b>	<b>684</b>	<b>800</b>	<b>968</b>
<p>A = integer (BGA size/pitch) ; R = integer (A/3) ;  Pincount = (A-R) × R × 4 ; body sizes rounded to nearest JEDEC size</p> <p>* This is the I/O limit for the 50mm BGA package, and is not sufficient for the 8758 pins shown in Table43.</p>										



**Table 63A. Single Chip Packages  
Examples - FBGA/CSP (Near Term)**

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>
FBGA/CSP area array pitch (mm)	<b>0.5</b>	<b>0.5</b>	<b>0.4</b>	<b>0.4</b>	<b>0.4</b>	<b>0.4</b>	<b>0.4</b>
FBGA/CSP size (mm/side)	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>10</b>
# Rows/# leads (one fan-out layer)	<b>3/192</b>	<b>3/192</b>	<b>3/252</b>	<b>3/252</b>	<b>3/252</b>	<b>3/252</b>	<b>3/252</b>
# Rows/# leads (two fan-out layers)	<b>4/420</b>	<b>4/240</b>	<b>4/320</b>	<b>4/320</b>	<b>4/320</b>	<b>4/320</b>	<b>5/380</b>
FBGA/CSP size (mm/side)	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>
# Rows/# leads (one fan-out layer)	<b>3/456</b>	<b>3/456</b>	<b>3/576</b>	<b>3/576</b>	<b>3/576</b>	<b>3/576</b>	<b>3/576</b>
# Rows/# leads (two fan-out layers)	<b>4/592</b>	<b>4/592</b>	<b>4/752</b>	<b>4/752</b>	<b>4/752</b>	<b>4/752</b>	<b>5/920</b>

*A = integer (CSP size / pitch - 1); R = # rows, # leads = (A-R) × R × 4*

**Table 63B. Single Chip Packages  
Examples - FBGA/CSP (Long Term)**

<i>Year of First Product Shipment Technology Generation</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
FBGA/CSP area array pitch (mm)	<b>0.3</b>	<b>0.3</b>	<b>0.25</b>
FBGA/CSP size (mm/side)	<b>10</b>	<b>10</b>	<b>10</b>
# Rows/# leads (one fan-out layer)	<b>3/348</b>	<b>3/348</b>	<b>3/432</b>
# Rows/# leads (two fan-out layers)	<b>5/540</b>	<b>6/624</b>	<b>6/792</b>
FBGA/CSP size (mm/side)	<b>21</b>	<b>21</b>	<b>21</b>
# Rows/# leads (one fan-out layer)	<b>3/792</b>	<b>3/792</b>	<b>3/960</b>
# Rows/# leads (two fan-out layers)	<b>5/1280</b>	<b>6/1512</b>	<b>6/1840</b>

*A = integer (CSP size / pitch - 1); R = # rows, # leads = (A-R) × R × 4*

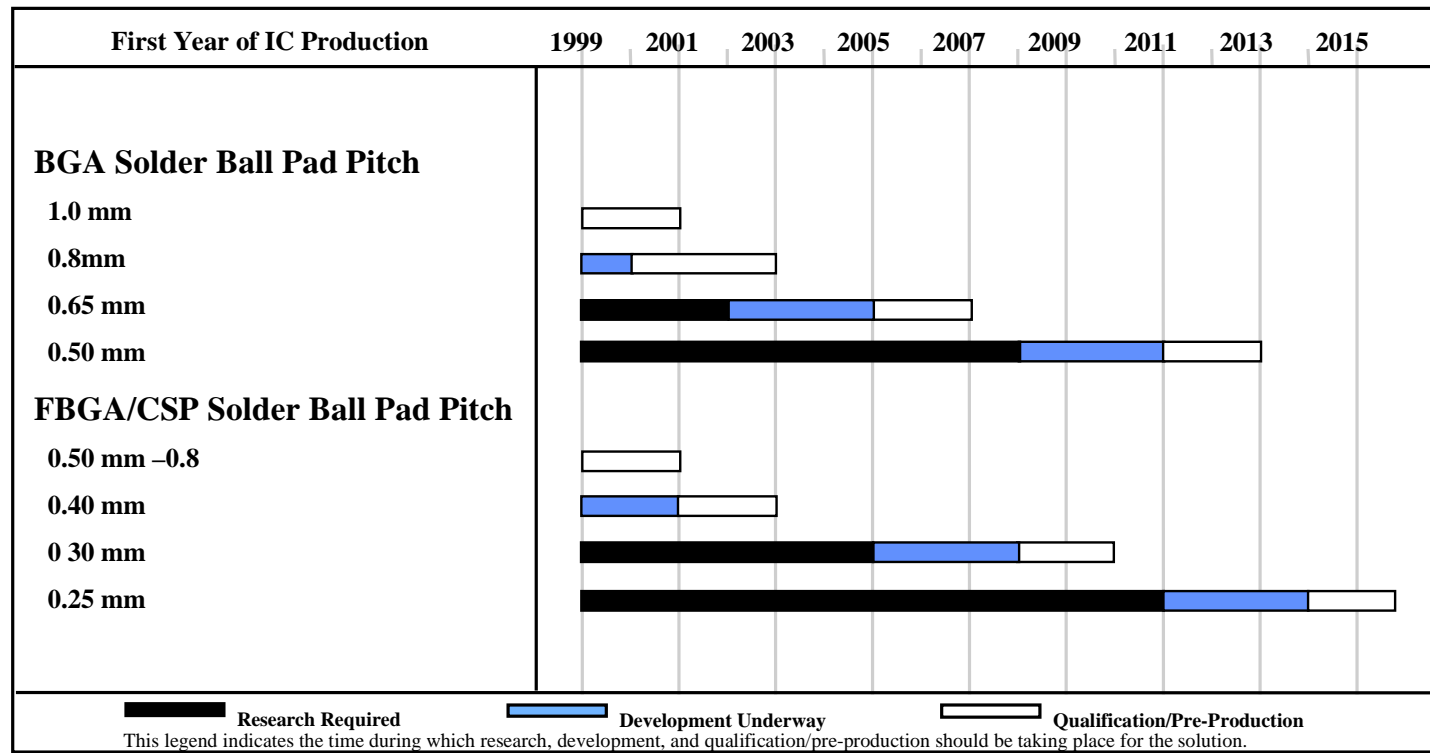
## Table 64A. Potential PWB Solutions for BGA and FBGA/CSP Pkg. (Near Term)

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>
FBGA/CSP <b>solder ball</b> pad pitch (mm)	0.5	0.5	0.4	0.4	0.4	0.4	0.4
Pad size ( $\mu\text{m}$ )	200	200	160	160	160	160	160
Line width ( $\mu\text{m}$ )	60	60	48	48	48	48	48
Line spacing ( $\mu\text{m}$ )	60	60	48	48	48	48	48
# Rows accessed	3	3	3	3	3	3	3

## Table 64B. Potential PWB Solutions for BGA and FBGA/CSP Pkg. (Long Term)

<i>Year of First Product Shipment Technology Generation</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>
FBGA/CSP <b>solder ball</b> pad pitch (mm)	0.3	0.3	0.25
Pad size ( $\mu\text{m}$ )	120	120	100
Line width ( $\mu\text{m}$ )	36	36	30
Line spacing ( $\mu\text{m}$ )	36	36	30
# Rows accessed	3	3	3

# Figure 46. Potential PWB Solutions for BGA and FBGA/CSP Packages



\* FBGA assumes fraction of PTH pitch requires fan-out on PWB surface

# High density package substrate and printed wiring boards

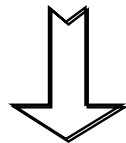
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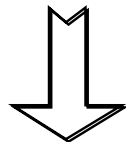
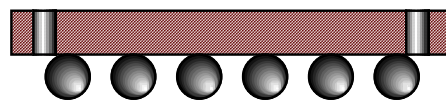


# Key Role of Substrate

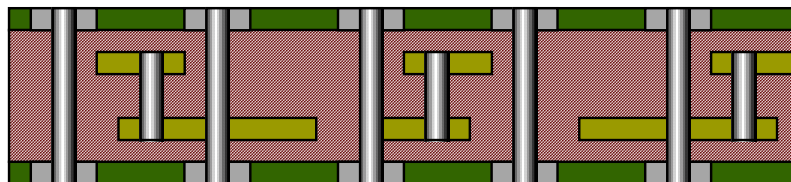
Bare Die



Substrate  
(Interposer)



Mother Board



- High pad density
- High operation frequency

- Fine pitch interconnection
- Low capacity

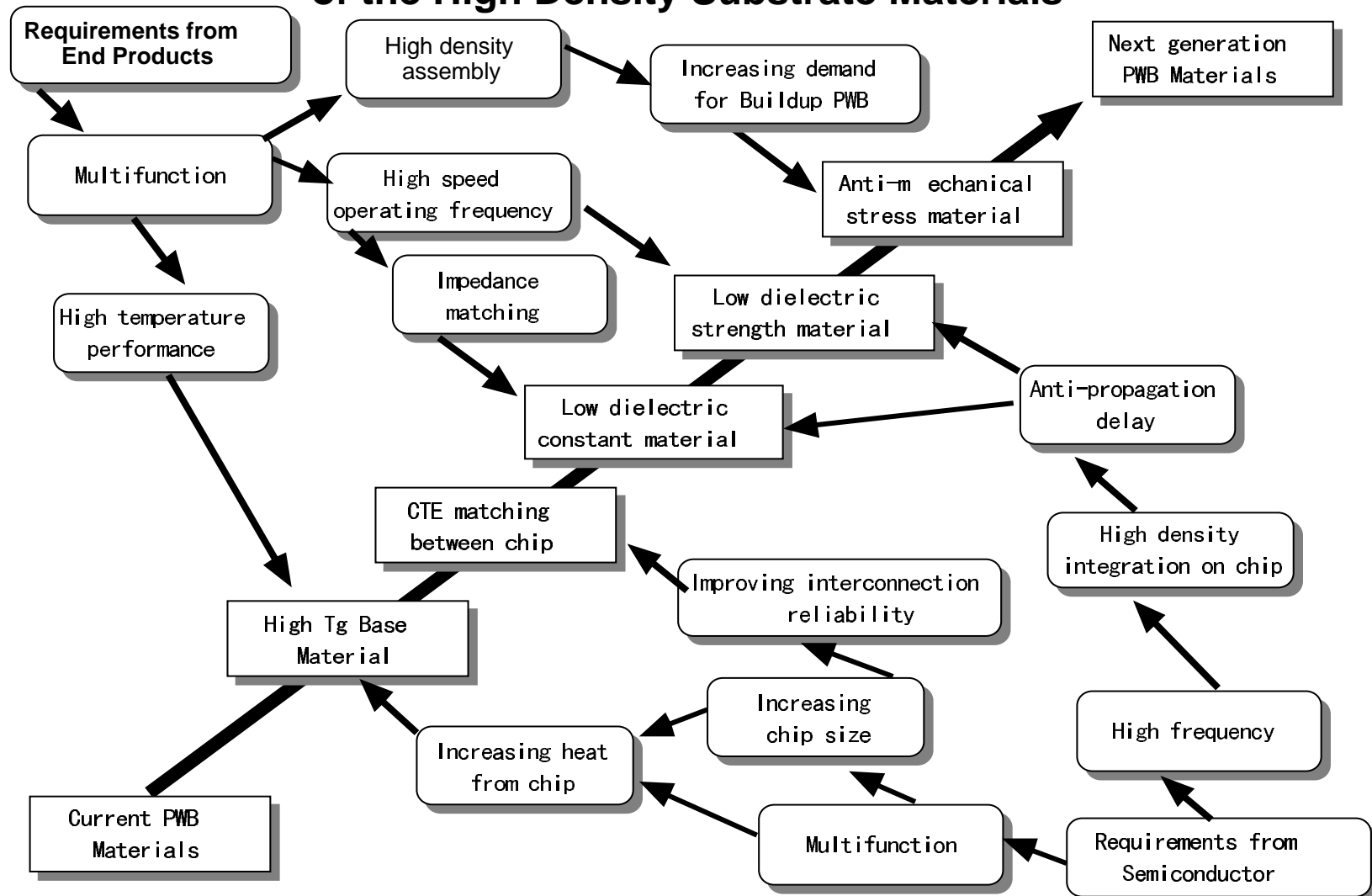
- Fine density interconnection
- Same foot print as of Substrate

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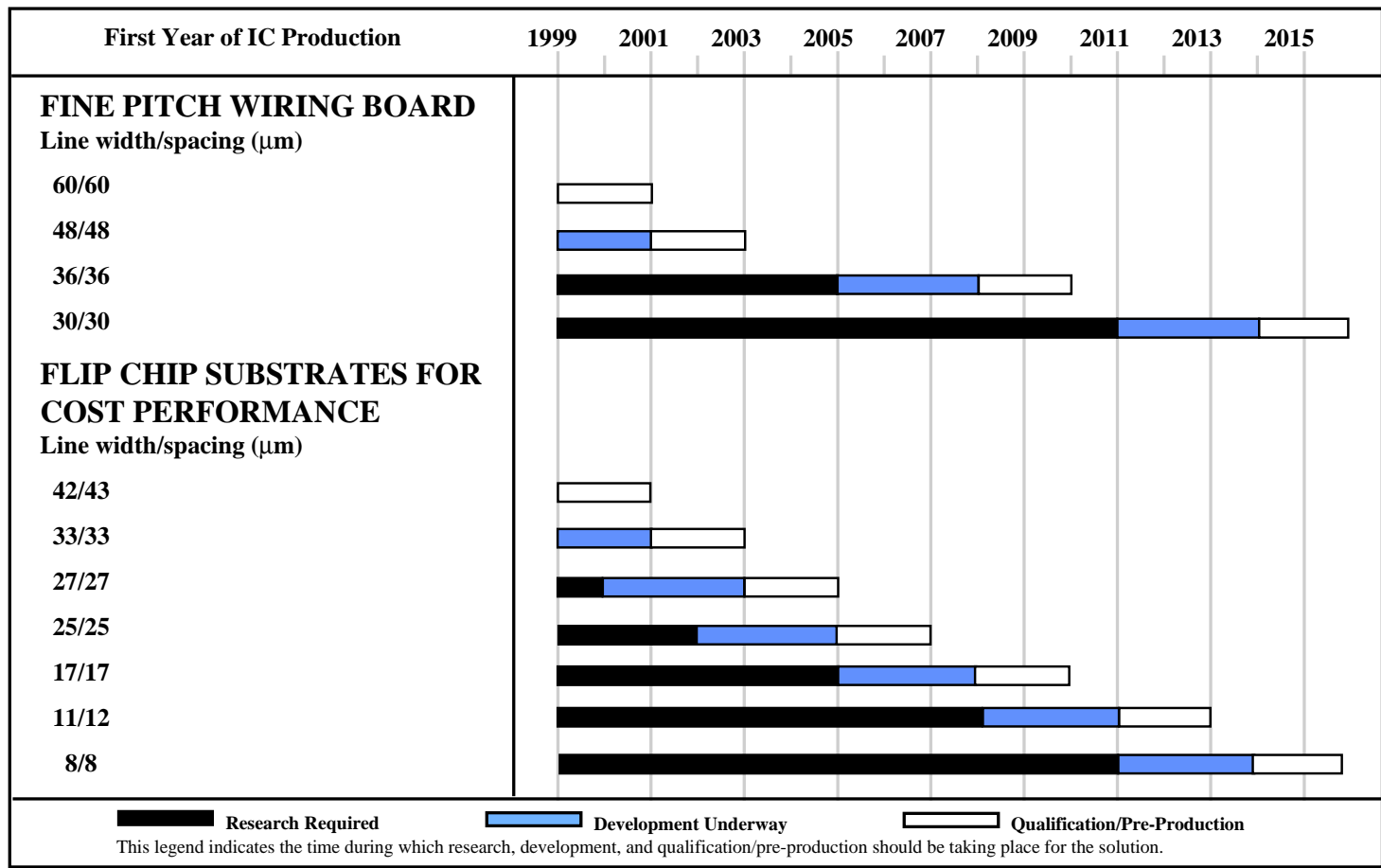
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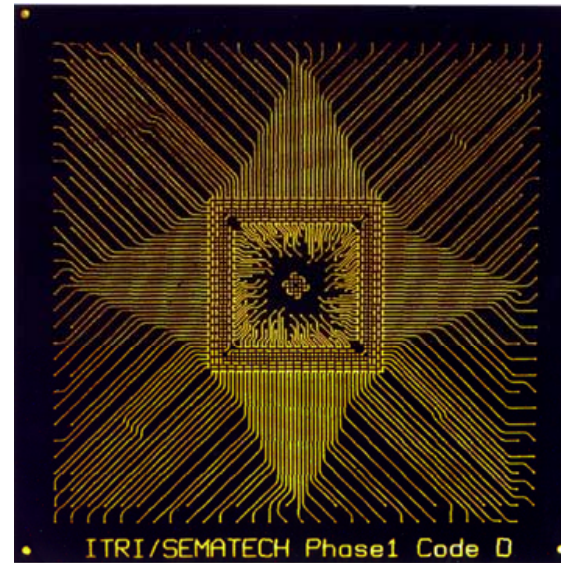
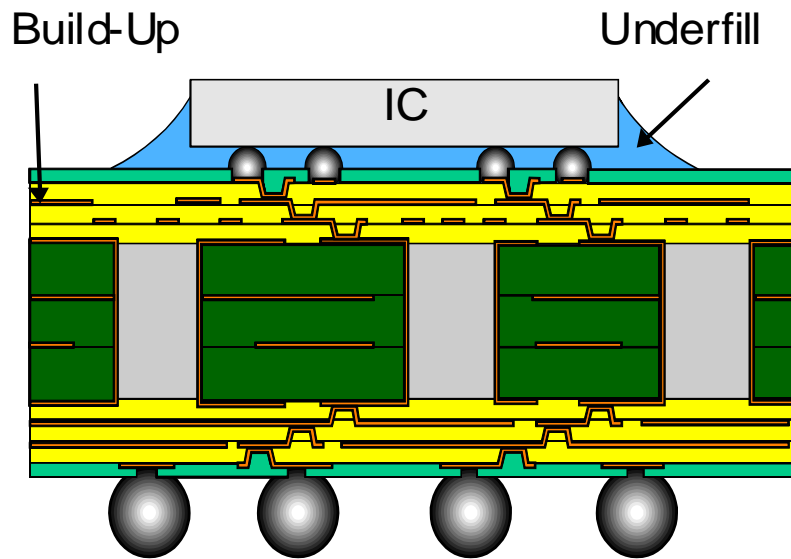


**Figure 47. A Potential Procedure for the Development of the High Density Substrate Materials**

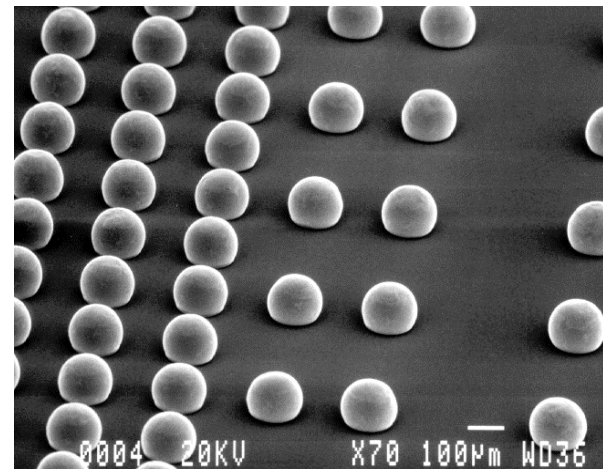


# Figure 48. High Density Polymer Substrate Potential Solutions





Thin film build-up using 75  $\mu\text{m}$  vias



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# Definition of BGA & FBGA in ITRS to 2014

With # signal I/O for **BGA** well exceeding 1000s, surface redistribution on PWB is not effective. **The pitch (in mm) between BGA solder balls** has to be identical to that between the PWB PTHs to access the internal wiring layers in the PWB.

Year	1999	2002	2005	2008	2011	2014
H/P (mm)	1.00	0.80	0.65	0.65	0.50	0.50
C/P (mm)	1.27	1.00	1.00	0.80	0.80	0.65

**FBGA** focuses on a **minimum** package size, **the pitch (in mm) between FBGA solder balls** is a fraction of that between the PWB PTHs. Surface redistribution on PWB is needed.

Year	1999	2002	2005	2008	2011	2014
pitch (mm)	0.50	0.40	0.40	0.30	0.30	0.30

# PWB Top-side Fan-out for FBGA Packages

Year	1999	2002	2005	2008	2011	2014
Solder ball pitch ( $\mu\text{m}$ )	500	400	400	300	300	250
pad size ( $\mu\text{m}$ )	200	160	160	120	120	100
line width ( $\mu\text{m}$ )	60.0	48.0	48.0	36.0	36.0	30.0

Comment:

Top-side redistribution is not needed on PWB for BGA mounting, but is needed for the Flip Chip BGA substrates.

Top-side redistribution for Cost-performance BGA substrate:

line width ( $\mu\text{m}$ )	42.5	33.0	25.0	17.0	11.5	8.0
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# Flip Chip BGA Substrate Top-side Fan-out

Year	1999	2002	2005	2008	2011	2014
Pad pitch ( $\mu\text{m}$ )	200	200	150	150	150	150
Pad size ( $\mu\text{m}$ )	100	100	75	75	75	75

## Cost-performance application

	# lines replacing one depopulated pad:					
	3	4	4	6	9	13
line width ( $\mu\text{m}$ )	42.5	33.0	25.0	17.0	11.5	8.0

## High-performance application

	# lines replacing one depopulated pad:					
	5	7	7	10	16	25
line width ( $\mu\text{m}$ )	27.0	20.0	15.0	10.5	6.5	4.0

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# Flip Chip Substrate Fan Out Requirements (Table 65)

- Cost Performance and high performance only
  - Only one pad pitch change at the 100 nm generation to minimize test probe head cost
- Depopulated outer row to increase fan out line width and spacing (e.g., 42 $\mu$ m vs. 34 $\mu$ m for 1999)

**Table 65A/B. Flip Chip Substrate Top-Side Fan-Out Requirements (Near Term)**

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100nm</i>	<i>2008 70nm</i>	<i>2011 50nm</i>	<i>2014 35nm</i>
<i>Flip Chip Pad Pitch (μm)</i>	200	200	200	200	200	200	150	150	150	150
<i>Pad Size (μm) @</i>	100	100	100	100	100	100	75	75	75	75
<b>Chip Size (mm/side)</b>										
Cost-performance	12	12	12	12	12	12	12	12	12	12
High-performance	17	17	17	17	17	17	17	17	17	17
<b>Array size = # pads along chip edge</b>										
Cost-performance (maximum)	59	59	59	59	59	59	79	79	79	79
Cost-performance (needed)	51	56	51	56	53	58	75	75	75	78
High-performance (maximum)	84	84	84	84	84	84	112	112	112	112
High-performance (needed)	73	81	79	79	79	81	107	112	109	111
<b># Outer Rows Accessed (will determine # fan-out layers needed)</b>										
Cost-performance	4	4	5	5	6	6	5	7	10	14
High-performance	6	6	7	8	9	10	8	11	17	26
<b>Effective Total Wiring Density for Fan-out Need (cm/cm<sup>2</sup>)</b>										
Cost-performance	200	200	250	250	300	300	333	467	667	933
High-performance	300	300	350	400	450	500	533	733	1133	1733
<b>Wiring Substrate (Three or more lines replacing one depopulated pad—accessing 2.0 or more rows per fan-out layer)</b>										
Line width (μm)	42.5	42.5	33.0	33.0	27.0	27.0	25.0	17.0	11.5	8.0
Line spacing (μm)	43.1	43.1	33.6	33.6	27.5	27.5	25.0	17.5	12.1	8.6
<b>Wiring Substrate (Five or more lines replacing one depopulated pad—accessing 3.0 or more rows per fan-out layer)</b>										
Line width (μm)	27.0	27.0	23.0	20.0	17.5	15.5	15.0	10.5	6.5	4.0
Line spacing (μm)	27.5	27.5	23.1	20.0	17.7	16.0	15.0	10.9	7.1	4.8
<b># Leads Accessed</b>										
Cost-performance	752	832	920	1020	1128	1248	1400	1904	2600	3584
High-performance	1608	1800	2016	2272	2520	2840	3168	4444	6256	8840

*A = array size, R = # rows, # leads = (A-R) × R × 4 ; via pitch must be ≤ pad pitch*

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System-on-a-chip (SoC)  
RF & mixed signal packaging  
System-in-a-Package (SiP)  
Integrated design environment  
Reliability issues

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# System-on-a-Chip Packaging

- The chip size of Low-cost and Handheld ICs is usually small, often leadcount and pad pitch limited.
- Migration path:  $\mu$ controller core in one chip, then DSP+  $\mu$ controller cores in one chip, then add A/D & D/A, .....
- Two packages reduce to one with equal or less I/O
- Reduce package cost, PWB area, delay time & power
- Increase inter-core bus width, improve performance
- Packaging challenges:
  - signal integrity: de-coupling, shielding, grounding
  - verification: early packaging involvement in SoC design
  - testing: wafer probe and packaging level (@ design stage)

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# RF and Mixed Signal Packaging

- Driven by low cost mobile and high bandwidth products
- Si (2.5 GHz), GaAs or SiGe (higher frequency)
- Flip chip connection, embedded passives on package
- FBGA/CSP: low inductance and high density
- Integrated modeling and simulation at chip and packaging levels: design cycle time reduction
- Single chip radio: memory, process and mixed signal functions
- Micro-Electro-Mechanical System (MEMS)
  - filter, switch, oscillator, ..... etc.
  - small size, low insertion loss, low power, integration with ICs, and potential of low cost with batch fabrication
  - challenges: reliability, temperature sensitivity, hermetic/vacuum packaging

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# System-in-a-Package (SiP)

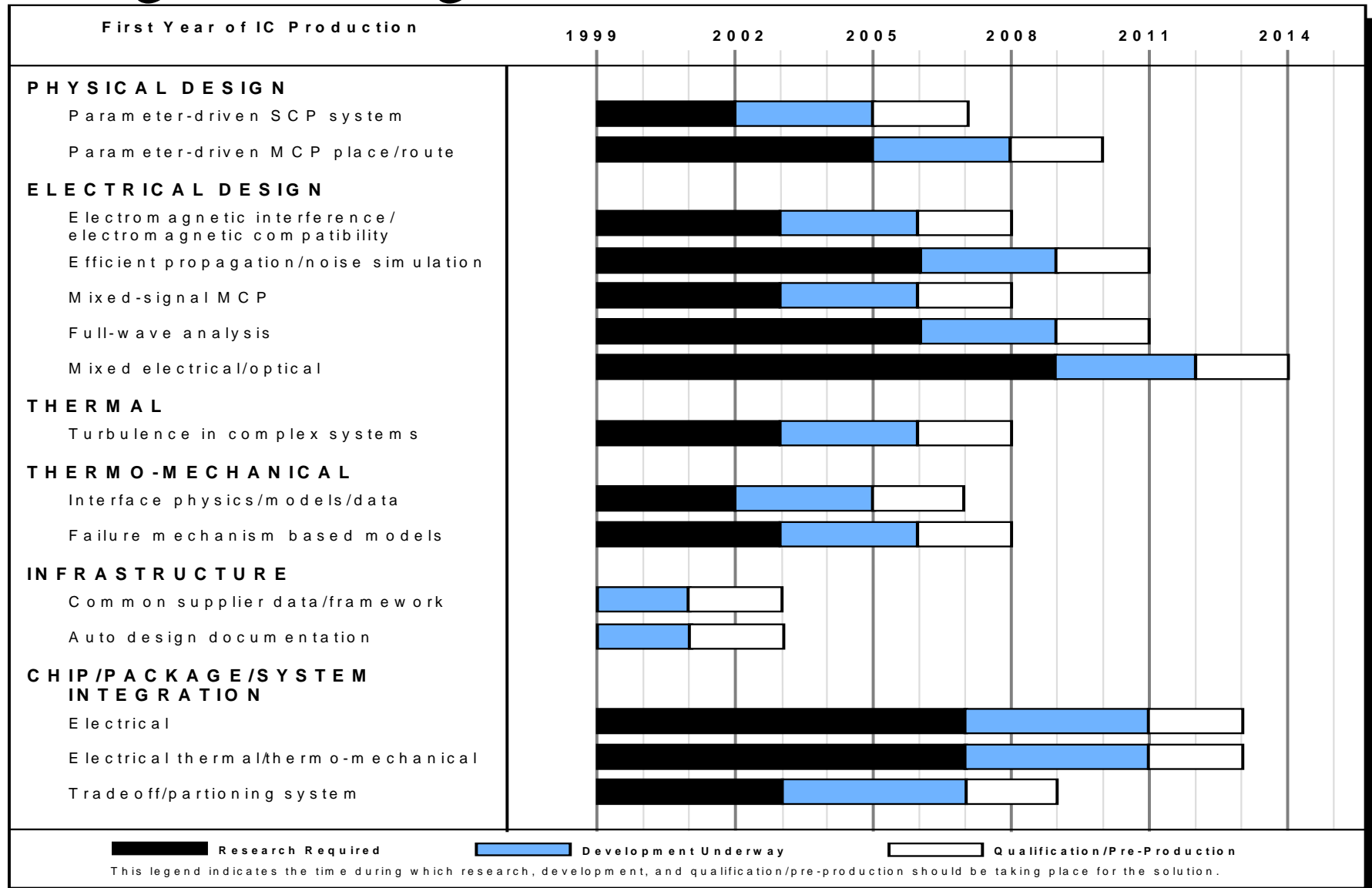
- Digital ICs, Analog ICs, RF ICs on the Few-chip package (FCP)
- Driving force: time-to-market
- Migration path: SoC for chip count reduction (low cost, small size)
- Enablers:
  - flip chip
  - physical design tools
  - high density substrate
  - low cost known-good-die
  - reworkability
  - module testing
- High performance MCM:
  - many high I/O logic and memory chips at close proximity
  - extremely high wiring density substrate
  - key considerations: reliability, overall system cost and performance

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# Integrated Design Environment Potential Solution



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# Reliability Issues

- New packaging format & new materials
  - Cu & low-k dielectric (instead of Al and SiO<sub>2</sub>)
  - Light, thin, short & small
  - Area array flip chip attach
  - Soft errors (alpha particles and cosmic rays)
  - Organic substrate (CTE mismatch with Si chip)
  - High power, large chip, & high I/O in some applications
- Fault isolation techniques & tools
  - Materials bulk and interface properties
  - New failure modes



# Summary

- Invaluable input from international participants
- Industry feedback important
- Flip chip current/pad: critical for high power IC
- High density substrate critical for BGA packages
- Surface fan-out on PWB needed for FBGA mounting
- RF and mixed signal packaging challenges
  - MEMS for microwave filter, switch, oscillator, ...
- SiP for time-to-market benefit
- SoC for cost and size reduction

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