PIDS TWG Report on the ITRS Roadmap Issues

July 8-9, 1999

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Outline

- **Difficult Challenges**
    - **Near Term Challenges**
    - **Long term Challenges**
- **Memory and Logic Issues**
- **Analog, Mixed Signal and RF Issues**
- **Device reliability issues**
- **Other Issues**

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Near Term Difficult Challenges:

1999 Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Meeting device performance targets with available gate stack materials	Production worthy high-k dielectrics and compatible gate materials will not be available.
Function integration at low V_{dd}	Crosstalk, substrate noise, and device performance difficult to optimize simultaneously at high clock rates and low V_{dd}.
Managing power, ground, signal, and clock on multilevel coupled interconnect	Despite the use of low-k dielectrics, interconnect scaling is increasing coupling capacitance, crosstalk and signal integrity issues. Power, clock, and ground distribution will consume an increasing fraction of available interconnect.
Management of increasing reliability risks with the rapid introduction of new technologies.	Inadequate identification and modeling of failure modes in new materials, new operating regions (e.g. tunneling) and new SOC technologies (e.g. MEMS)
Integration of precision passive elements	Maintaining high Q, low noise, and tolerances of discrete components.

- **No gate dielectric available for 100nm node (65nm devices)**
- **Meeting device requirements at Low V_{DD}**
- **Management of Reliability issues with many new materials**
- **Need for Precision Passive elements**

Long Term Difficult Challenges:

FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Overcoming fundamental scaling limits for current device structures	Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling
Integration choices for system on a chip	Cost effective process integration of many functions on a single chip.
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variations.
Design for manufacturability, reliability, and performance.	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, etc.
Low power, low voltage, high performance, and reliable nonvolatile memory element	NVM program and erase require voltages which are incompatible with highly scaled low voltage devices

- **Scaling limits will reduce performance of devices and memory cells**
- **SOC issues will cause difficult integration problems as well as the need for smart design tools to design around process limitations**
- **Atomic Level Fluctuations causing unacceptable statistical variation**

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Memory and Logic Issues

- **Device scaling will end unless new gate stack materials are developed**

- **SOC integration issues will put a greater demand on process innovation**
  - Embedded Combinations critical for development
  - Predicting choices drive development more than scaling

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Memory and Logic Requirements

	Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2000* *165 nm*	*2001* *150 nm*	*2002* *130 nm*	*2003* *120 nm*	*2004* *110 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
3	MPU / ASIC Half Pitch (nm)	230	210	180	160	145	130	115	45	32	22
5	Min. Logic V_{dd} (V) (desktop)	**1.5 - 1.8**	**1.5 - 1.8**	**1.2 - 1.5**	**1.2 - 1.5**	**1.2 - 1.5**	**0.9 - 1.2**	**0.9 - 1.2**	**0.6 - 0.9**	**0.5 - 0.6**	**0.3 - 0.6**
6	Tox equivalent (nm)	**1.9–2.5**	**1.9–2.5**	**1.5-1.9**	**1.5-1.9**	**1.5-1.9**	**1.2-1.5**	**1.2-1.5**	**0.8-1.2**	**0.6-0.8**	**0.5-0.6**
7	Nominal I_{on} @ 25 °C (μA/μm) [NMOS/PMOS] High Perf.	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**
8	Max I_{off} @ 25 °C (nA/μm) (For min. L device) High Perf.	**5**	**7**	**8**	**10**	**13**	**16**	**20**	**40**	**80**	**160**
9	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	**0**	**27**	**42**	**49**	**65**	**71**	**75**	**87**	**95**	**97**
10	Nominal I_{on} @ 25 °C (μA/μm) [NMOS/PMOS] Low Power	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**
11	Max I_{off} @ 25 °C (pA/μm) (For min. L device) Low Power	**5**	**7**	**8**	**10**	**13**	**16**	**20**	**40**	**80**	**160**
12	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	**0**	**31**	**50**	**60**	**75**	**81**	**84**	**92**	**97**	**98**

- **Simultaneously satisfying I_{on} and I_{off} needs will require new Materials and structures**
  - **Gate stack material critical**

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Potential Solutions

Advanced Transistor Structures

Novel Transistor Structures

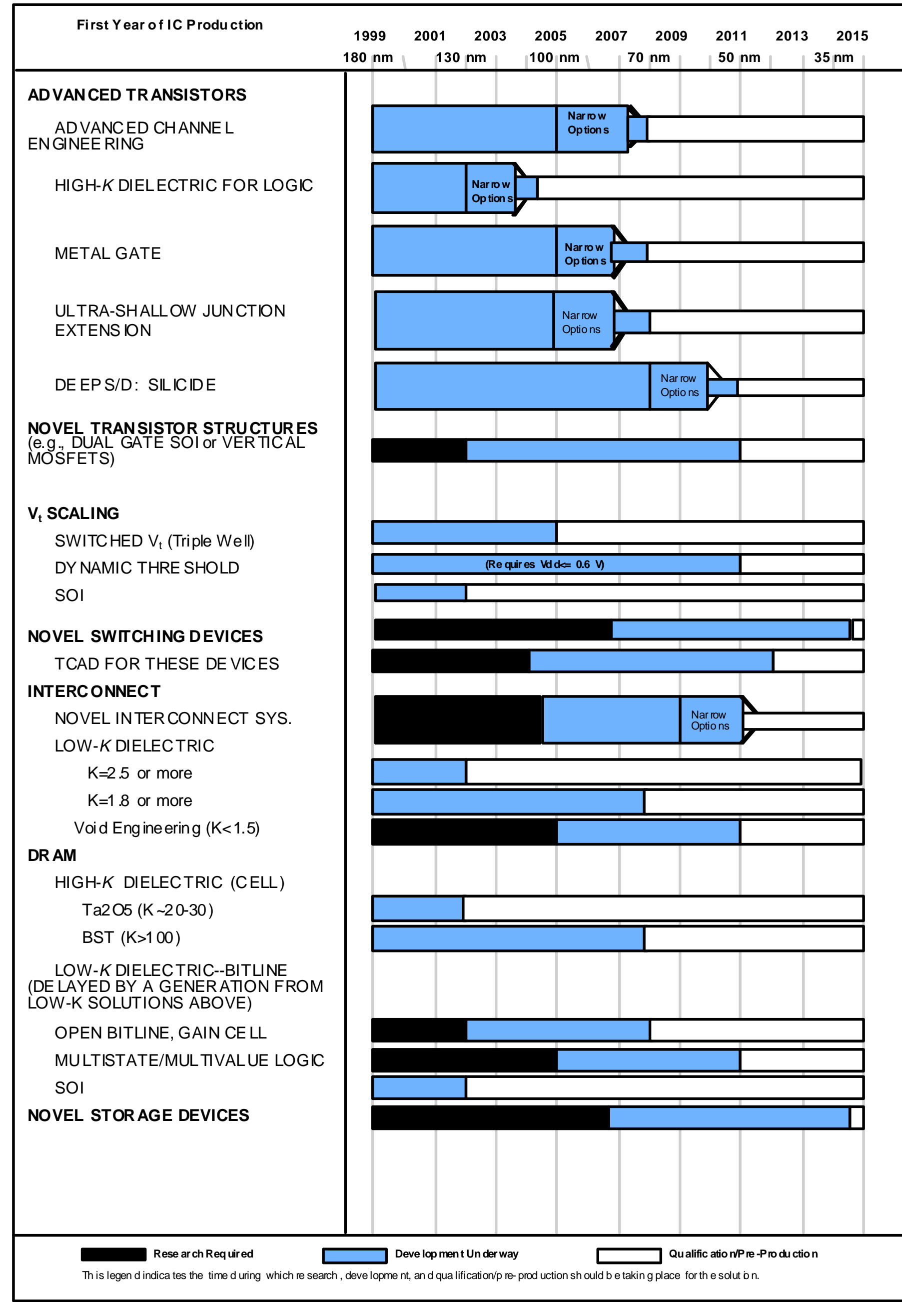
Vt Scaling

Novel Switching devices

Interconnect

DRAM

Novel Storage Devices



Analog, Mixed Signal and RF Requirements

1	Year of Introduction "Technology Node"	1999 180 nm	2000 165nm	2001 150nm	2002 130 nm	2003 120nm	2004 110nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
2	Mininimum Digital Supply Voltage (V)	1.8-1.5			1.5-1.2		1.2-0.9		0.9-0.6	0.6-0.5	0.5-0.3
3	Mininimum Analog Supply Voltage (V)	3.3-2.5	2.5-1.8						1.8-1.5		1.5
4	RF Frequency (GHz)	0.9-2.5	0.9-10						0.9-10	0.9-100	

- **Analog and mixed signal difficulties are compounded at low voltages.**
  - **Excessive analog power dissipation under reduced signal swing conditions must be addressed.**

- **Precision passive elements may require unique materials and more complex fabrication techniques.**

- **Crosstalk and noise issues will dominate at low voltages, high density, and high frequency.**

Potential Solutions

Active devices

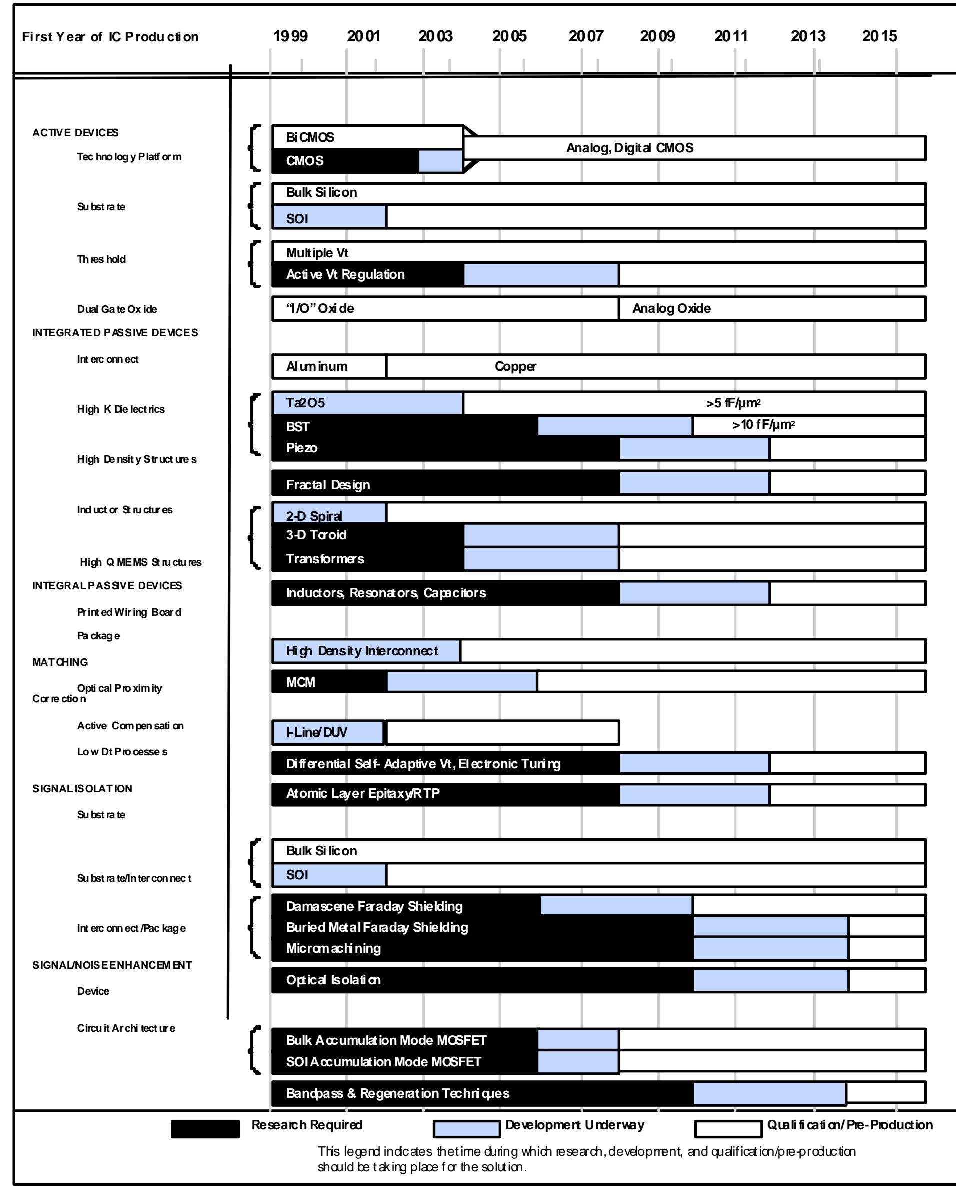
Integrated Passive devices

Integral Passives

Matching

Signal Isolation

Signal/Noise enhancement



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Device Reliability

- Reliability Infrastructure is not prepared for new material introductions

- Lead Time for new technologies is long for reliability evaluations

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Reliability Needs

Table 17 Reliability Short Term Technology Requirements

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Customer Reliability Expectations (@85°C Junction Temperature)								
Early Failures (ppm) (First 4000 operating hours)	50-2000	50-2000	50-2000	50-2000	50-2000	50-2000	50-2000	
Long Term Reliability (FITs = Failures in 1E9 hours) (5-10 Years)	10-100	10-100	10-100	10-100	10-100	10-100	10-100	
Soft Error Rate (FITs)	1000	1000	1000	1000	1000	1000	1000	
Relative Failure Rate per Transistor (normalized to 180nm)	1	1	1	.62	.62	.62	.34	
Relative Failure Rate per m of Interconnect (normalized to 180nm)	1	1	1	.51	.51	.51	.34	
System on A Chip Reliability Prediction	Logic & Memory			MicroMa chine			Micro Optics	
Failure Analysis Cycle Time (days)	1-12	1-12	1-12	1-10	1-10	1-10	1-10	FAILURE LOCA-TION

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Note: Reliability requirement includes chip and package failures. Additional parameters (e.g., temperature cycling and humidity) need to be specified for package reliability.

Table:Title (11 pt) - Table # TWG Long Term Technology Requirements Title

YEAR OF INTRODUCTION	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Customer Reliability Expectations (@85°C Junction Temperature)				
Early Failures (ppm) (First 4000 operating hours)	50-2000	50-2000	50-2000	
Long Term Reliability (FITs = Failures in 1E9 hours) (5-10 Years)	10-100	10-100	10-100	
Relative Failure Rate per Transistor (normalized to 180nm)	.16	.07	.03	
Relative Failure Rate per m of Interconnect (normalized to 180nm)	.18	.10		
Soft Error Rate (FITs)	1000	1000	1000	
System on A Chip Reliability Prediction	Micro Biological			
Failure Analysis Cycle Time (days)	1-10	1-10	1-10	

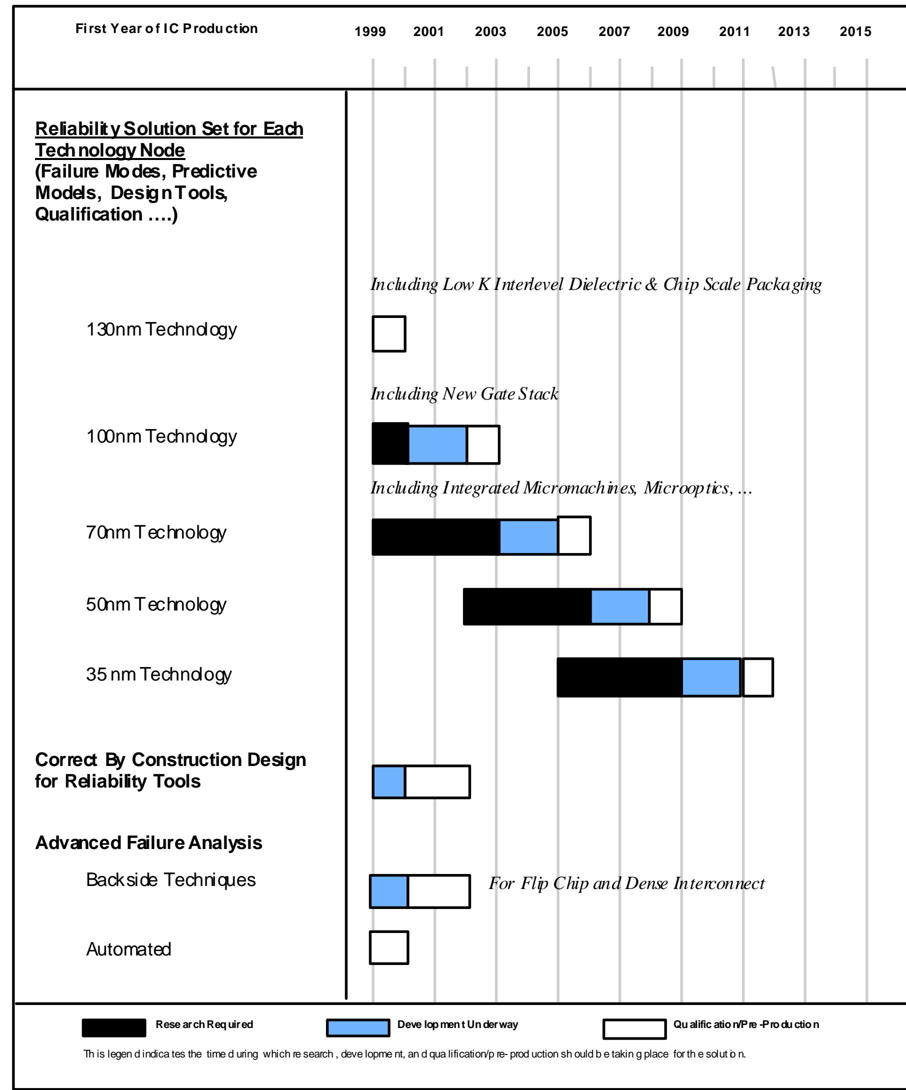
Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Potential Solutions

Reliability solutions need ~6 year lead

Correct by Construction Design for reliability tools

Advanced Failure analysis



Other Issues:

Vdd Scaling Choice:

- V_{dd} Chosen to limit maximum field in gate oxide and dynamic power dissipation.

SOC

- Need Table of complexity (# of masks) for technology combinations

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Complexity table for SOC applications

Cost of adding technology in units of mask levels	Logic	SRAM	Flash	DRAM	CMOS RF	FPGA	MEMS	FRAM	Chem. Sensors	Electro-Optical	Biological
Logic	0										
SRAM	1-2	0									
Flash	4	3-4	0								
DRAM	4-5	3-4	?	0							
CMOS RF	?	?	?	?	0						
FPGA	?	?	?	?	?	0					
MEMS	?	?	?	?	?	?	0				
FRAM	?	?	?	?	?	?	?	0			
Chem. Sensors	?	?	?	?	?	?	?	?	0		
Electro-Optical	?	?	?	?	?	?	?	?	?	0	
Biological	?	?	?	?	?	?	?	?	?	?	0
?	?	?	?	?	?	?	?	?	?	?	?
?	?	?	?	?	?	?	?	?	?	?	?
?	?	?	?	?	?	?	?	?	?	?	?
?	?	?	?	?	?	?	?	?	?	?	?

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Summary

•Gate stack and new material issues will limit device performance

•Vdd scaling is an issue for analog, RF and digital technologies

•New material introductions will increase reliability risks

•SOC integration increasing complexity of processing

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