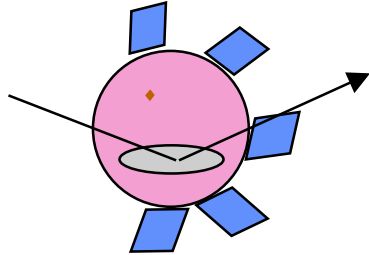
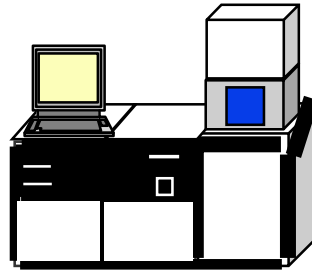


IN-SITU



IN-LINE



OFF-LINE / AT-LINE



1999 Metrology Roadmap

Europe

**Alec Reader (Philips)
Patrick Dussouillez (ST Microelectronics)**

Japan

Fumio Mizuno (Hitachi)

Taiwan

**Henry Ma (EPISIL)
George Yen (ProMOS)**

US

**Bob Scace (NIST)
Alain Diebold (SEMATECH)**

International Technology Roadmap for Semiconductors

ITRS

Work in Progress --- Not for Publication

Outline

- **Scope and Critical Challenges**
- **Overview Messages**
- **Lithography Metrology**
- **Front End Processes**
- **Interconnect Metrology**
- **Integrated Metrology**
- **Risks**

In-line Metrology usage

400 + step Process Flow

steps

~25 Overlay

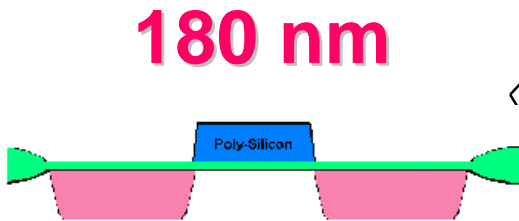
~20 CD

<20 Defect/Particle

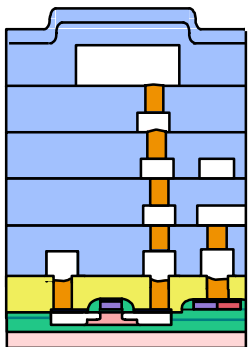
~ 6 { Poly Si Control
ILD Thickness
Contact Etch
ILD Etch Control
Metal Thickness

~ 4 Implant Dose

1 Gate Ox Thickness



6 metal levels



Metrology Roadmap Topics

- **Microscopy (Imaging)**
- **CD & Overlay**
- **Film Thickness and Profile**
- **Materials and Contamination Analysis**
- **Dopant Profile (Dose/Junct./Shape)**
- **In-Situ Sensors for Process Control**
- **Reference Materials**
- **Correlation of Physical and Electrical Measurements**

Difficult Challenges > 100 nm / Before 2005

- Metrology integration for in-situ and in-line metrology tools
- Particles, oxygen, and metallics detection at levels of interest for starting materials and reduced edge exclusion for metrology tools
- Measurement of the frequency-dependent dielectric constant of low k interconnect materials at 5x to 10x base frequency.
- Control of high-aspect ratio technologies such as Damascene challenges all metrology methods.
- Measurement of complex material stacks

Additional Difficult Challenges < 100 nm / Beyond 2005

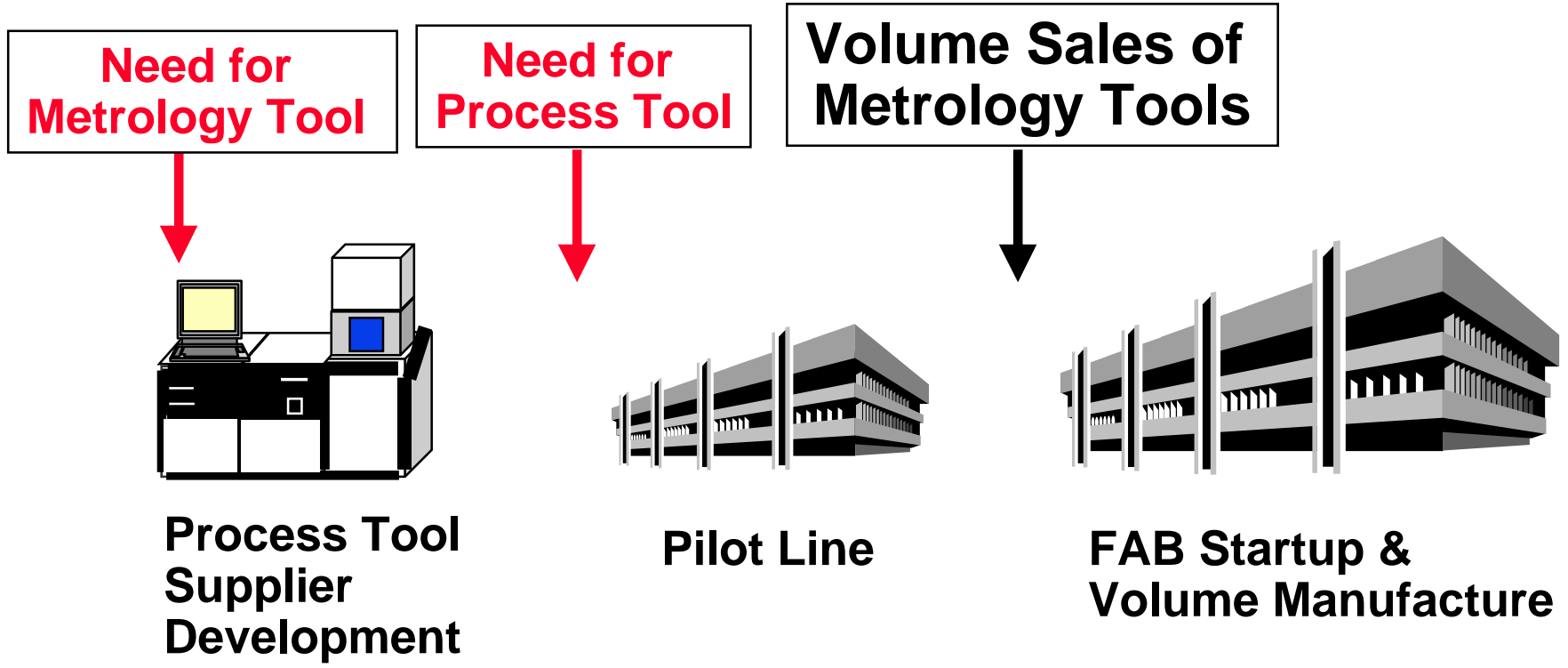
- Microscopy for critical dimension measurement, overlay, defect detection, and analysis
- Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials
- Statistical limits of sub-70 nm process control
- 3-D dopant profiling
- Production worthy, physical inline metrology for transistor processes that provides SPC required to achieve consistent electrical properties

Overview Messages

- Infrastructure
- Requirements have too much RED
- Challenge Associated with Precision Requirements
- Microscopy Development
- Interfacial Measurements

Metrology Timing vs Infrastructure Capabilities

Gap in long term R&D Spending + Development Funding Model



Typical Potential Solutions Time Line for Process Tool

Too Many Metrology Technology Requirements are RED

Table 61b Long Term Metrology Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	2008 70 nm	2011 50 nm	2014 35 nm	DRIVE R
Wafer Gate CD Control*	4.0	3.0	2.0	
Wafer Dense Line CD Control*	7.0	5.0	3.5	
Wafer Contact CD Control*	8.0	5.5	4.0	
Wafer CD Metrology Tool Precision* P/T=.2 for Isolated Lines**	0.8	0.6	0.4	
Wafer CD Metrology Tool Precision* P/T=.2 for Dense Lines**	1.4	1.0	.07	
Wafer CD Metrology Tool Precision* P/T=.2 for Contacts**	1.6	1.1	0.8	
Maximum CD Measurement Bias (in percent)	10	10	10	
Mask CD Control Isolated Lines*	7	5	3.3	
Mask CD Control Dense Lines*	11	8	5.6	
Mask Contact Area Control Normalized to v of Area*	12	9	6.4	
Mask CD Metrology Tool Precision* P/T=.2 for Isolated Lines**	1.4	1.0	0.7	
Mask CD Metrology Tool Precision* P/T=.2 for Dense Lines**	2.2	1.6	1.1	
Mask Area Metrology Tool Precision for Contact Normalized to v of Area - v of Target for P/T=.2	1.6	1.8	1.3	
Wafer Overlay control (nm)	25	20	15	
Wafer Overlay Output Metrology Precision (nm, 3 sigma)* P/T=.1	2.5	2.0	1.5	
Final Mask Image Placement	16	12	9	
Mask Image Placement Metrology Precision P/T=.1	1.6	1.2	0.9	
Mask Phase (in degrees)	1			
Phase Metrology Precision P/T=.2 (in degrees)	2			
Variation in Attenuated mask Film Transmission % of Deviation from Nominal (in percent)	4			
Transmission Metrology Precision % of Nominal Attenuated PSM Transmission P/T=.2 (in percent)	8			

* All precision values are 3 sigma in nm and include metrology tool matching.

** Measurement tool performance needs to be independent of line shape, line materials, and density of lines.



Solutions Exist

Solutions Being Pursued

No

Known



Examples of Precision Requirements

Year of First Product Shipment Technology Generation	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2003 100 nm	Driver
DRAM 1/2 Pitch	180	165	150	130	120	110	100	D½
Logic Isolated Lines	140	120	100	85	80	70	65	M Gate

Microscopy and Lithography

Microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	MPU
Wafer Gate CD Control*	13	12	10	8.5	8	7	6.3	MPU
Wafer CD Tool Precision* P/T=.2 Isolated Lines**	2.6	2.4	2.0	1.8	1.6	1.4	1.3	MPU
Mask Area Metrology Tool Precision P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2	MPU

Front End Processes

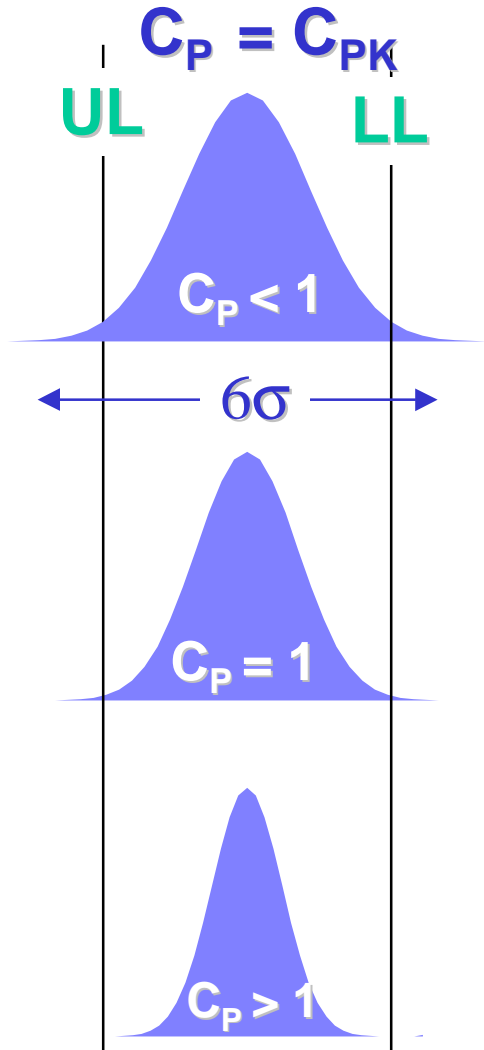
Logic Dielectric Thick Precision 1σ (nm) ^B	0.0025	0.0024	0.0021	0.0017	0.0016	0.0013	0.0012	MPU Gate
2D Dopant Profile Spatial Resolution (nm)	3	3	3	2	2	2	1.5	MPU Gate

Interconnect

Barrier layer Thick (nm)	23	19	16	13	11	7	3	MPU
process range (± 3σ)	20%	20%	20%	20%	20%	20%	20%	
Precision 1σ (nm)	0.08	0.06	0.05	0.04	0.035	0.02	0.01	

Effect of P/T on Process $C_p = (UL-LL) / 6 \sigma$

If Distribution is Centered



EFFECT OF MEASUREMENT PRECISION (P/T RATIO) ON C_p AS MEASURED

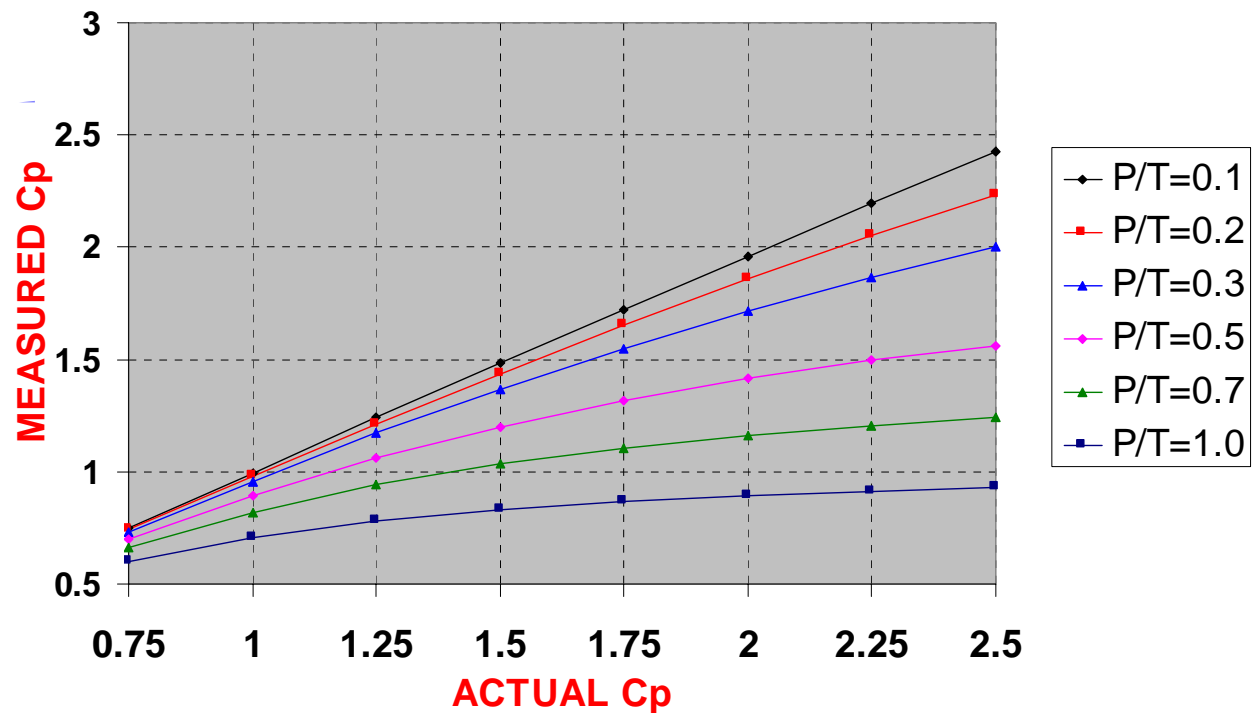


Chart from Jerry Schlesinger, TI

International Technology Roadmap for Semiconductors



Work in Progress --- Not for Publication

Domestic vs International Points of View

- Precision vs Accuracy
- Precision US Centric
- Accuracy and Precision Global Centric

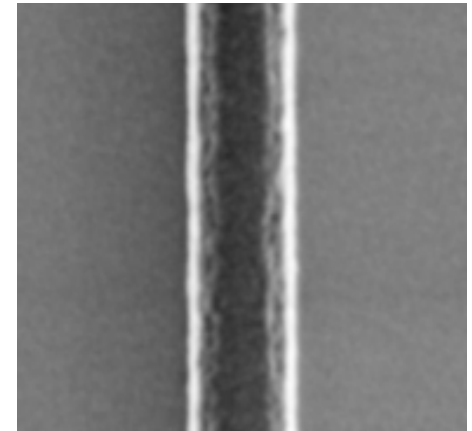
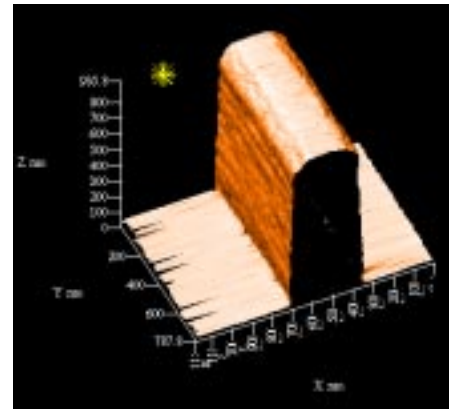
Microscopy

Issues:

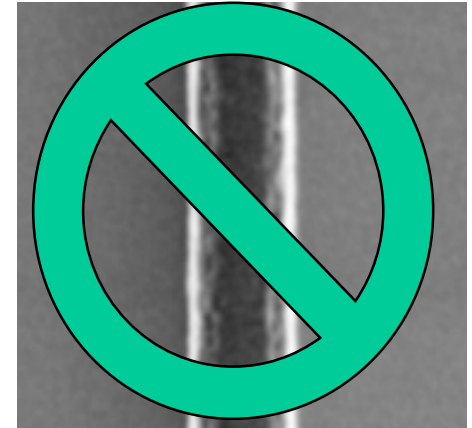
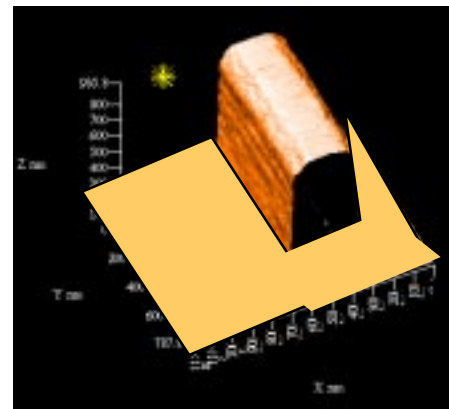
CD and Detection require new microscopy

- SEM with resolution required for sub 100 nm has **poor Depth of Focus**
- 3D Information Required
- Improved throughput required

SEM



Today : Depth of focus > 1 micron

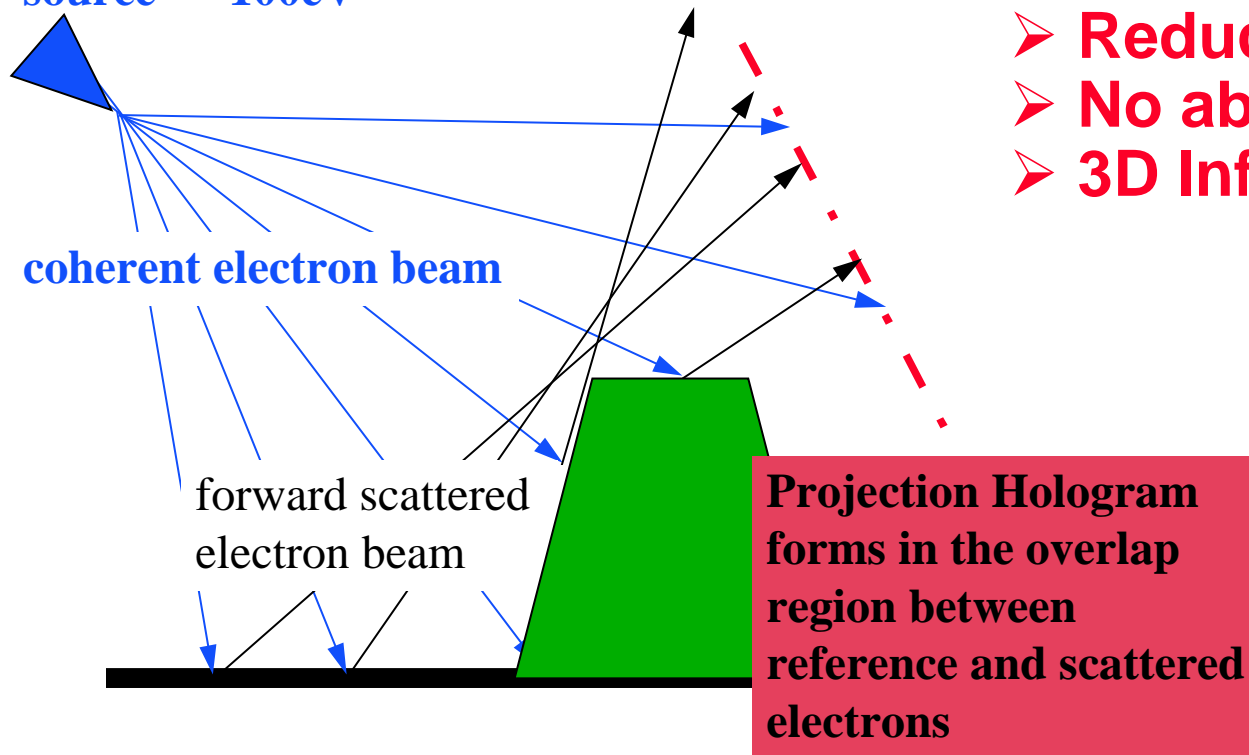


With Future Resolution:
Depth of focus << 1 micron

Microscopy and Lithography Metrology

Long Term Research and Development

Nanotip Field Emission
source ~ 100eV



Electron Holography

- Low damage
- Reduce Charging
- No aberration/diffraction
- 3D Information

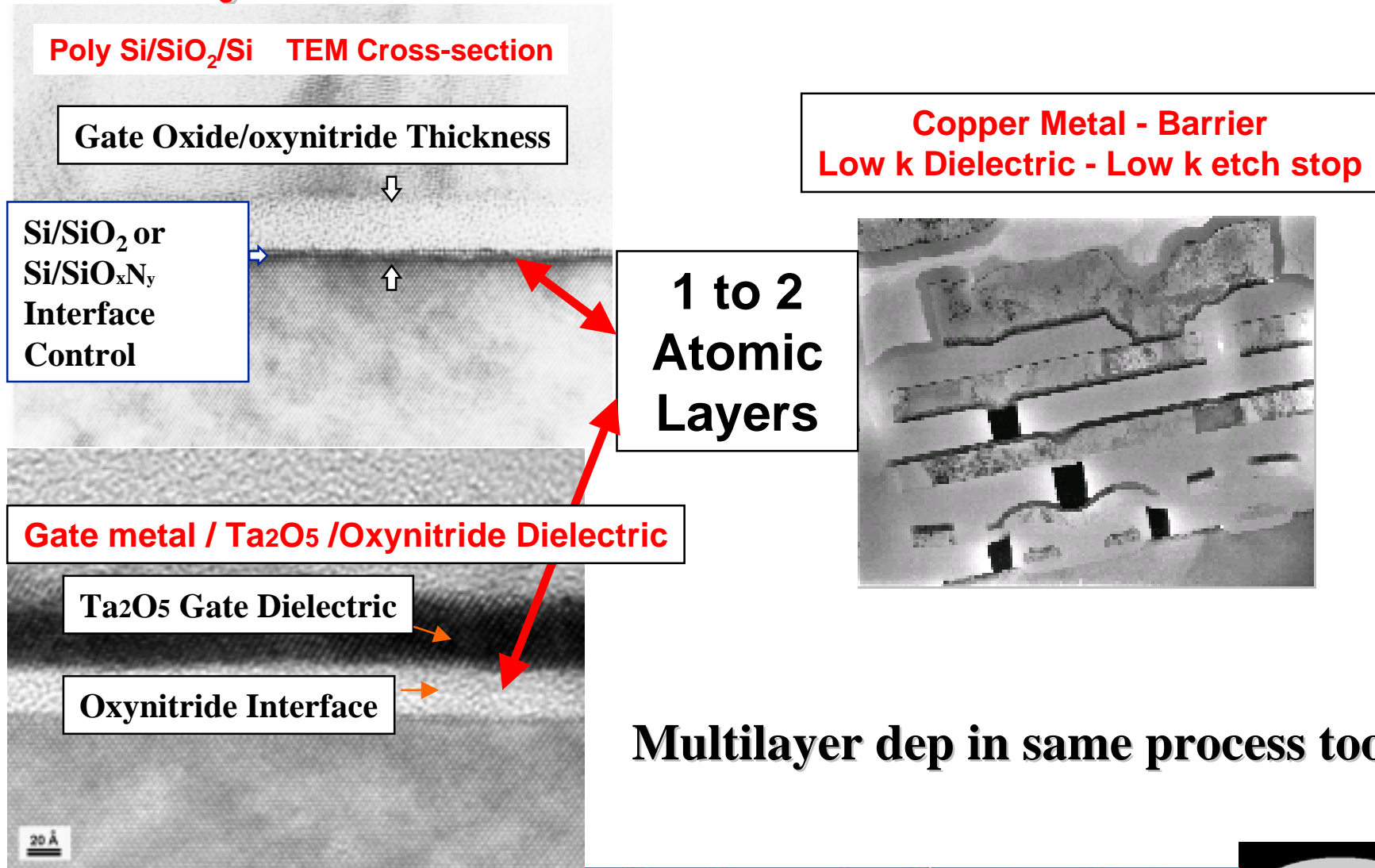
David Joy, Univ. of TN

International Technology Roadmap for Semiconductors

Work in Progress --- Not for Publication

ITRS

Interfaces - Control challenge for today and the future (*in-situ* ?)



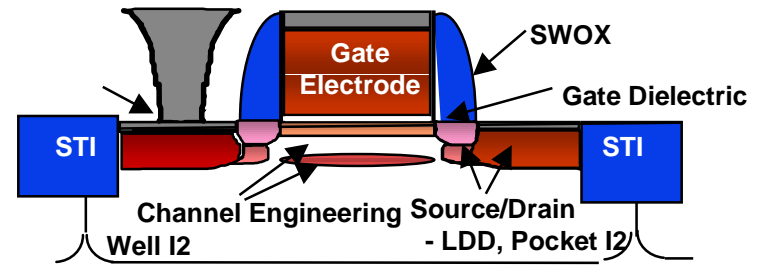
Multilayer dep in same process tool

Changes from 1997 NTRS

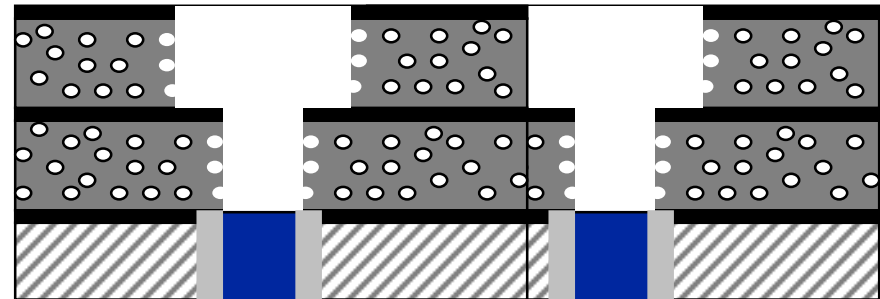
- Mask Metrology Expanded
- New needs from 157 nm Lithography
- Sensors now a part of Integrated Metrology

Lithography Metrology

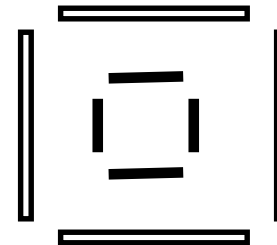
Gate Length Control



Damascene Line Width

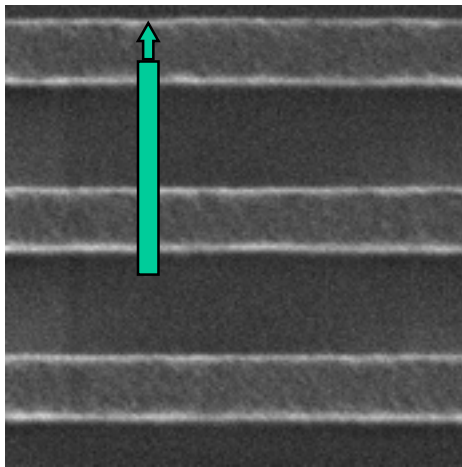


Overlay Control



Lithography Metrology

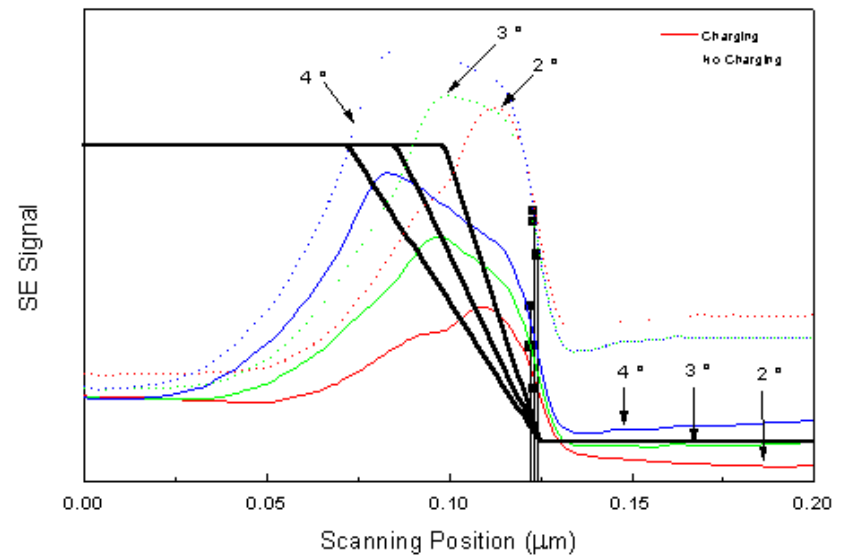
Improve CD-SEM thru 100 nm node



**top down
CD-SEM**

KRISS

Isolated (Sidewall Angle)



Signal → CD Value

NEED: Determine CD from Fundamental Model

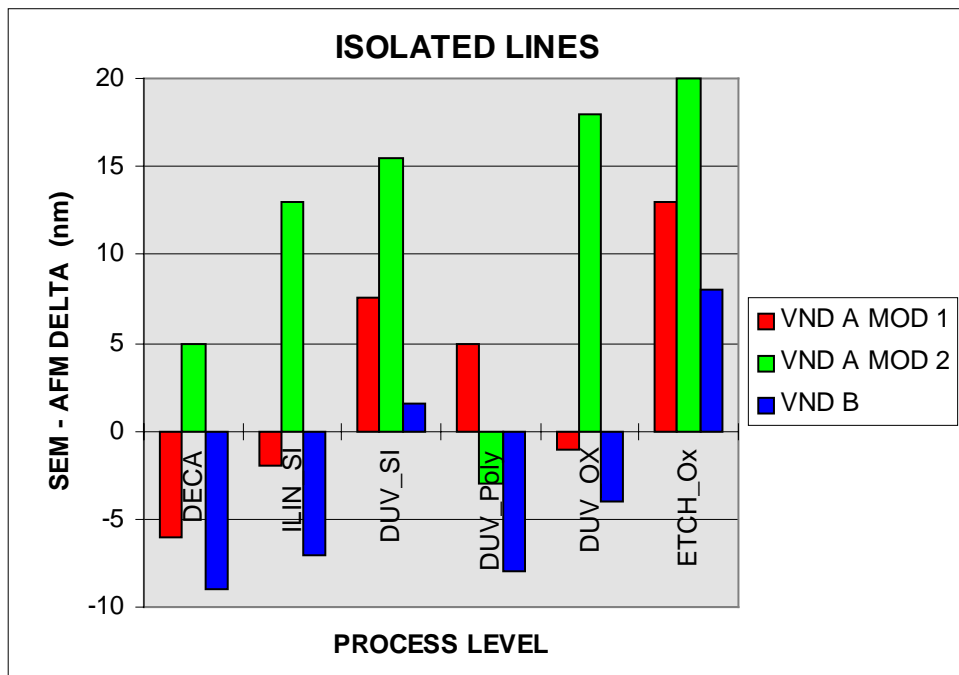
International Technology Roadmap for Semiconductors



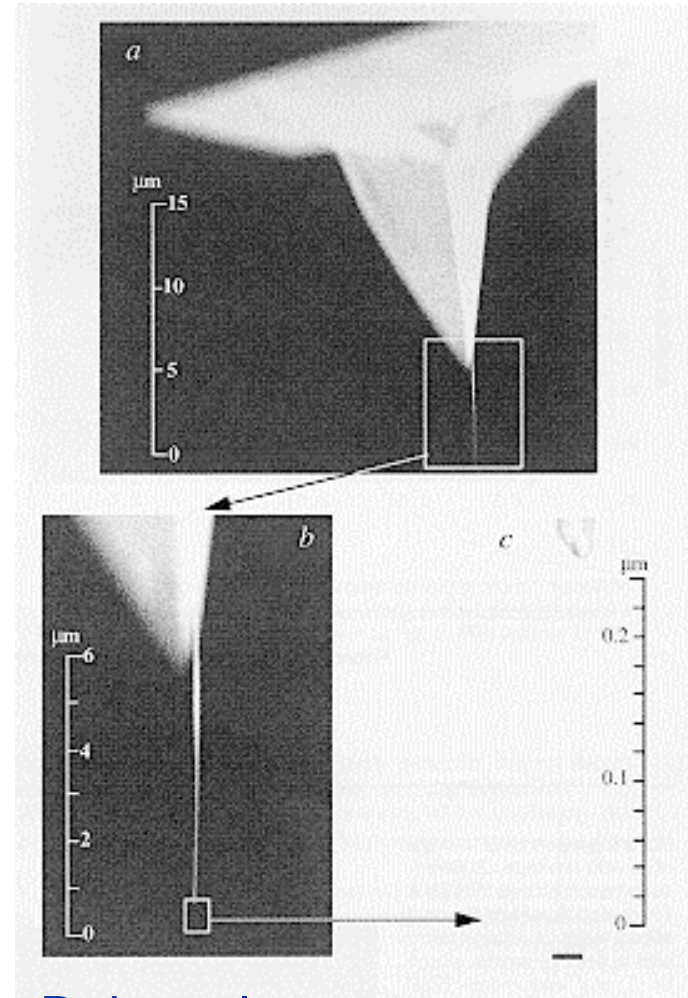
Work in Progress --- Not for Publication

Process Level Dependence of CD SEM

Calibration requires New Probe tips for CD-AFM

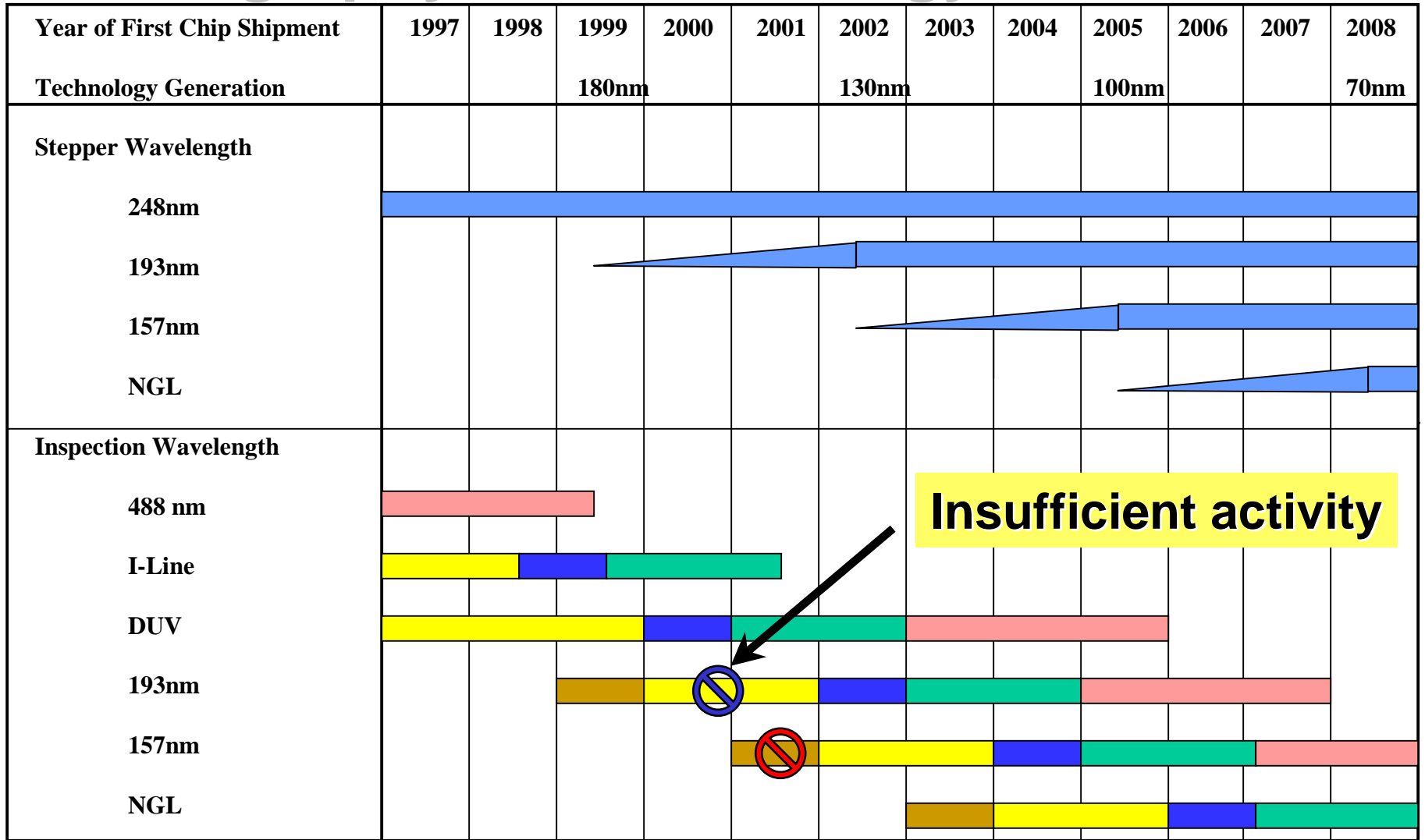


H. Marchman



Dai, et al.,
Nature **384**, 147 (1996)

Lithography Mask Metrology



Wally Carpenter

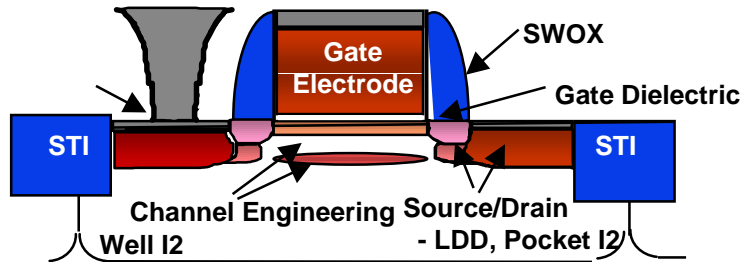
International Technology Roadmap for Semiconductors



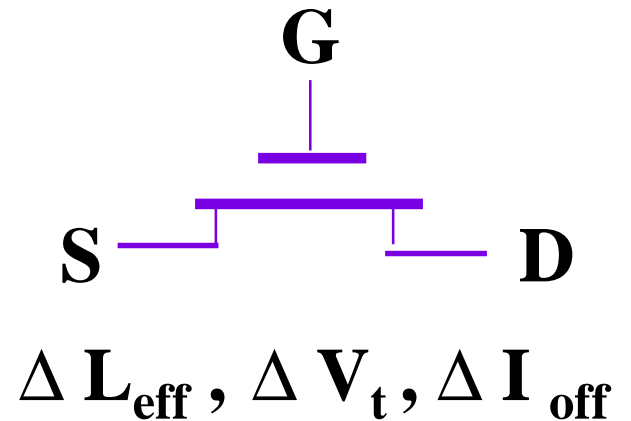
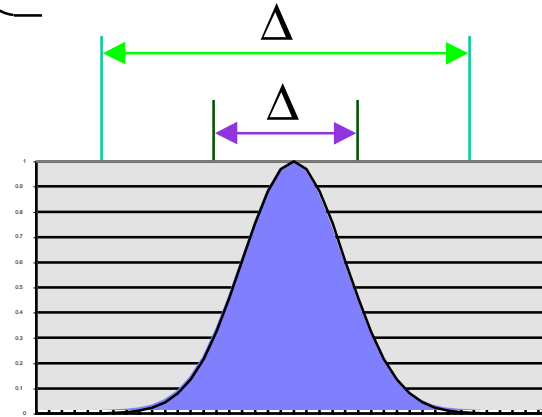
Work in Progress --- Not for Publication

Front End Processes

(Transistor & Capacitor Process) Metrology



Δt_{oxide} , ΔL_g ,
 $\Delta \text{dose/junction}$

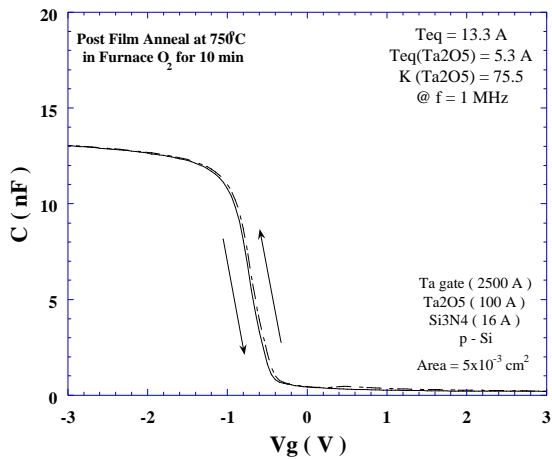


**Electrical Measurement requires
 fabrication of a transistor.**

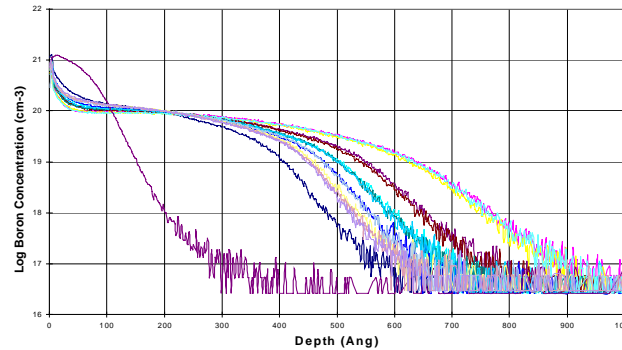
**Will physical metrology be able to adequately
 control critical processes at 100 nm and beyond ?**

Transistor Process Metrology Challenges

New Materials & Ultra Shallow Junctions



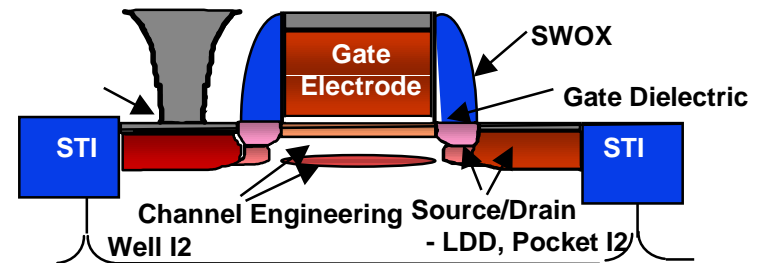
SIMS Profile
Boron Concentration vs Junction Depth Xj



Gate metal / Ta₂O₅ / Oxynitride Dielectric

Ta₂O₅ Gate Dielectric

Oxynitride Interface

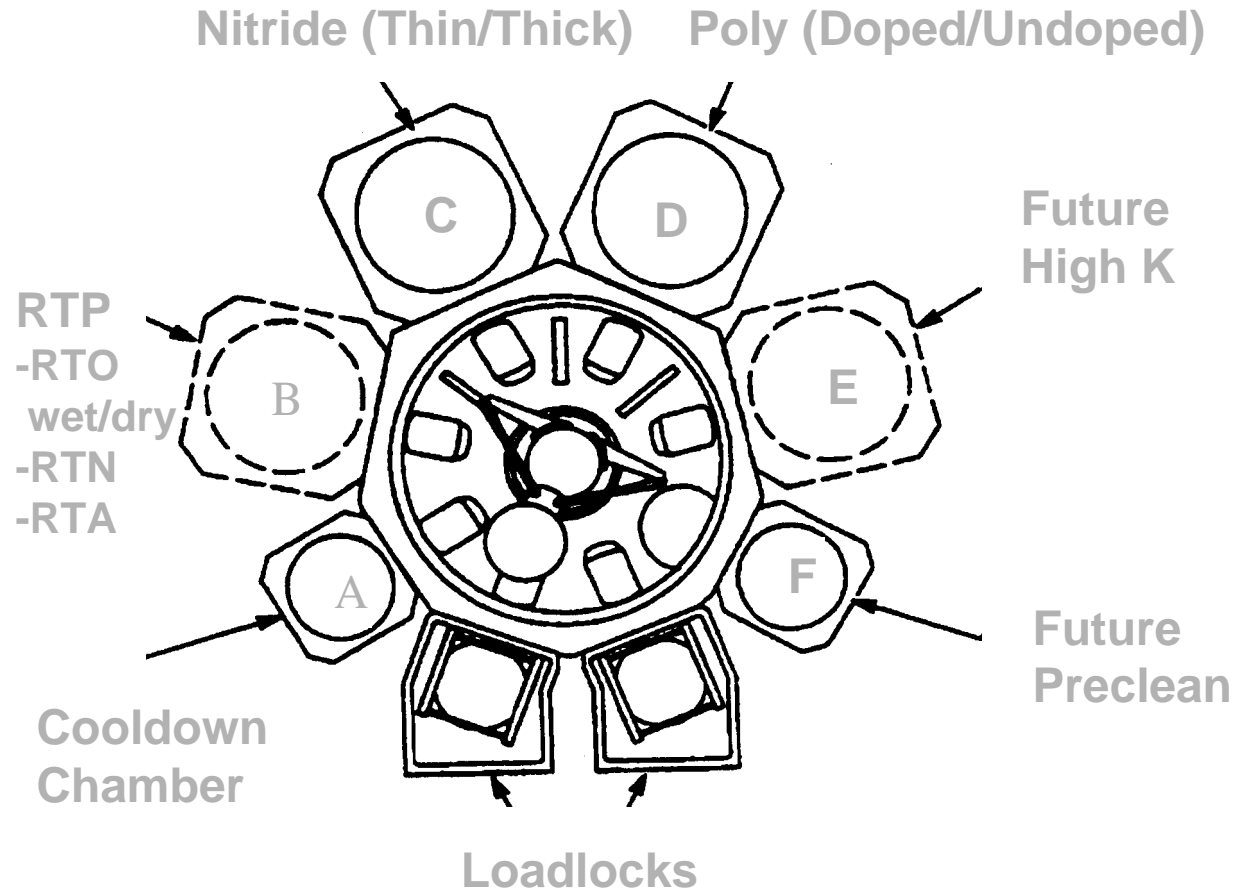


Front End Process Metrology

In-Situ Needs vs Integrated Metrology Trend

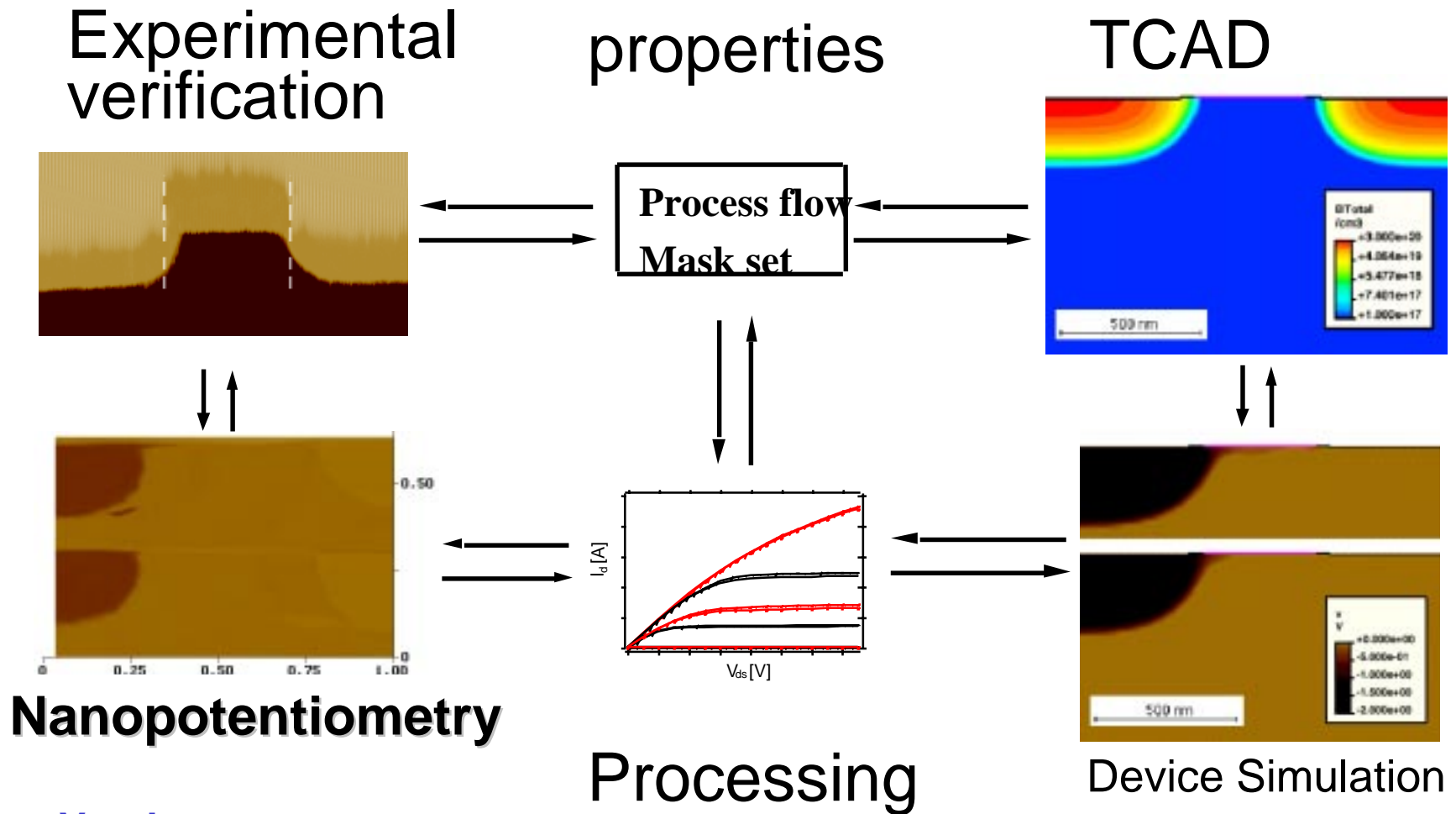
**Clustered
gate dielectric
& electrode**

**e.g., Metal
Gate forces in-
situ metrology
for dielectric**



2D Dopant Profiling

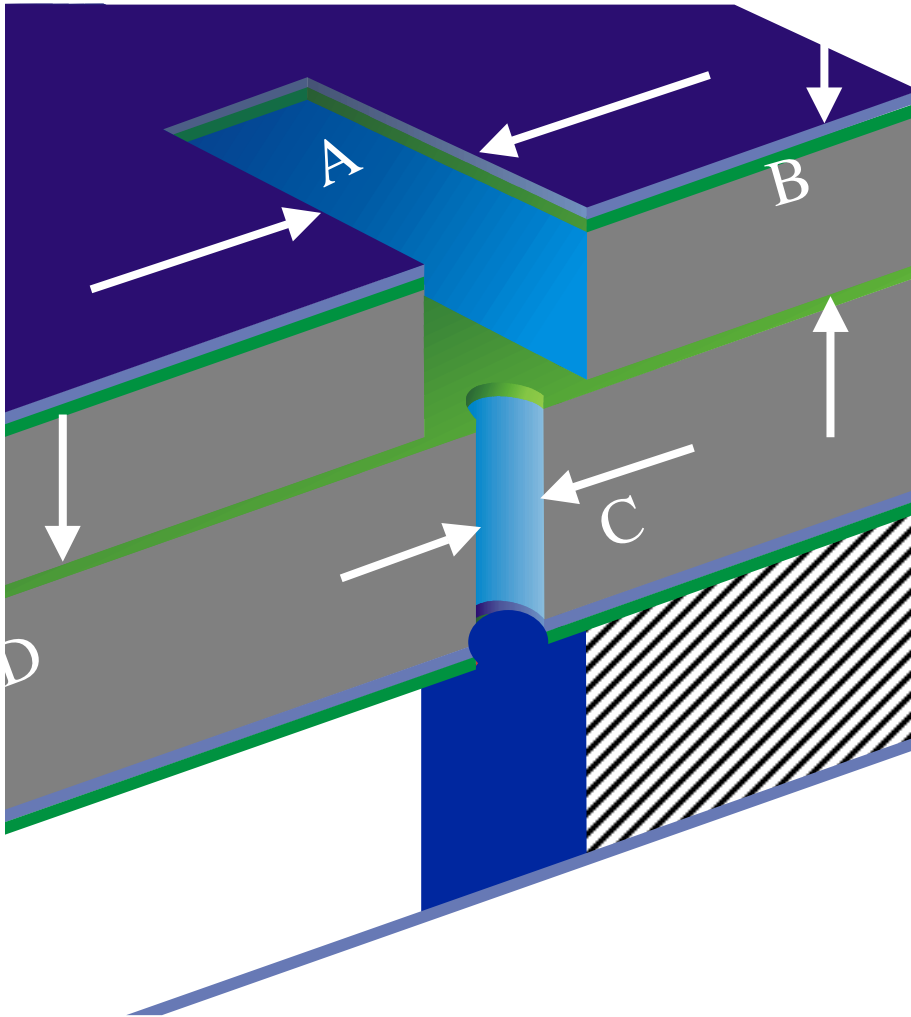
Issue : Spatial Resolution



imec - Vandervorst

Interconnect Metrology

New Materials and Processes



Copper/barrier Film Thickness

100 micron diameter size test areas
by acoustic

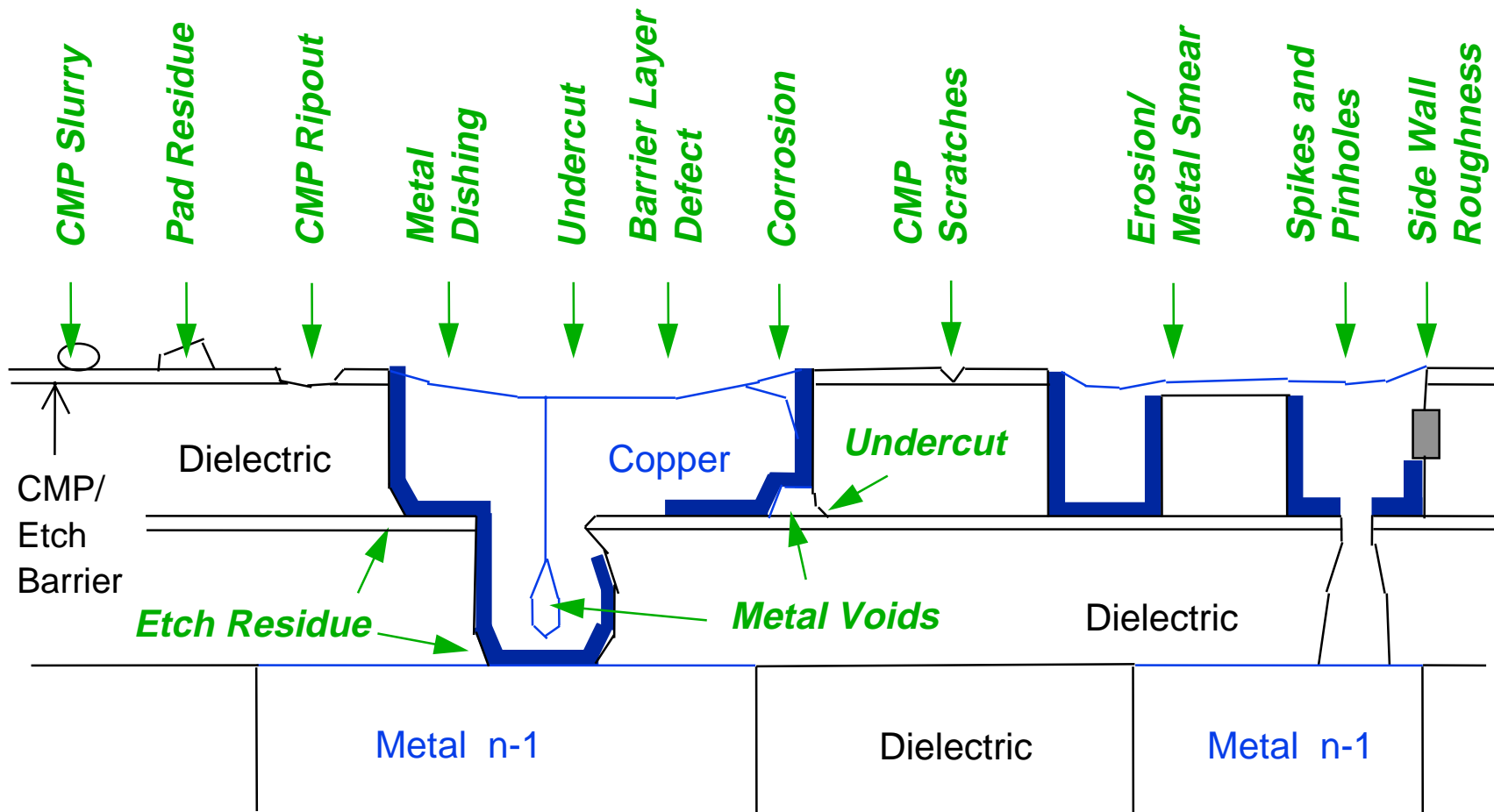
Low k Dielectrics

High frequency dielectric testing
needs development for > 40 GHz

Need optical models for porous
materials

Developing Physical Properties and
Delamination testing

Systematic Failure Modes in Dual Damascene Processes



David Jensen - AMD/SEMATECH

International Technology Roadmap for Semiconductors



Work in Progress --- Not for Publication

Depth of Focus Requirements for Litho

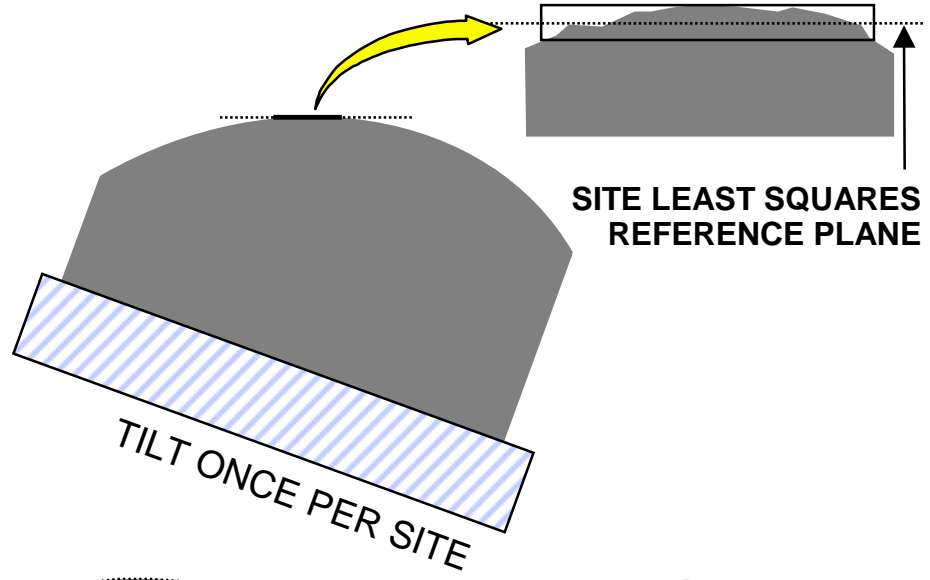
CMP Metrology tool should measure what litho tool “sees”

Full Field Steppers

SEMI STD

Site Frontside
least-sQuared
site reference

Range = SFQR
Deviation = SFQD

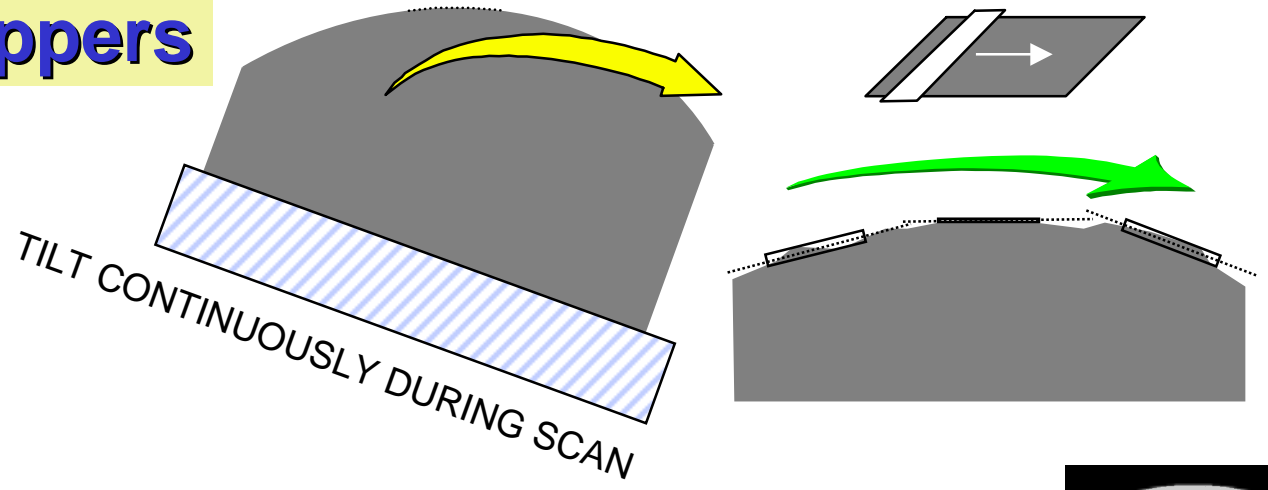


Scanning Steppers

SEMI STD

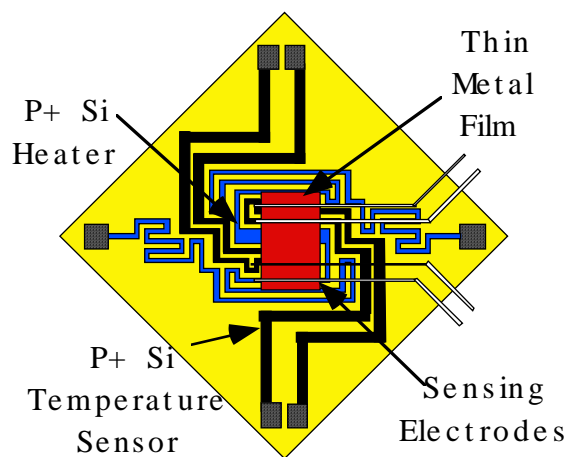
Site Frontside
Scanning*
site reference

Range = SFSR
Deviation = SFSD

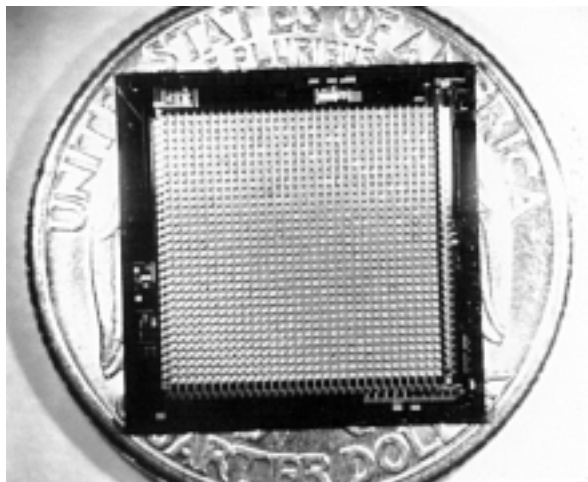


SENSOR based Integrated Metrology

MEMS : Sensor Technology of the Future



A MONOLITHIC DETECTOR FOR PROCESS GAS PURITY



Infrared Imager for RTP

GOAL:

measure temp & uniformity

$\pm 1^{\circ}\text{C}$ to 1000°C

SENSOR based Integrated Metrology

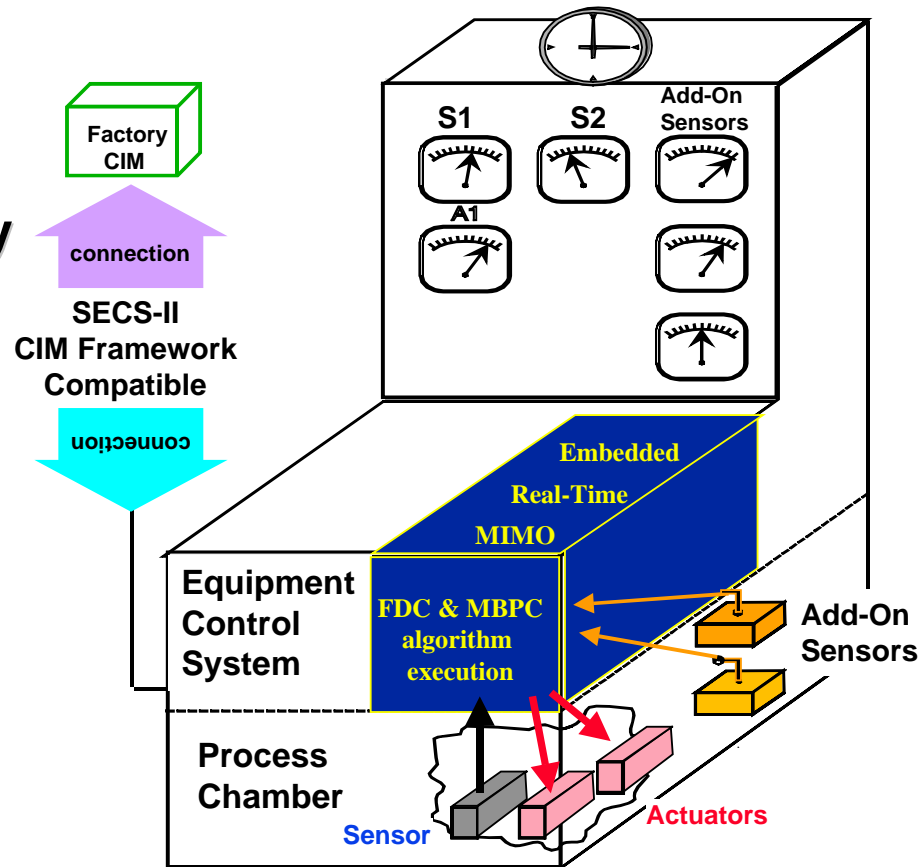
Comments on :

Advanced Process Control - Advanced Equipment Control

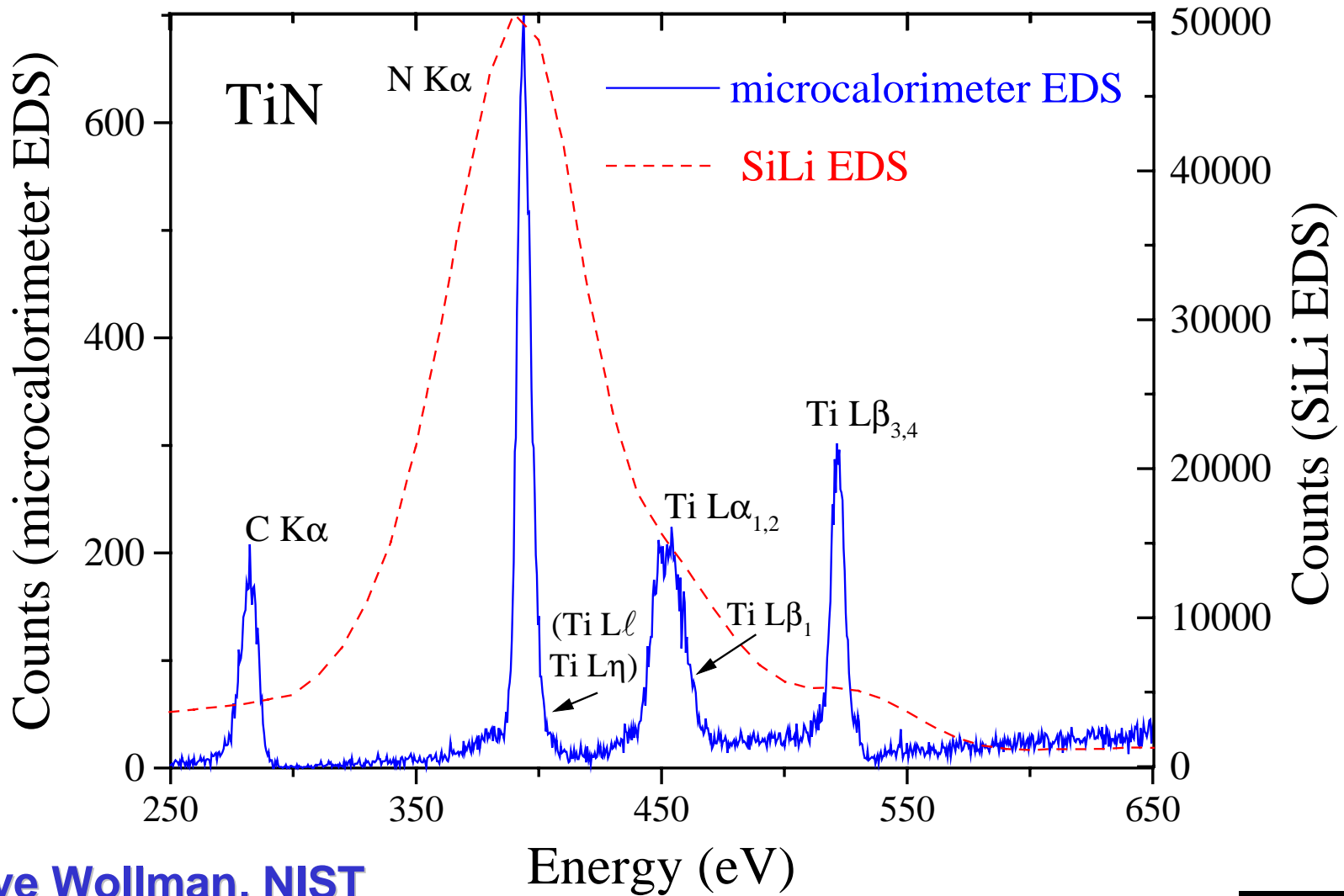
- **AEC/APC GOAL :**
model based predictive control
based on process and metrology
models using in-situ and in-line
measurements

➤ **Momentum ?**

➤ **Now suppliers advocate
Integrated Metrology**



Microcalorimeter EDS vs EDS



Dave Wollman, NIST

International Technology Roadmap for Semiconductors

Work in Progress --- Not for Publication



Accelerated MPU Gate impacts all GAPS

Key Drivers \Leftrightarrow GAPS

Shrinking Dimensions	\Leftrightarrow	< 100 nm Microscopy for CD, Detection
	\Leftrightarrow	High Aspect Ratio Capability
	\Leftrightarrow	Metrology with adequate precision and correlation w/electrical tests
	\Leftrightarrow	Process Control for Processes at Statistical Limits
	\Leftrightarrow	3-D Dopant Profiling

New Materials in Transistor, Capacitor, and Interconnect	\Leftrightarrow	Measure High Frequency Dielectric Constant
	\Leftrightarrow	Measurements and standards for new materials stacks

RISKS

- **Near Term Lack of Metrology Tools for accelerated Technology Cycle**
- **Important New Approaches need additional funding for long term R+D**
(ex. - Electron Holography, arrayed AFM and SEM)
- **Long time between R&D investment in metrology tools and sales to repay that investment**
- **Lack of methodology for Statistically Limited Processes and appropriate metrology**
- **Shrinking scribe lines limit test areas needed for adequate measurement precision**

Background

Accelerated MPU Gate impacts all GAPS

Key Drivers \Leftrightarrow GAPS

Shrinking Dimensions	\Leftrightarrow	< 100 nm Microscopy for CD, Detection
	\Leftrightarrow	High Aspect Ratio Capability
	\Leftrightarrow	Metrology with adequate precision and correlation w/electrical tests
	\Leftrightarrow	Process Control for Processes at Statistical Limits
	\Leftrightarrow	3-D Dopant Profiling

New Materials in Transistor, Capacitor, and Interconnect	\Leftrightarrow	Measure High Frequency Dielectric Constant
	\Leftrightarrow	Measurements and standards for new materials stacks

Metrology Roadmap Topics

- **Measurements for Process Facing Statistical Limits**
- **Microscopy**
- **Lithography Metrology**
- **Front End Process Metrology**
- **Interconnect Metrology**
- **Materials and Contamination Characterization**
- **Reference Materials**
- **Integrated Metrology**

1999 Metrology Members

RCG Advocate - Bob Scace NIST

Dick Brundle	Applied Materials	Lu Nguyen	National
Murray Bullis	SEMI/ FEP	Herschel Marchman	Univ. South Fl.
Alain Diebold	SEMATECH	Kevin Monahan	KLA
Charles Evans	Chs. Evans & Assoc.	Laura Oliphant	Intel
James Greed	VLSI Standards	Noel Poduje	ADE
Joe Griffith	Lucent	Gary Rubloff	Univ. Maryland
David Joy	Univ. of Tennessee	Jerry Schlesinger	Texas Insts.
Mike Kelly	Sandia	Gil Shelden	Int'l SEMATECH
Stephen Knight	NIST	Brad van Eck	SEMATECH
		Ken Wise	Univ. of Michigan

Alternative Metrology Member

Richard Hockett	Charles Evans & Assoc.
Brad Scheer	VLSI Standards

1999 Metrology Advisors

David Alles
Marlin Braun
Chi Shih Chang
Alain Deleporte
Joe Glaney
Andrew Gurnell
James Harper
John Hauser
Clive Hayzelden
Rudi Hendel
Howard Huff
Dan Herr
Don Kania
Sheldon Moll
David Perloff
Michael Postek
Gay Samuelson
David Seiler
Richard Spanier
Peter Zeitzoff

Tencor
Physical Electronics
SEMATECH
IBM France/ Int'l SEMATECH
Veeco
Bio-RAD
VEECO Instruments
NCSU
KLA - Tencor
Applied Materials
SEMATECH
SRC
Veeco
Amray, Inc
Voyan Tech
NIST
Intel
NIST
Rudolph Tech
SEMATECH

Cross-cut TWG contacts

Factory Integr.

Murray Bullis

SEMI

FEP

David Seiler

NIST

Interconnect

Dick Brundle + Sam Broydo

Applied

Lithography

Gil Shelden

International SEMATECH

Packaging

Lyu Nguyen

National

Bob Werner

Packaging TWG Chair

Table 61(a) Metrology "SHORT TERM" Technology Requirements

<i>Year of First Product Shipment Technology Generation</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2003 100 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch</i>	180	165	150	130	120	110	100	D½
<i>Logic Isolated Lines</i>	140	120	100	85	80	70	65	M Gate
Microscopy								
In-line, nondestructive microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	M Gate
Maximum aspect ratio / diameter (nm) (DRAM contacts)	6.3 200	6.7 175	7.1 160	7.5 140	8.0 130	8.5 120	9 110	D½
Materials and Contamination Characterization								
Real Particle Detection limit (nm) ^B	70	60	50	43	40	35	30	M Gate
Minimum Particle size for compositional analysis (on patterned wafers) (nm)	48	40	33	28	27	23	22	M Gate
Surface detection limits (Al, Zn)/ (Ni, Fe, Cu, Na, Ca) (atoms/cm ²) with Signal to Noise of 3:1	2.5 x 10 ⁹ 1 x 10 ⁹	2.5 x 10 ⁹ 9 x 10 ⁸	2 x 10 ⁹ 8 x 10 ⁸	1.5 x 10 ⁹ 7 x 10 ⁸	1.5 x 10 ⁹ 7 x 10 ⁸	1 x 10 ⁹ 6 x 10 ⁸	1 x 10 ⁹ 5 x 10 ⁸	M Gate
2- and 3-D dopant profile spatial resolution (nm)	3	3	3	2	2	2	1.5	M Gate

Table 61(a) Metrology "LONG TERM" Technology Requirements

<i>Year of First Product Shipment Technology Generation</i>	<i>2008 70 nm</i>	<i>2017 50 nm</i>	<i>2014 35 nm</i>	<i>DRIVER</i>
<i>DRAM 1/2 Pitch</i>	70	50	35	D ½
<i>Logic Isolated Lines</i>	45	32	22	M Gate
Microscopy				
In-line, nondestructive microscopy resolution (nm) for P/T=0.1	0.45	0.30	0.2	M Gate
Maximum aspect ratio / diameter (nm) (DRAM contacts)	10.5 80	12 60	13.5 45	D ½
Materials and Contamination Characterization				
Real Particle Detection limit (nm) ^B	22	16	11	M Gate
Minimum Particle size for compositional analysis (on patterned wafers) (nm)	15	10	7	M Gate
Surface detection limits (Al, Zn)/ (Ni, Fe, Cu, Na, Ca) (atoms/cm ²) with Signal to Noise of 3:1	5 x 10 ⁸ 4 x 10 ⁸	≤ 5 x 10 ⁸ 7 x 10 ⁷	≤ 5 x 10 ⁸ ≤ 6 x 10 ⁷	M Gate
2- and 3-D dopant profile spatial resolution (nm)	1	0.8-0.6	0.8-0.6	M Gate

<i>Solutions Exist</i>	<i>Solutions Being Pursued</i>	<i>No Known Solutions</i>
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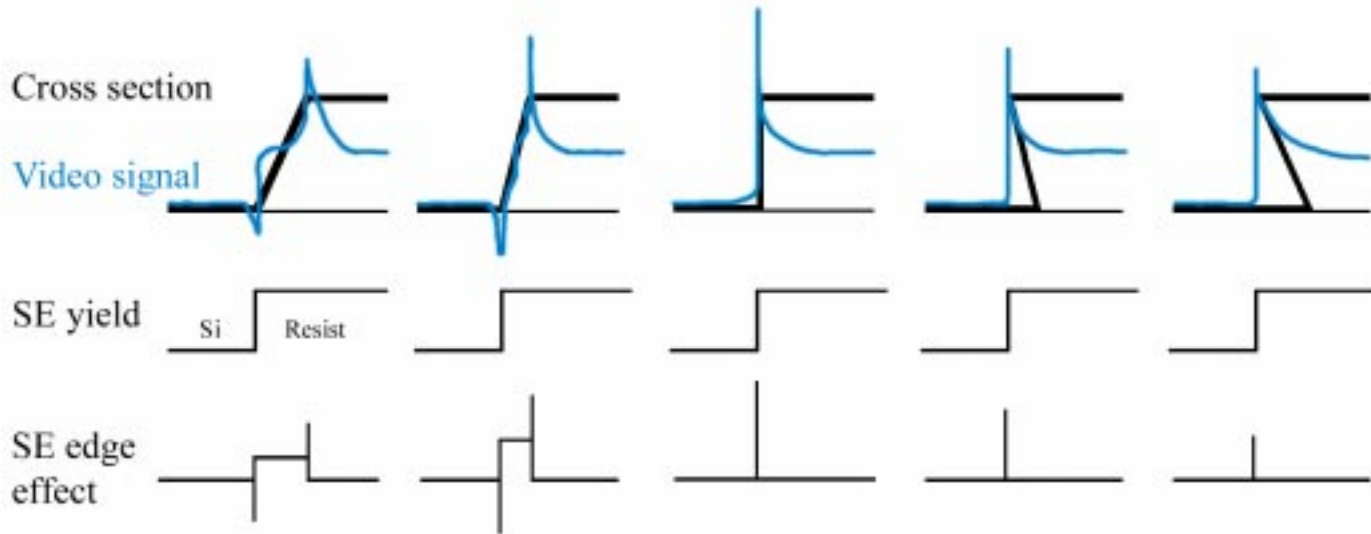
^A Metal and via aspect ratios are additive for dual-Damascene process flow.

^B This value depends on surface microroughness and layer composition.

Lithography Metrology

Improve CD-SEM thru 100 nm node

Signal Waveforms on Various Edges



There is information that is currently not being used!

Andras Vladar H.P.

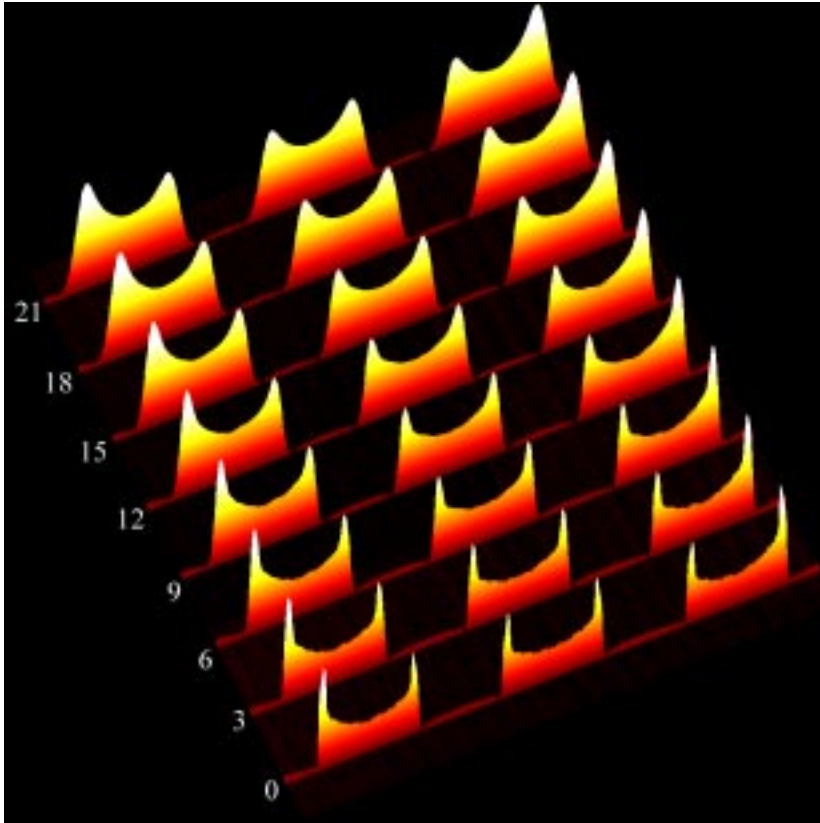
International Technology Roadmap for Semiconductors



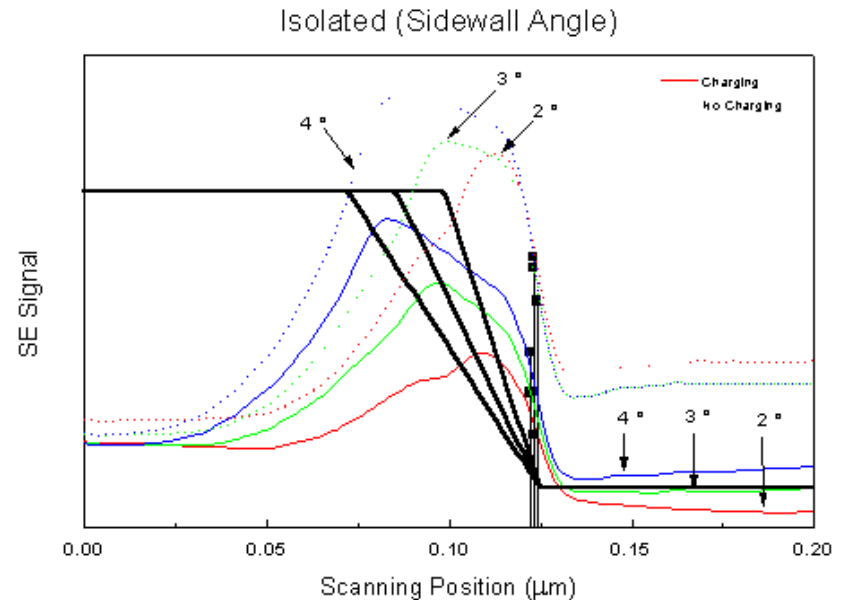
Work in Progress --- Not for Publication

Lithography Metrology

Improve CD-SEM thru 100 nm node



Changing waveforms due to various primary electron beam diameters (nm)



Side wall angle dependence

Yeong-Uk Ko

Korea Research Institute of Standards and Science

Andras Vladar H.P.

International Technology Roadmap for Semiconductors

Work in Progress --- Not for Publication



Table 61a Short Term Metrology Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Wafer Gate CD Control*	13	10.8	9.0	8.1	7.2	6.3	5.9	
Wafer Dense Line CD Control*	18	16.5	15	13	12	11	10	
Wafer Contact CD Control*	20	18.5	17	15	14.5	14	13	
Wafer CD Metrology Tool Precision* P/T=.2 for Isolated Lines**	2.6	2.2	1.8	1.6	1.4	1.3	1.2	
Wafer CD Metrology Tool Precision* P/T=.2 for Dense Lines**	3.6	3.3	3.0	2.6	2.4	2.2	2.0	
Wafer CD Metrology Tool Precision* P/T=.2 for Contacts**	4.0	3.7	3.4	3.0	2.9	2.6	2.3	
Maximum CD Measurement Bias (in percent)	10	10	10	10	10	10	10	
Mask CD Control Isolated Lines*	16	14	12	10	9	8	7	
Mask CD Control Dense Lines*	24	21	17	13	12	11	10	
Mask Contact Area Control Normalized to v of Area*	24	21	17	14	13	12	11	
Mask CD Metrology Tool Precision* P/T=.2 for Isolated Lines**	3.2	2.8	2.4	2	1.8	1.6	1.4	
Mask CD Metrology Tool Precision* P/T=.2 for Dense Lines**	4.8	4.2	3.4	2.6	2.4	2.2	2	
Mask Area Metrology Tool Precision for Contact Normalized to v of Area - v of Target for P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2	
Wafer Overlay control (nm)	65	58	52	45	42	38	35	
Wafer Overlay Output Metrology Precision (nm, 3 sigma)* P/T=.1	6.5	5.8	5.2	4.5	4.2	3.8	3.5	
Final Mask Image Placement	39	35	31	27	25	23	21	
Mask Image Placement Metrology Precision P/T=.1	3.9	3.5	3.1	2.7	2.5	2.3	2.1	
Mask Phase (in degrees)	2	2	2	2	2	2	2	
Phase Metrology Precision P/T=.2 (in degrees)	.4	.4	.4	.4	.4	.4	.4	
Variation in Attenuated mask Film Transmission % of Deviation from Nominal (in percent)	4	4	4	4	4	4	4	
Transmission Metrology Precision % of Nominal Attenuated PSM Transmission P/T=.2 (in percent)	.8	.8	.8	.8	.8	.8	.8	

* All precision values are 3 sigma in nm and include metrology tool matching.

Table 61b Long Term Metrology Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	2008 70 nm	2011 50 nm	2014 35 nm	DRIVE R
Wafer Gate CD Control*	4.0	3.0	2.0	
Wafer Dense Line CD Control*	7.0	5.0	3.5	
Wafer Contact CD Control*	8.0	5.5	4.0	
Wafer CD Metrology Tool Precision* P/T=.2 for Isolated Lines**	0.8	0.6	0.4	
Wafer CD Metrology Tool Precision* P/T=.2 for Dense Lines**	1.4	1.0	.07	
Wafer CD Metrology Tool Precision* P/T=.2 for Contacts**	1.6	1.1	0.8	
Maximum CD Measurement Bias (in percent)	10	10	10	
Mask CD Control Isolated Lines*	7	5	3.3	
Mask CD Control Dense Lines*	11	8	5.6	
Mask Contact Area Control Normalized to v of Area*	12	9	6.4	
Mask CD Metrology Tool Precision* P/T=.2 for Isolated Lines**	1.4	1.0	0.7	
Mask CD Metrology Tool Precision* P/T=.2 for Dense Lines**	2.2	1.6	1.1	
Mask Area Metrology Tool Precision for Contact Normalized to v of Area - v of Target for P/T=.2	1.6	1.8	1.3	
Wafer Overlay control (nm)	25	20	15	
Wafer Overlay Output Metrology Precision (nm, 3 sigma)* P/T=.1	2.5	2.0	1.5	
Final Mask Image Placement	16	12	9	
Mask Image Placement Metrology Precision P/T=.1	1.6	1.2	0.9	
Mask Phase (in degrees)	1			
Phase Metrology Precision P/T=.2 (in degrees)	2			
Variation in Attenuated mask Film Transmission % of Deviation from Nominal (in percent)	4			
Transmission Metrology Precision % of Nominal Attenuated PSM Transmission P/T=.2 (in percent)	8			

* All precision values are 3 sigma in nm and include metrology tool matching.

** Measurement tool performance needs to be independent of line shape, line materials, and density of lines.

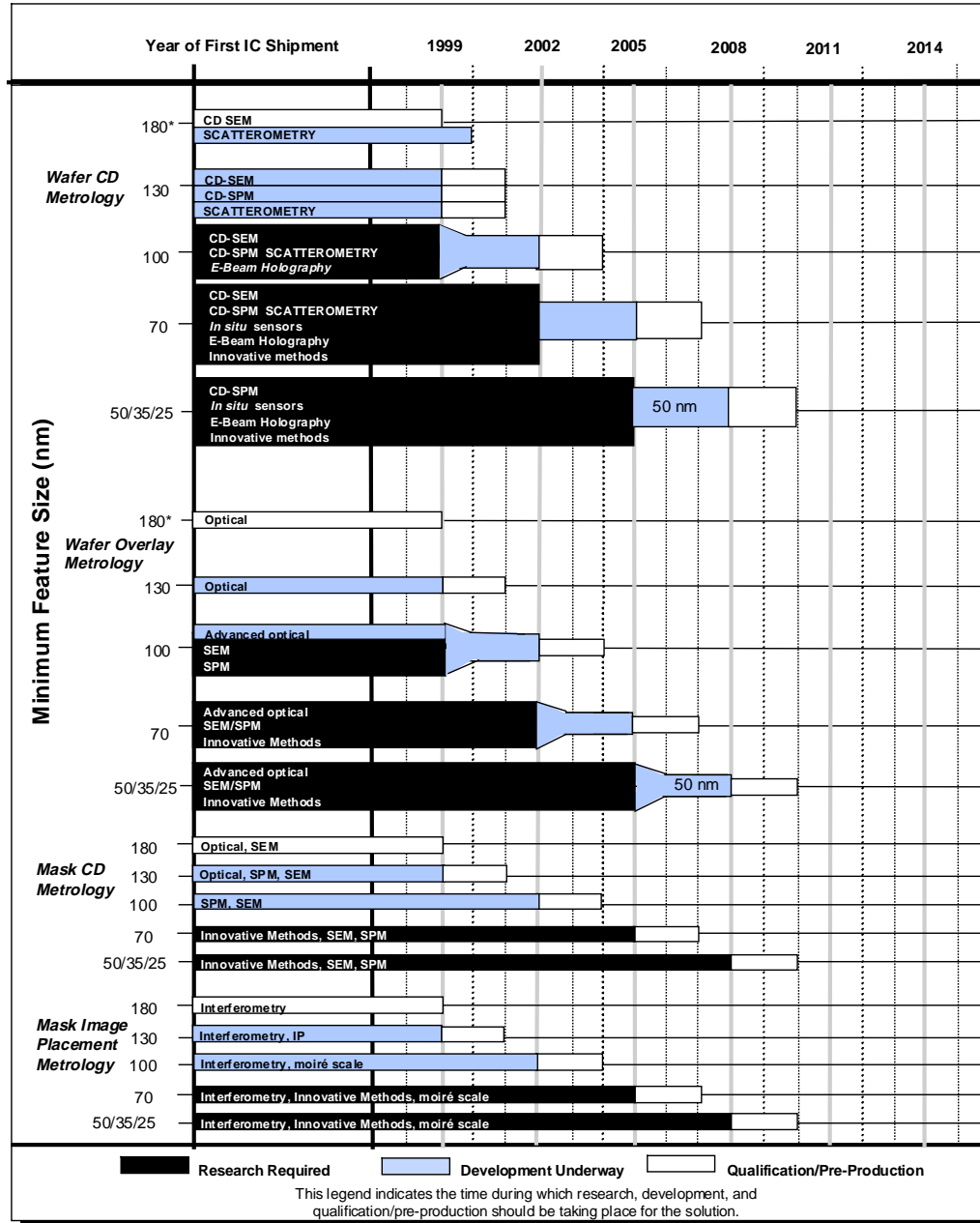
Solutions Exist

Solutions Being Pursued

No

Known

Litho



LITHOGRAPHY - FIGURE 22 LITHOGRAPHY METROLOGY POTENTIAL SOLUTIONS

Table 61(c) Front End Processes Metrology "SHORT TERM" Technology Requirements

Year of First Product Shipment Technology Generation	1999 180 nm	2000 180 nm	2001 180 nm	2002 130 nm	2003 130 nm	2004 130 nm	2003 100 nm	Driver
DRAM 1/2 Pitch	180	180	180	130	130	130	100	D/2
Logic Isolated Lines	140	120	100	85	80	70	65	MGate
Oxygen range (ASTM ^A "79) in heavily doped substrates; measurement precision ± 0.5 ppm	18-31	18-31	18-31	18-31	18-31	18-31	18-31	
Logic Dielectric Equivalent Thickness (nm) ± 3σ process range	1.9 – 2.5 ± 4%	1.8 – 2.3 ± 4%	1.6 – 2.0 ± 4%	1.3 – 1.7 ± 4%	1.2 – 1.6 ± 4%	1.0 – 1.4 ± 4%	0.9 – 1.1 ± 4%	MGate
Logic Dielectric Measurement Precision 1σ (nm) ^B	0.0025	0.0024	0.0021	0.0017	0.0016	0.0013	0.0012	MGate
DRAM Capacitor Structure Dielectric Material Process Control Requirements	CvL MIS Ta2O5	CvL MIS Ta2O5	CvL MIS Ta2O5	STD MIM BST	STD MIM BST	STD MIM BST	STD MIM BST	D/2
2- and 3-D Dopant Profile Spatial Resolution (nm)	3	3	3	2	2	2	1.5	
At-line Dopant Concentration Precision (Across Concentration Range) ^C	5%	5%	5%	4%	4%	4%	3%	

Table 61(c) Front End Processes "LONG TERM" Metrology Technology Requirements

<i>Year of First Product Shipment Technology Generation</i>	<i>2008 70 nm</i>	<i>2011 50 nm</i>	<i>2014 35 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch</i>	70	50	35	
<i>Logic Isolated Lines</i>	45	32	22	
Oxygen range (ASTM "79" ^A) in heavily doped substrates; measurement precision ± 0.5 ppma	18 – 31	18 - 31	18 - 31	
Bulk Detection Limits for Trace Metals for Bulk Silicon and SOI Top Silicon Layer. (Fe concentration in atoms/cm ³)	1 x 10 ¹⁰	1 x 10 ¹⁰	1 x 10 ¹⁰	
Logic Dielectric Equivalent Thickness (nm) ± 3σ process range	0.6 – 1.0 ± 4%	0.5 – 0.8 ± 4%	0.3 – 0.6 ± 4%	
Logic Dielectric Measurement Precision 1σ (nm) ^B	0.0008	0.0007	0.0004	
DRAM Capacitor Structure Dielectric Material Process Control Requirements	STD MIM BST	STD MIM PZT	STD MIM PZT	
2- and 30D Dopant Profile Spatial Resolution (nm)	1	0.8 - 0.6	0.8 - 0.6	
At-line Dopant Profile ^C Concentration Precision (Across Concentration Range)	4%	4%	4%	

<i>Solutions Exist</i>	<i>Solutions Being Pursued</i>	<i>No Known Solutions</i>
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^A IOC '88 value obtained by multiplying ASTM value by 0.65.

^B Precision calculated from $P/T=0.1=6 * \text{precision}/\text{process range}$. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitrides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as TaO5 will be used at and after the 70 nm logic generation. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\epsilon_{\text{high } k} / \epsilon_{\text{ox}}$) by the effective oxide thickness. For example, a 6.4 nm thick TaO5 ($k=25$) layer has a 1 nm equivalent oxide ($k=3.9$) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.

^C High precision measurements with low systematic error are required.

FEP

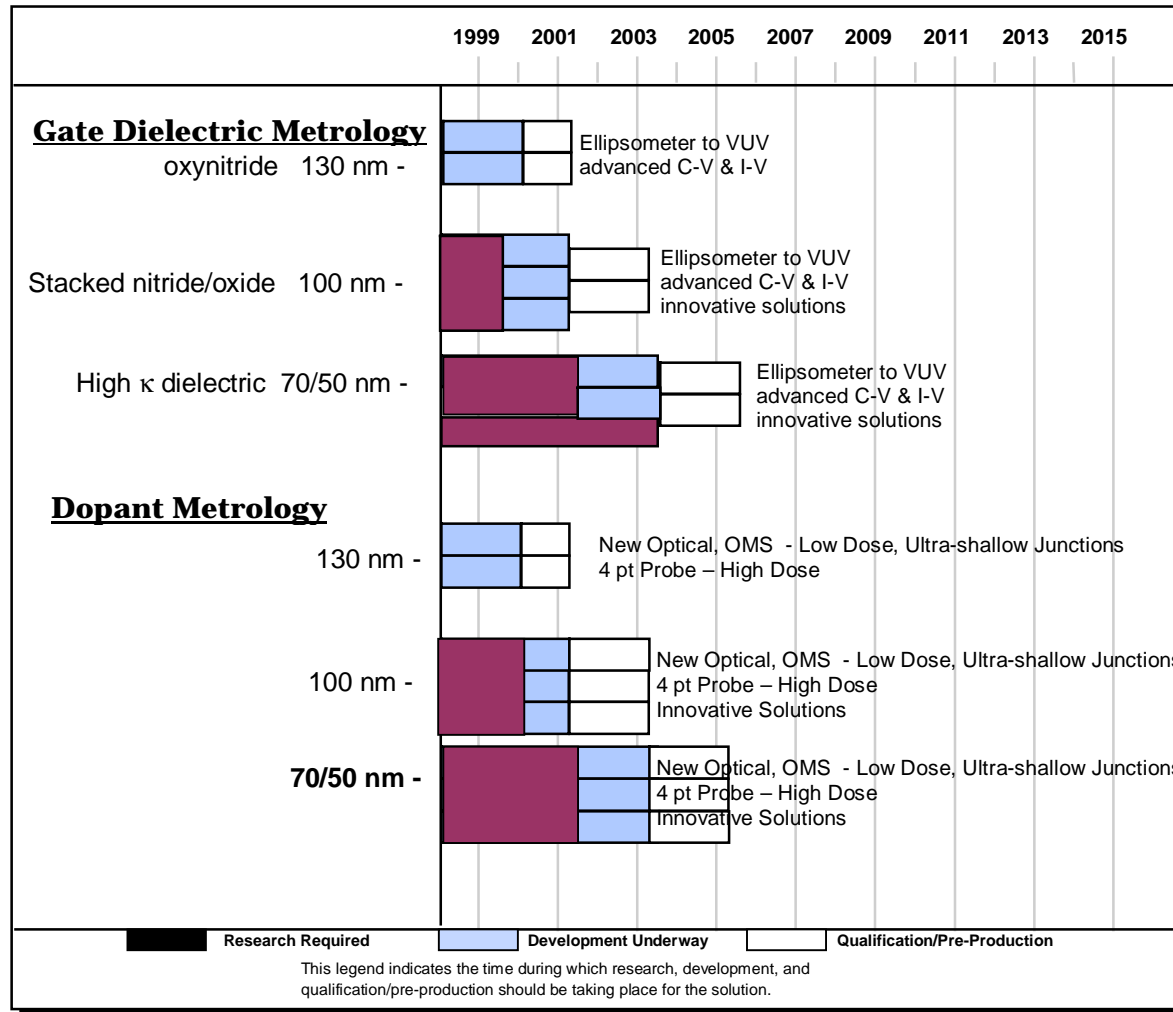


Table 64(d) Interconnect Metrology 'SHORT TERM' Technology Requirements

<i>Year of First Product Shipment</i> <i>Technology Generation</i>	<i>1999</i> <i>180nm</i>	<i>2000</i> <i>180nm</i>	<i>2001</i> <i>180nm</i>	<i>2002</i> <i>130nm</i>	<i>2003</i> <i>130nm</i>	<i>2004</i> <i>130nm</i>	<i>2005</i> <i>100nm</i>	<i>DRIVER</i>
<i>DRAM1/2 Pitch</i>	<i>180</i>	<i>180</i>	<i>180</i>	<i>130</i>	<i>130</i>	<i>130</i>	<i>100</i>	
<i>Logic Isolated Lines</i>	<i>140</i>	<i>120</i>	<i>100</i>	<i>85</i>	<i>80</i>	<i>70</i>	<i>65</i>	
Planarity requirements within litho field for minimum interconnect CD (nm)	250	250	250	200	200	200	175	MPU
Measurement of deposited barrier layer at Thickness (nm) / process range ($\pm 3\sigma$) Precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers A	23/20% 0.08	19/20% 0.06	16/20% 0.05	13/20% 0.04	11/20% 0.035	7/20% 0.02	3/20% 0.01	MPU
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)								
Measure interlevel metal insulator effective dielectric constant (k) and anisotropy on patterned structures at 5x to 10x local clock frequency (GHz) B	3.5-4.0 1.25	3.5-4.0 TBD	2.7-3.0 TBD	2.7-3.0 2.1	2.2-2.7 TBD	2.2-2.6 TBD	1.6-2.2 3.5	MPU

Table 64(d) Interconnect Metrology "LONG TERM" Technology Requirements

Year of First Product Shipment Technology Generation	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Planarity requirements within litho field for minimum interconnect CD (nm)	175	175	175	MPU
Measurement of deposited barrier layer at Thickness (nm) / process range ($\pm 3\sigma$) Precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers ^A	0	0		MPU
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)	1	1	1	MPU
Measure interlevel metal insulator effective dielectric constant (k) and anisotropy on patterned structures at 5x to 10x clock frequency (GHz) ^B	<1.5 6	<1.5 10	<1.5 17	MPU

<i>Solutions Exist</i>	<i>Solutions Being Pursued</i>	<i>No Known Solutions</i>
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^A
* Roadmap predicts barrier for 35 nm Technology Generation will be formed by reactive processes in metal or dielectric or both instead of by deposition.

^B
Minimum effective dielectric constant is listed. Due to divergence of DRAM and Logic requirements, minimum listed number is associated with logic requirements. The development of a measurement technique for low k dielectric constant and anisotropy is nearly complete up to 40 GHz. Technology transfer to industry will take place from 1999 to 2000.

Interconnect

