Modeling and Simulation TWG

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Modeling and Simulation TWG:
Key Messages

- High frequency circuit models
- Models to reduce cross-die variation (OPC, CMP, equipment modeling)
- Model alternative lithography technology tradeoffs
- Gate stack modeling for ultra-thin/alternative dielectrics
- Modeling limits of MOS; models for innovative MOS and beyond
- Goals for cost reduction due to TCAD

Difficult Challenges:
High frequency circuit modeling (>1GHz)

DIFFICULT CHALLENGES ^{3}100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

•Efficient simulation of full-chip interconnect delay

•Accurate 3-D interconnect model; inductance effects

•High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects

- Efficient, accurate interconnect modeling critical for future high speed circuits

Difficult Challenges:

Unified Package/die-level models

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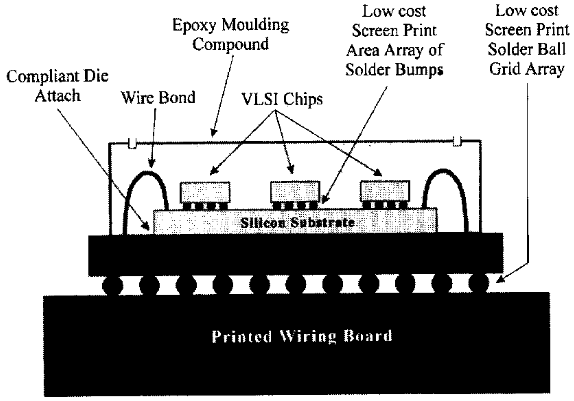
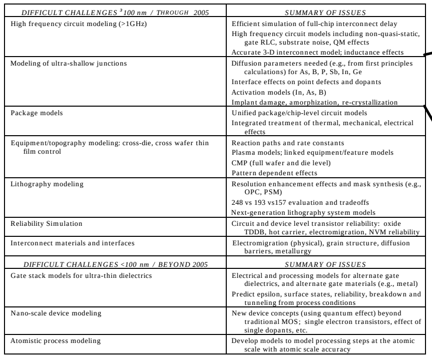
- **Unified package/chip-level circuit models**
- **Integrated treatment of thermal, mechanical, electrical effects**

- Packages becoming increasingly complex electrical devices
- High frequency interaction of package and die must be modeled together
- Thermo-mechanical effects must be understood
- Long-range: mixed electrical/optical analysis



Difficult Challenges:

Modeling of ultra-shallow junctions



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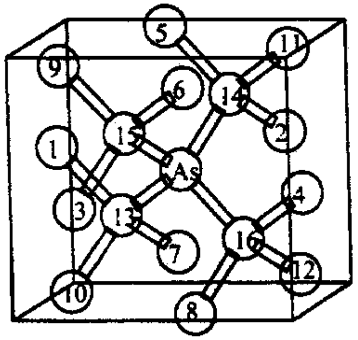
- **Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge**
- **Interface effects on point defects and dopants**
- **Activation models (In, As, B); metastable states**
- **Implant damage, amorphization, re-crystallization**

- Significant progress recently using <u>quantum calculations</u> for diffusion parameters
- <u>Interface</u> interactions dominate
  - ➢Shallow junctions: all dopants are next to surface
- <u>Activation</u> issues become important
  - ➢ Scaled devices need low resistivity source/drain



Difficult Challenges: Equipment/topography modeling: Model thin film and etch control across die/wafer

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- **Reaction paths and rate constants**
- **Plasma models; linked equipment/feature models**
- **CMP (full wafer and die level)**
- **Pattern dependent effects**

•<u>Within-die variation</u> becoming key performance limiter; reduction is a source of performance gain

•Future litho has <u>reduced depth of focus</u>, increasingly tight cross-die layer uniformity requirements

• <u>300mm wafer</u> transition imminent

Difficult Challenges:
Model Alternative Lithography Tradeoffs

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- **Resolution enhancement effects and mask synthesis (e.g., OPC, PSM)**
- **Predictive resist models**
- **248 vs 193 vs 157 evaluation and tradeoffs**
- **Next-generation litho system models**

- Near term: resolution enhancement techniques, wavelength tradeoffs;
- Near term: layout compensation (e.g. OPC)
- Long term: early evaluation of competing Next Generation Litho approaches

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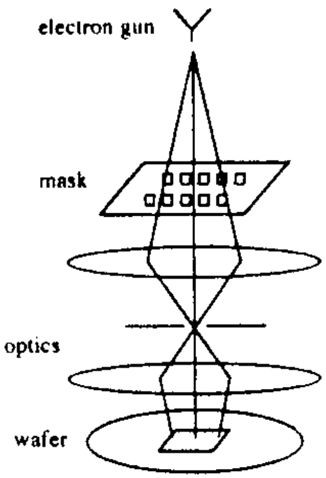
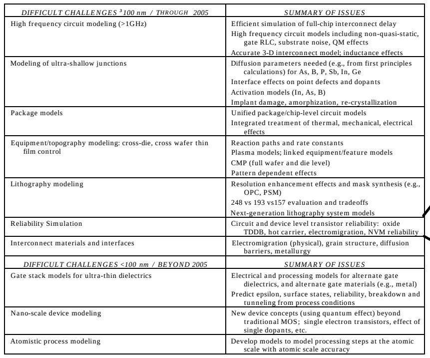


Difficult Challenges:

Reliability models for circuit design and technology development



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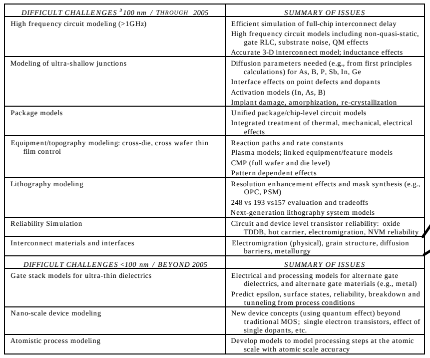
- **Circuit and device level transistor reliability: oxide TDDB, SER, hot carrier, electromigration,**
- **NVM reliability**
- **ESD, latchup**

- Device level: need predictive models for transistor reliability issues

- Circuit level: empirical models to guard-band designs

Difficult Challenges:

Model new interconnect materials and interfaces



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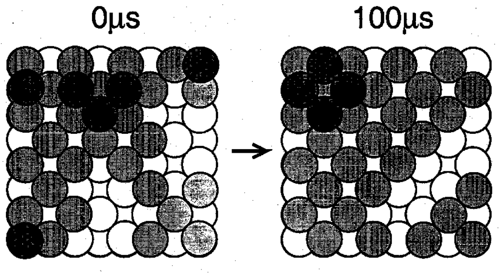
•Electromigration (physical), grain structure, diffusion barriers, metallurgy

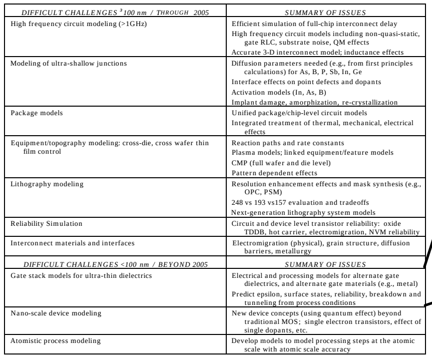
- Interconnect systems are rapidly evolving:
  - → New materials: dielectrics, barrier layers, metallurgies
- Increasing concerns: thermo-mechanical stress, diffusion, electromigration



Cu diffusion (A. Voter, LANL)

Difficult Challenges:

Gate stack modeling for ultra-thin dielectrics



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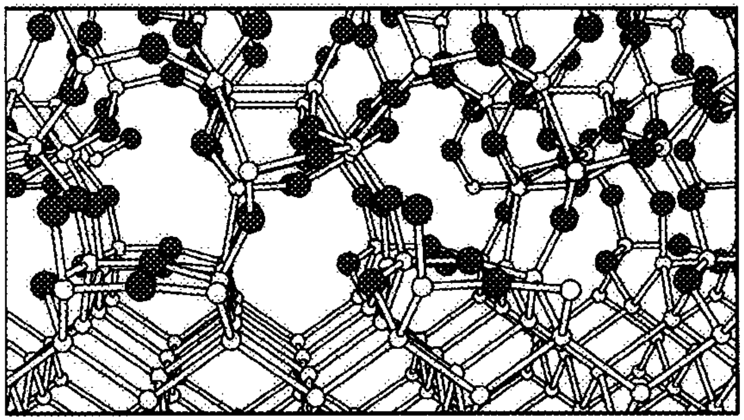
- **Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal)**
- **Model epsilon, surface states, reliability, breakdown and tunneling from process conditions**

- Detailed process modeling of gate dielectric to optimize the thinnest SiO2/SiO_xN_y systems, metal gate
- Modeling of alternative gate dielectric materials (atomic scale)
- Rigorous quantum treatment of gate stack



Simulated Si/SiO2 interface (K. Ng, D. Vanderbilt, PRB 59 April 1999)

Difficult Challenges:

Nano-scale device modeling

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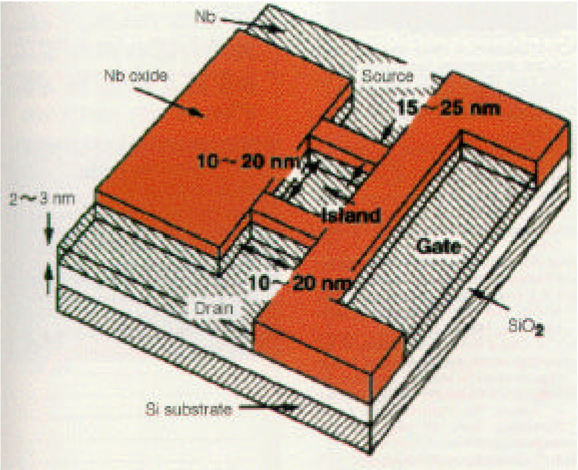
- **Model new device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.**

- Possibility: scaling of traditional MOS device <u>slows</u> or <u>ends</u>

- Advanced research needed: exploration of innovative MOS concepts and devices beyond MOS

- Emphasize <u>system performance</u> modeling of new devices



Single electron transistor

(J. Shirakashi, ETL, Tsukuba)

Difficult Challenges:

Atomistic process modeling

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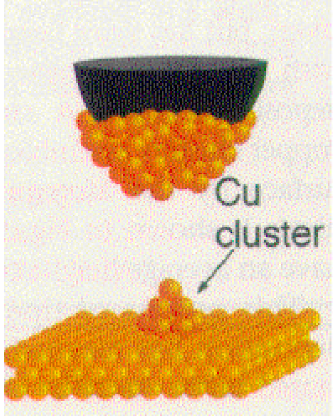
•Develop models to model processing steps at the atomic scale with atomic scale accuracy

• Whatever direction technology takes, manipulation of atomic layer dimensions needed near end of the roadmap.

• Development of theoretical, simulation and instrumental infrastructure should start now



Technology Requirements: Cost Reduction

YEAR OF INTRODUCTION	***1999*** ***180nm***	***2000***	***2001***	***2002*** ***130nm***	***2003***	***2004***	***2005*** ***100nm***	***Driver***
OVERALL COST REDUCTION TARGET (DUE TO TCAD)	**20%**			**25%**			**35%**	

- Goal of TCAD Technology Requirements: overall development cost reduction
- Successful Application to Family Processes
- For Devices of New Technology Node,

  More efforts needed for Predictive Modeling
- Still at its Infancy Level for Back End Process Modeling

Basis for Cost Reduction

	Relative Cost	0.18	0.13	0.10
Total		20%	25%	35%
New Tech Node (front end)	4	30%	40%	50%
Family Process (front end)	1	50%	60%	60%
Back end Process Modules	4	0%	2%	10%

- Already contribute to Process Integration
- Wait for New Models for Back end Process modules

Technology Requirements: Process TCAD (Accuracy)

YEAR OF INTRODUCTION	*1999* *180nm*	*2000*	*2001*	*2002* *130nm*	*2003*	*2004*	*2005* *100nm*	*Driver*
PROCESS TCAD								
Vertical and lateral junction depth simulation accuracy	**18nm (10%)**			**13nm (10%)**			**10nm (10%)**	
Total source/drain series resistance (accuracy)	**20%**			**20%**			**20%**	
Long-channel Vt (accuracy)	**3% (45-54mV)**			**3% (36-45mV)**			**3% (27-36mV)**	

- Thermal Process of Lower Temperature and Shorter Time
- Classical but still Important Issues in TCAD
- Proper Evaluation Method highly Expected, especially for Dopant Profiles
- Effective Use achieved after Proper Calibration

Technology Requirements:
Process TCAD (Capabilities)

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
PROCESS TCAD								
Gate Stack: evaluate materials		Model alternate dielectrics			Model metal vs. poly gate			
Diffusion coefficients		Kinetics of diffusion and activation			Interface interactions with point defects and dopants			
Stress/extended defects		Front end stress model			Extended defects and disloactions			

- Atomistic-level Models required for New Gate Materials
- Point-defects issues still Important
- Extended defects to be Modeled Properly in view of Mechanical stresses and Generation/Recombination of point defects

Technology Requirements: Device Simulation (Accuracy)

YEAR OF INTRODUCTION	*1999* *180nm*	*2000*	*2001*	*2002* *130nm*	*2003*	*2004*	*2005* *100nm*	*Driver*
DEVICE MODELING (NUMERICAL)								
Accuracy of ft at given ft (% of maximum chip frequency)	**10%**			**10%**			**10%**	
Gate leakage current accuracy (%) (decreases due to increase of Ig/Id)	**100%**			**70%**			**40%**	
Ioff accuracy	**100%**			**70%**			**40%**	
Vt rolloff accuracy (mV)	**25mV**			**20mV**			**20mV**	

- Increasing Importance of Leakage/Off Current Modeling and Cut-off Frequency Modeling
- Ever-lasting importance of Vt Rolloff modeling

Technology Requirements:
Device Simulation (Capabilities)

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DEVICE MODELING (NUMERICAL)								
Gate stack models		**Gate current tunneling models**			**Full quantum gate stack models**			
Reliability models		**Transistor reliability models (gate oxide)**			**Interconnect reliability models (electromig., stress)**			
Noise/variation		**Dopant fluctuation**			**Noise models**			

- Quantum models needed for New Gate Stack Materials
- Predictive models needed for Reliablity Issues
  - Gate Oxide (Thinner Oxide, New Gate Materials…)
  - Interconnects (Electro/Stress Migration…)
- Smaller Devices more Susceptible to EMS

Long term device modeling

Modeling limits of MOS devices

- Noise margins
- Atomic-level fluctuations
- Reduction of yield due to statistical variation

Modeling for innovative MOS and beyond

- elevated source/drain
- SOI
- vertical MOS
- quantum effect devices? Others?

Potential Solutions:
Interconnect models

More accurate interconnect parasitic models are critical for high frequency design:

- Improved analytic capacitance models
  - 2D and 3D
  - cross-talk
- On-chip inductance modeling
  - substrate models
- Transmission line; full EM wave solvers
- Other interconnect modeling needs?

Potential Solutions:
Circuit models: Memory, System-on-Chip

Memory models:

- flash (program/erase)
- DRAM (read/write)
- FRAM

System-on-Chip

- Integrated digital, analog, and memory circuit models
- Other SoC circuit issues?

New circuit model challenges:

- RF device models:
  - active devices, passive devices
- SOI models (floating body effect)
- High voltage devices (for flat panel display)

Potential Solutions:

Reliability modeling (circuit/numerical)

- Gate dielectric degradation (circuit, numerical)
- Electromigration (circuit)
- ESD, Latchup (circuit, numerical)
- SER (circuit, numerical)
  - DRAM and logic
  - alpha and neutrons

Summary

- Next two generations (130nm, 100nm) provide many modeling challenges:
  - High frequency circuit models (RLC, xTOR)
  - Model cross-die variation due to litho, etch, thin film (e.g., OPC, CMP, equipment modeling)
  - Model lithography technology tradeoffs (resolution enhancement techniques, wavelength, PSM)
  - Goals for cost reduction due to TCAD
- Beyond 100nm, basic theoretical research needed:
  - Gate stack process and electrical model (atomic level)
  - Limts of MOS devices, innovative MOS devices and beyond

Modeling and Simulation Difficult Challenges

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005
High frequency circuit modeling (>1Ghz)
Modeling of ultra-shallow junctions
Unified Package/die-level models
Model thin film and etch variation across die/wafer Equipment/topography
Model alternative Lithography technologies
Reliability Simulation for circuit design and technology development
Model new interconnect materials and interfaces
DIFFICULT CHALLENGES <100 nm / BEYOND 2005
Gate stack models for ultra-thin dielectrics
Nano-scale device modeling
Atomistic process modeling