International Technology Roadmap for Semiconductors Conference

8-9 July 1999
Santa Clara Convention Center
Santa Clara, California

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AGENDA

THURSDAY — JULY 8, 1999

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7:30	Registration/Continental Breakfast	
8:00	Welcome	*IRC Members*

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8:15	Overall Technology Characteristics	*Alan Allan*
9:00	Design Report	*Steve Schulz*
9:30	Discussion/Feedback	
10:00	Summary	

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10:10	Break	

❖

10:30	Test Report	*Bob Nesbitt,Mark Barber*
11:00	Discussion/Feedback	
11:30	Summary	

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11:40	Lunch	

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12:40	Defect Reduction	*David Jensen, Osada*
13:10	Discussion/Feedback	
13:40	Summary	
13:50	Process Integration	*Steve Hillenius*
14:20	Discussion/Feedback	
14:50	Summary	

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15:00	Break	

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15:20	Lithography	*George Gomba*
15:50	Discussion/Feedback	
16:20	Summary	
16:30	Factory Integration	*Toshi Uchino, Ron Huber*
17:00	Discussion/Feedback	
17:30	Summary	

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17:40	Reception	

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18:10	Dinner with Key Note Jim Meindl	

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AGENDA

FRIDAY — JULY 9, 1999

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7:30	Registration/Continental Breakfast	
	❖	
8:00	Welcome	*IRC Members*
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8:15	Metrology	*Alain Diebold, Alec Reader*
8:45	Open Discussion/Feedback	
9:15	Summary	
	❖	
9:25	Break	
	❖	
9:45	Assembly and Packaging	*Chi Shih Chang, Darroll Paiga*
10:15	Open Discussion/Feedback	
10:45	Summary	
10:55	Front End Processes	*Walter Class*
11:25	Open Discussion/Feedback	
11:55	Summary	
	❖	
12:05	Lunch	
	❖	
13:05	Modeling and Simulation	*Paco Leon*
13:35	Open Discussion/Feedback	
14:05	Summary	
	❖	
14:15	Break	
	❖	
14:35	Environment, Safety & Health	*Francesca Illuzzi*
15:05	Open Discussion/Feedback	
15:35	Summary	
15:45	Interconnect	*Chris Case, Bob Geffken*
16:15	Open Discussion/Feedback	
16:45	Summary	
	❖	
16:55	Closing Remarks	*IRC Members*
	❖	
17:15	Adjourn	

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

Technology Generations—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	DRIVER
DENSE LINES (DRAM Half-Pitch) (nm)	WAS	180	161	145	130	119	109	100	
DRAM 1/2 PITCH (nm)	**IS**	**180**	**165**	**150**	**130**	**120**	**110**	**100**	
ISOLATED LINES (MPU Gates) (nm)	WAS	140	125	112	100	89	79	70	***D 1/2***
MPU GATE LENGTH (nm)	**IS**	**140**	**120**	**100**	**85**	**80**	**70**	**65**	***M GATE***
MPU / ASIC 1/2 PITCH (nm)	**NEW**	**230**	**210**	**180**	**160**	**145**	**130**	**115**	***M & A 1/2***
ASIC Gate Length (nm)	**NEW**	**180**	**165**	**150**	**130**	**120**	**110**	**100**	***A GATE***
Memory									
GENERATION ***@ introduction***	WAS/**IS**	1G			4G			16G	
GENERATION @ production ramp	WAS	256M			1G			4G	
GENERATION @ production (150 mm2 target) - Scenario 2**	**IS**	256M		**512M**			**1G**		
*Bits/cm2 @ introduction - Scenario 1**	WAS	270M	390M	543M	770M	1.1B	1.6B	2.2B	
Bits/cm2 @ introduction - Scenario 2**	**IS**	**175M**			**389.1M**			**875.2M**	
Bits/cm2 @ production (150 mm2 target) - Scenario 2**	**NEW**	**179M**		**358M**			**716M**		
Logic (High-Volume: Microprocessor) - cost-performance									
MPU *Logic transistors/cm2 (packed, including on-chip SRAM) (@introduction)*	WAS	6.2M	8.9M	12.62M	18M	23.3M	30.2M	39M	
Cost Performance MPU t/cm2 (including. on-chip SRAM) (@340 mm2 introduction. target)	**IS**	**7M**		**14M**		**28M**		**56M**	
Cost Performance MPU t/cm2 (including. on-chip SRAM) (@170 mm2 ramp target)	**NEW**	**7M**		**14M**		**28M**		**56M**	
Logic (Low-Volume: Microprocessor) - high-performance									
High Performance MPU t/cm2 (including. on-chip SRAM) (@450 mm2 ramp target)	**NEW**	**24.5M**		**49M**		**98M**		**196M**	
ASIC *Usable transistors/cm2 (auto layout)*	WAS	14M	16.8M	20.1M	24M	28.5M	33.8M	40M	
ASIC Usable transistors/cm2 (auto layout)	**IS**	**40M**	**55M**	**75M**	**115M**	**160M**	**225M**	**325M**	

* DRAM Scenario 1 - 1998 Update ** DRAM Scenario 2 - EIAJ cell factor limit

*** MPU Scenario 1 - Both cost-performance and high-performance MPU's target constant chip size @ introduction and also @ production ramp

**** High-performance MPU includes constant 280 mm2 on-chip SRAM added to ramp-level cost-performance core (2MByte/1999, doubles every 2 years)

***** Due to potential transistor area factor limitations (similar to DRAM cell-area factor limitations), there is a potential risk Scenario for both cost-performance and high - performance MPU - that is, introductory chip size could again increase after 2001 (return to 3-year node cycle), and the rate of increase could be even faster than the original 1997 NTRS/1998 ITRS Update (> 60% / 2 years)

Technology Generations—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DENSE LINES (DRAM Half-Pitch) (nm)	WAS	70	50	35	
DRAM 1/2 PITCH (nm)	**IS**	**70**	**50**	**35**	
ISOLATED LINES (MPU Gates) (nm)	WAS	50	35	25	**D 1/2**
MPU GATE LENGTH (nm)	**IS**	**45**	**32**	**22**	**M GATE**
MPU / ASIC 1/2 PITCH (nm)	**NEW**	**80**	**55**	**40**	**M & A 1/2**
ASIC Gate Length (nm)	**NEW**	**70**	**50**	**35**	A GATE
Memory					
GENERATION **@ introduction**	WAS/**IS**	64G	256G	1T	
GENERATION @ production ramp	WAS	16G	64G	256G	
GENERATION @ production (150 mm2 target) - Scenario 2**	**IS**			**16G**	
Bits/cm2 @ introduction - Scenario 1*	WAS	6.1B	17.2B	48.4B	
Bits/cm2 @ introduction - Scenario 2**	**IS**	**2B**	**4B**	**9.3B**	
Bits/cm2 @ production (150 mm2 target) - Scenario 2**	**NEW**			**11.5B**	
Logic (High-Volume: Microprocessor) - cost-performance					
MPU Logic transistors/cm2 (packed, including on-chip SRAM) (@introduction)	WAS	84M	180M	388M	
Cost Performance MPU t/cm2 (including. on-chip SRAM) (@340 mm2 introduction. target)	**IS**		**448M**		
Cost Performance MPU t/cm2 (including. on-chip SRAM) (@170 mm2 ramp target)	**NEW**		**448M**		
Logic (Low-Volume: Microprocessor) - high-performance					
High Performance MPU t/cm2 (including. on-chip SRAM) (@450 mm2 ramp target)	**NEW**		**1.6B**		
ASIC Usable transistors/cm2 (auto layout)	WAS	64M	100M	161M	
ASIC Usable transistors/cm2 (auto layout)	**IS**	**925M**	**2.6B**	**7.4B**	

** DRAM Scenario 1 - 1998 Update ** DRAM Scenario 2 - EIAJ cell factor limit*

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****** Due to potential transistor area factor limitations (similar to DRAM cell-area factor limitations), there is a potential risk Scenario for both cost-performance and high - performance MPU - that is, introductory chip size could again increase after 2001 (return to 3-year node cycle), and the rate of increase could be even faster than the original 1997 NTRS/1998 ITRS Update (> 60% / 2 years)*

Chip Size—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Functions/Chip									
DRAM Functions per Chip [B2] @ samples/introduction (bits)	WAS/**IS**	1.1B			4.3B			17.2B	
DRAM Functions per Chip @ production (Millions of bits)	WAS	268.5M			1.1B			4.3B	
DRAM Functions/Chip @ production (150 mm2 target) – Scenario 2**	**IS**	**268.5M**		**536M**			**1.1B**		
MPU Functions per Chip [B2] @ samples/introduction (transistors)	WAS	21M			76M			200M	
MPU Functions/Chip @ sample/introduction (340 mm2 target) - Scenario 1*	**IS**	**24M**		**48M**		**95.2M**		**191M**	
MPU Functions/Chip @ ramp (170 mm2 target) – Scenario 1*	**NEW**	**11.9M**		**24M**		**48M**		**95.2M**	
High Performance MPU Functions/Chip @ ramp (340 mm2 target) – Scenario 1*	**NEW**	**110M**		**220M**		**440M**		**880M**	
Chip Size (mm2) (@ introduction)									
DRAM ***(Scenario 1* - 98 Update)***	WAS	400			560			790	
DRAM (Scenario 2** - EIAJ)	**IS**	**614**			**1,104**			**1,963**	
Microprocessor - ***(98 Update: +20% / 3 years)***	WAS	340			430			520	
Microprocessor - (Scenario 1 - constant target 340 mm2)***	**IS**	**340**		**340**		**340**		**340**	
ASIC [maximum litho field area]	WAS	800	832	865	900	932	965	1,000	
Chip Size (mm2) (@production)									
DRAM (Scenario 2** - EIAJ)	**NEW**	**150**		**150**			**150**		
Microprocessor @ Ramp (B2) Year 3 (2nd shrink) +20% / 3 years)	WAS	205			260			310	
Microprocessor @ Ramp - (Sc. 1 - constant target 170 mm2)***	**IS**	**170**		**170**		**170**		**170**	
High Performance MPU* - (Sc. 1*** - constant target 450 mm2) 450 mm2)***	**NEW**	**450**		**450**		**450**		**450**	

** DRAM Scenario 1 - 1998 Update ** DRAM Scenario 2 - EIAJ cell factor limit*

**** MPU Scenario 1 - Both cost-performance and high-performance MPU's target constant chip size @ introduction and also @ production ramp*

***** High-performance MPU includes constant 280 mm2 on-chip SRAM added to ramp-level cost-performance core (2MByte/1999, doubles every 2 years)*

****** Due to potential transistor area factor limitations (similar to DRAM cell-area factor limitations), there is a potential risk Scenario for both cost-performance and high - performance MPU - that is, introductory chip size could again increase after 2001 (return to 3-year node cycle), and the rate of increase could be even faster than the original 1997 NTRS/1998 ITRS Update (> 60% / 2 years)*

Chip Size—Near Term Years

(Note: 1999 Litho Field Sizes represents current capability)

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Maximum Lithographic Field Size - Area (mm2)	WAS	800	829	858	900	932	965	1,000	
Maximum Lithographic Field Size – Area (mm2)	**IS**								
Maximum Lithographic Field Size - Width (mm)	WAS	32	33	35	36	37	39	40	
Maximum Lithographic Field Size – Width (mm)	**IS**								
Maximum Lithographic Field Size - Length (mm)	WAS	25	25	25	25	25	25	25	
Maximum Lithographic Field Size – Length (mm)	**IS**								
Minimum Lithographic Field Size - Area (mm2)	**NEW**	**484**	**484**	**484**	**484**	**484**	**484**	**484**	
Minimum Lithographic Field Size - Width (mm)	**NEW**	**22**	**22**	**22**	**22**	**22**	**22**	**22**	
Minimum Lithographic Field Size - Length (mm)	**NEW**	**22**	**22**	**22**	**22**	**22**	**22**	**22**	
Maximum substrate diameter (mm)									
Bulk or epitaxial or SOI*** wafer	WAS	300	300	300	300	300	300	300	
Bulk or epitaxial or SOI* wafer**	**IS**								

* DRAM Scenario 1 - 1998 Update ** DRAM Scenario 2 - EIAJ cell factor limit

*** MPU Scenario 1 - Both cost-performance and high-performance MPU's target constant chip size @ introduction and also @ production ramp

**** High-performance MPU includes constant 280 mm2 on-chip SRAM added to ramp-level cost-performance core (2MByte/1999, doubles every 2 years)

***** Due to potential transistor area factor limitations (similar to DRAM cell-area factor limitations), there is a potential risk Scenario for both cost-performance and high - performance MPU - that is, introductory chip size could again increase after 2001 (return to 3-year node cycle), and the rate of increase could be even faster than the original 1997 NTRS/1998 ITRS Update (> 60% / 2 years)

Chip Size—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Functions/Chip					
DRAM Functions per Chip [B2] @ samples/introduction (bits)	WAS/**IS**	69B	277B	1.1G	
DRAM Functions per Chip @ production (Millions of bits)	WAS	17.2B	68.7B	275B	
DRAM Functions / Chip @ production (150 mm2 target) – Scenario 2**	**IS**			**17.2B**	
MPU Functions per Chip [B2] @ samples/introduction (transistors)	WAS	520M	1.4B	3.62B	
MPU Functions / Chip @ sample/introduction (340 mm2 target) – Scenario 1*	**IS**		**1.53B**		
MPU Functions / Chip @ ramp (170 mm2 target) - Scenario 1*	**NEW**		**762M**		
High Performance MPU Functions / Chip @ ramp (340 mm2 target) – Scenario 1*	**NEW**		**7.04B**		
Chip Size (mm2) (@ introduction)					
DRAM **(Scenario 1* - 98 Update)**	WAS	1,120	1,580	2,240	
DRAM (Scenario 2 - EIAJ)**	**IS**	**3,436**	**6,872**	**11,780**	
Microprocessor - **(98 Update: +20% / 3 years)**	WAS	620	750	901	
Microprocessor - (Scenario 1* - constant target 340 mm2)**	**IS**		**340**		
ASIC [maximum litho field area]	WAS	1,100	1,300	1,482	
Chip Size (mm2) (@production)					
DRAM (Scenario 2 - EIAJ)**	**NEW**			**150**	
Microprocessor @ Ramp (B2) Year 3 (2nd shrink) +20% / 3 years)	WAS	370	450	540	
Microprocessor @ Ramp - (Sc. 1* - constant target 170 mm2)**	**IS**		**170**		
High Performance MPU** - (Sc. 1*** - constant target 450 mm2) 450 mm2)**	**NEW**		**450**		

* DRAM Scenario 1 - 1998 Update ** DRAM Scenario 2 - EIAJ cell factor limit

*** MPU Scenario 1 - Both cost-performance and high-performance MPU's target constant chip size @ introduction and also @ production ramp

**** High-performance MPU includes constant 280 mm2 on-chip SRAM added to ramp-level cost-performance core (2MByte/1999, doubles every 2 years)

***** Due to potential transistor area factor limitations (similar to DRAM cell-area factor limitations), there is a potential risk Scenario for both cost-performance and high - performance MPU - that is, introductory chip size could again increase after 2001 (return to 3-year node cycle), and the rate of increase could be even faster than the original 1997 NTRS/1998 ITRS Update (> 60% / 2 years)

Chip Size—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Maximum Lithographic Field Size - Area (mm2)	WAS	1,100	1,300	1,482	
Maximum Lithographic Field Size - Area (mm2)	**IS**				
Maximum Lithographic Field Size - Width (mm)	WAS	44	52	59	
Maximum Lithographic Field Size - Width (mm)	**IS**				
Maximum Lithographic Field Size - Length (mm)	WAS	25	25	25	
Maximum Lithographic Field Size - Length (mm)	**IS**				
Minimum Lithographic Field Size - Area (mm2)	**NEW**	**484**	**484**	**484**	
Minimum Lithographic Field Size - Width (mm)	**NEW**	**22**	**22**	**22**	
Minimum Lithographic Field Size - Length (mm)	**NEW**	**22**	**22**	**22**	
Maximum substrate diameter (mm)					
Bulk or epitaxial or SOI*** wafer	WAS	300	450	450	
Bulk or epitaxial or SOI* wafer**	**IS**				

* DRAM Scenario 1 - 1998 Update ** DRAM Scenario 2 - EIAJ cell factor limit

*** MPU Scenario 1 - Both cost-performance and high-performance MPU's target constant chip size @ introduction and also @ production ramp

**** High-performance MPU includes constant 280 mm2 on-chip SRAM added to ramp-level cost-performance core (2MByte/1999, doubles every 2 years)

***** Due to potential transistor area factor limitations (similar to DRAM cell-area factor limitations), there is a potential risk Scenario for both cost-performance and high - performance MPU - that is, introductory chip size could again increase after 2001 (return to 3-year node cycle), and the rate of increase could be even faster than the original 1997 NTRS/1998 ITRS Update (> 60% / 2 years)

Performance and Package Chips—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Number of Chip I/Os "Number of **Total** Chip Pads" - Maximum									
Chip–to–package (pads) cost-performance (MPU) - [Array]	WAS	934	1,037	1,151	1,277	1,418	1,574	1,747	
Chip–to–package (pads) cost-performance (MPU) - [Array] (From Chi-Shi Chang Email 6/6/99)	IS	840			1,280			2,430	
Chip–to–package (pads) high–performance (ASIC) - [Array]	WAS	1,867	2,072	2,300	2,553	2,834	3,146	3,492	
Chip–to–package (pads) high–performance (ASIC) - [Array] (From Chi-Shi Chang Email 6/6/99)	IS	1,670			2,440			4,380	
Chip–to–package (pads) high–performance (ASIC) - [Array] (From Test TWG Test Requirements Table for ASIC (Tables 3 and 4))	IS	1,850	2,100	2,300	2,550	2,850	3,200	3,500	
Chip–to–package (pads) - [Peripheral] (From Chi-Shi Chang Email 6/6/99)	NEW	368			464			584	
Number of Signal I/Os Chip Pads- Array									
Chip–to–package (pads) cost-performance [MPU - 1/3 of Total]	NEW	280			427			810	
Chip–to–package (pads) high–performance [ASIC - 1/2 of Total]	NEW	835			1,220			2,190	
Number of Power / Ground Chip Pads - Array									
Chip–to–package (pads) cost-performance [MPU - (2/3 of Total)]	NEW	560			853			1,620	
Chip–to–package (pads) high-performance [ASIC - (1/2 of Total)]	NEW	835			1,220			2,190	
Number of **Total** Package Pins/Balls – Maximum									
Microprocessor/controller, cost-performance	WAS	700	777	862	957	1,062	1,179	1,309	
Microprocessor/controller, cost-performance (From AP TWG Table 43)	IS	740	821	912	1,012	1,123	1,247	1,384	
Microprocessor/controller, cost-performance (From Test TWG Test Requirements Table for MPU (Total) (Tables 5 and 6))	IS	2,304	2,560	3,042	3,042	3,042	3,042	3,042	
Microprocessor/controller, cost-performance (From Test TWG Test Requirements Table for MPU (I/O)(Tables 5 and 6))	IS	768	1,024	1,024	1,024	1,024	1,024	1,024	
Microprocessor/controller, cost-performance (From Test TWG Test Requirements Table for MPU (Power and Ground) (Tables 5 and 6))	IS	1,536	1,536	2,018	2,018	2,018	2,018	2,018	
ASIC (high-performance)	WAS	1,400	1,554	1,725	1,915	2,126	2,359	2,619	
ASIC (high-performance (From AP TWG Table 43)	IS	1,600	1,792	2,007	2,248	2,518	2,820	3,158	

Performance and Package Chips—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Chip Pad Pitch (micron)(From Chi-Shi Chang Email 6/6/99)									
Pad Pitch - Ball Bond	**NEW**	**50**			**45**			**40**	
Pad Pitch - Wedge Bond	**NEW**	**45**			**40**			**35**	
Pad Pitch - Area Array	**NEW**	**200**			**200**			**150**	
Cost-Per-Pin									
Package cost (cents/pin) (cost-performance) - maximum	WAS	2.71	2.51	2.33	2.16	2.05	1.95	1.85	
Package cost (cents/pin) (cost-performance) – maximum (From AP TWG Table 43)	**IS**	**1.90**	**1.81**	**1.71**	**1.63**	**1.55**	**1.47**	**1.40**	
Package cost (cents/pin) (cost-performance) - minimum	WAS	0.78	0.71	0.65	0.60	0.57	0.54	0.51	
Package cost (cents/pin) (cost-performance) – minimum (From AP TWG Table 43)	**IS**	**0.90**	**0.86**	**0.81**	**0.77**	**0.73**	**0.70**	**0.66**	
Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)	WAS	0.90	0.87	0.83	0.80				
Package cost (cents/pin) (Memory) – maximum (From AP TWG Table 43)	**NEW**	**1.90**	**1.71**	**1.54**	**1.39**	**1.25**	**1.12**	**1.01**	
Package cost (cents/pin) (Memory) – minimum (From AP TWG Table 43)	**NEW**	**0.40**	**0.38**	**0.36**	**0.34**	**0.33**	**0.31**	**0.29**	
Chip Frequency (MHz)									
On-chip local clock, (high performance)	WAS	1,250	1,486	1,767	2,100	2,490	2,952	3,500	
On-chip local clock, (high performance)	**IS**	1,250	1,486	1,767	2,100	2,490	2,952	3,500	
On-chip, across-chip clock (high performance)	WAS	1,200	1,321	1,454	1,600	1,724	1,857	2,000	
On-chip, across-chip clock (high performance)	**IS**	1,200	1,321	1,454	1,600	1,724	1,857	2,000	
On-chip, across-chip clock, high-performance ASIC	WAS	500	559	626	700	761	828	900	
On-chip, across-chip clock, high-performance ASIC	**IS**	500	559	626	700	761	828	900	
On-chip, across-chip clock (cost-performance)	WAS	600	660	727	800	890	989	1,100	
On-chip, across-chip clock (cost-performance	**IS**	600	660	727	800	890	989	1,100	
Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	WAS	1,200	1,321	1,454	1,600	1,724	1,857	2,000	
Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	**IS**	1,200	1,321	1,454	1,600	1,724	1,857	2,000	
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	WAS	480	589	722	885	932	982	1,035	
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	**IS**	480	589	722	885	932	982	1,035	
Maximum Number Wiring Levels – maximum	WAS	7	7	7	7	7	8	8	
Maximum Number Wiring Levels – maximum	**IS**								
Maximum Number Wiring Levels – minimum	WAS	6	6	7	7	7	7	7	
Maximum Number Wiring Levels – minimum	**IS**								

Performance and Package Chips—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Number of Chip I/Os "Number of **Total** Chip Pads" - Maximum					
Chip–to–package (pads) cost-performance **(MPU) - [Array]**	WAS	2,386	3,268	4,470	
Chip–to–package (pads) cost-performance (MPU) - [Array] (From Chi-Shi Chang Email 6/6/99)	**IS**	**3,370**	**5,000**	**7,150**	
Chip–to–package (pads) high–performance **(ASIC) - [Array]**	WAS	4,776	6,532	8,935	
Chip–to–package (pads) high–performance (ASIC) - [Array] (From Chi-Shi Chang Email 6/6/99)	**IS**	**5,960**	**8,600**	**12,300**	
Chip–to–package (pads) high–performance (ASIC) - [Array] (From Test TWG Test Requirements Table for ASIC (Tables 3 and 4))	**IS**	**4,700**	**6,500**	**8,900**	
Chip–to–package (pads) - [Peripheral] (From Chi-Shi Chang Email 6/6/99)	**NEW**	**736**	**927**	**1,167**	
Number of Signal I/Os Chip Pads- Array					
Chip–to–package (pads) cost-performance [MPU - 1/3 of Total]	**NEW**	**1,123**	**1,667**	**2,383**	
Chip–to–package (pads) high–performance [ASIC - 1/2 of Total]	**NEW**	**2,980**	**4,300**	**6,150**	
Number of Power / Ground Chip Pads - Array					
Chip–to–package (pads) cost-performance [MPU - (2/3 of Total)]	**NEW**	**2,247**	**3,333**	**4,767**	
Chip–to–package (pads) high-performance [ASIC - (1/2 of Total)]	**NEW**	**2,980**	**4,300**	**6,150**	
Number of **Total** Package Pins/Balls – Maximum					
Microprocessor/controller, cost-performance	WAS	1,791	2,449	3,350	
Microprocessor/controller, cost-performance (From AP TWG Table 43)	**IS**	**1,893**	**2,589**	**3,541**	
Microprocessor/controller, cost-performance (From Test TWG Test Requirements Table for MPU (Total) (Tables 5 and 6))	**IS**	**3,840**	**4,224**	**4,416**	
Microprocessor/controller, cost-performance (From Test TWG Test Requirements Table for MPU (I/O)(Tables 5 and 6))	**IS**	**1,280**	**1,408**	**1,472**	
Microprocessor/controller, cost-performance (From Test TWG Test Requirements Table for MPU (Power and Ground) (Tables 5 and 6))	**IS**	**2,560**	**2,816**	**2,944**	
ASIC (high-performance)	WAS	3,581	4,898	6,700	
ASIC (high-performance (From AP TWG Table 43)	**IS**	**4,437**	**6,234**	**8,758**	

Performance and Package Chips—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Chip Pad Pitch (micron)(From Chi-Shi Chang Email 6/6/99)					
Pad Pitch - Ball Bond	**NEW**	**40**	**40**	**40**	
Pad Pitch - Wedge Bond	**NEW**	**35**	**35**	**35**	
Pad Pitch - Area Array	**NEW**	**150**	**150**	**150**	
Cost-Per-Pin					
Package cost (cents/pin) (cost-performance) – maximum	WAS	1.59	1.36	1.17	
Package cost (cents/pin) (cost-performance) – maximum (From AP TWG Table 43)	**IS**	**1.20**	**1.03**	**0.88**	
Package cost (cents/pin) (cost-performance) – minimum	WAS	0.44	0.38	0.33	
Package cost (cents/pin) (cost-performance) – minimum (From AP TWG Table 43)	**IS**	**0.57**	**0.49**	**0.42**	
Chip-Scale Lead-Frame Package cost (DRAM) (cents/pin)	WAS				
Package cost (cents/pin) (Memory) – maximum (From AP TWG Table 43)	**NEW**	**0.74**	**0.54**	**0.39**	
Package cost (cents/pin) (Memory) – minimum (From AP TWG Table 43)	**NEW**	**0.25**	**0.22**	**0.19**	
Chip Frequency (MHz)					
On-chip local clock, (high performance)	WAS	6,000	10,000	16,824	
On-chip local clock, (high performance)	**IS**	6,000	10,000	**13,500**	
On-chip, across-chip clock (high performance)	WAS	2,500	3,000	3,699	
On-chip, across-chip clock (high performance)	**IS**	2,500	3,000	**3,600**	
On-chip, across-chip clock, high-performance ASIC	WAS	1,200	1,500	1,936	
On-chip, across-chip clock, high-performance ASIC	**IS**	1,200	1,500	**1,800**	
On-chip, across-chip clock (cost-performance)	WAS	1,400	1,800	2,303	
On-chip, across-chip clock (cost-performance	**IS**	1,400	1,800	**2,200**	
Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	WAS	2,500	3,000	3,674	
Chip-to-board (off-chip) speed, high-performance, reduced-width, multiplexed bus)	**IS**	2,500	3,000	**3,600**	
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	WAS	1,285	1,540	1,878	
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	**IS**	1,285	1,540	**1,800**	
Maximum Number Wiring Levels – maximum	WAS	9	9	10	
Maximum Number Wiring Levels – maximum	**IS**				
Maximum Number Wiring Levels – minimum	WAS	8	9	10	
Maximum Number Wiring Levels – minimum	**IS**				

Electrical Defects—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	*DRIVER*
Defect Reduction									
DRAM 1st Year Electrical D0 @ 60% Yield (d/m2)	WAS	1,455	1,301	1,163	1,040	926	825	735	
DRAM 1st Year Electrical D0 @ 60% Yield (d/m2)	**IS**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	
DRAM 3rd Year Electrical D0 @ 80% Yield (d/m2)	WAS	985	877	781	695	619	551	490	
DRAM @ Production (150 mm2) - 85% yield	**IS**	**1,101**	**1,101**	**1,101**	**1,101**	**1,101**	**1,101**	**1,101**	
MPU 1st Year Electrical D0 @ 60% Yield (d/m2)	WAS	1,710	1,582	1,464	1,355	1,272	1,193	1,120	
MPU 1st Year Electrical D0 @ 60% Yield (d/m2)	**IS**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	
MPU 3rd Year Electrical D0 @ 80% Yield (d/m2)	WAS	1,150	1,064	984	910	857	807	760	
MPU @ Production Ramp (170 mm2) – 75% yield	**IS**	**1,742**	**1,742**	**1,742**	**1,742**	**1,742**	**1,742**	**1,742**	
ASIC 1st Year Electrical D0 @ 60% Yield (d/m2)	WAS	725	697	671	645	623	601	580	
ASIC 1st Year Electrical D0 @ 60% Yield (d/m2)	**IS**								
Minimum, mask count – maximum	WAS	24	24	24	24	25	25	26	
Minimum, mask count – maximum	**IS**								
Minimum, mask count – minimum	WAS	22	23	23	24	24	24	24	
Minimum, mask count – minimum	**IS**								

D_0–defect density

Electrical Defects—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		*2008 70 nm*	*2011 50 nm*	*2014 35 nm*	*DRIVER*
Defect Reduction					
DRAM 1st Year Electrical D0 @ 60% Yield (d/m2)	WAS	520	370	263	
DRAM 1st Year Electrical D0 @ 60% Yield (d/m2)	**IS**	**OMIT**	**OMIT**	**OMIT**	
DRAM 3rd Year Electrical D0 @ 80% Yield (d/m2)	WAS	350	250	179	
DRAM @ Production (150 mm2) - 85% yield	**IS**	**1,101**	**1,101**	**1,101**	
MPU 1st Year Electrical D0 @ 60% Yield (d/m2)	WAS	940	775	645	
MPU 1st Year Electrical D0 @ 60% Yield (d/m2)	**IS**	**OMIT**	**OMIT**	**OMIT**	
MPU 3rd Year Electrical D0 @ 80% Yield (d/m2)	WAS	640	525	436	
MPU @ Production Ramp (170 mm2) - 75% yield	**IS**	**1,742**	**1,742**	**1,742**	
ASIC 1st Year Electrical D0 @ 60% Yield (d/m2)	WAS	530	450	396	
ASIC 1st Year Electrical D0 @ 60% Yield (d/m2)	**IS**				
Minimum, mask count – maximum	WAS	28	28	30	
Minimum, mask count – maximum	**IS**				
Minimum, mask count – minimum	WAS	26	28	29	
Minimum, mask count – minimum	**IS**				

D_0–defect density

Power Supply and Power Dissipation—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Power Supply Voltage (V)									
Minimum logic Vdd (V) - maximum **[for maximum performance]**	WAS	1.8	1.7	1.6	1.5	1.4	1.3	1.2	
Minimum logic Vdd (V) - maximum [for maximum performance]	**IS**	1.8	**1.8**	**1.5**	1.5	**1.5**	**1.2**	1.2	
Minimum logic Vdd (V) - minimum **[for lowest power]**	WAS	1.6	1.4	1.3	1.2	1.1	1.0	0.9	
Minimum logic Vdd (V) - minimum [for lowest power]	**IS**	**1.5**	**1.5**	**1.2**	1.2	**1.2**	**0.9**	0.9	
Maximum Power									
High-performance with heatsink (W)	WAS	90	102	115	130	139	149	160	
High-performance with heatsink (W) *(From AP TWG Table 43)*	**IS**	**88**		**108**	**129**			160	
From Test TWG Test Requirements Table for ASIC (Tables 3 and 4)	**IS**	90	**100**	115	130	**140**	**150**	160	
Battery (W) - (Hand-held)	WAS	1.4	1.6	1.8	2.0	2.1	2.3	2.4	
Battery (W) - (Hand-held *(From AP TWG Table 43)*	**IS**	1.4		**1.7**	2.0			2.4	

Power Supply and Power Dissipation—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		*2008 70 nm*	*2011 50 nm*	*2014 35 nm*	*DRIVER*
Power Supply Voltage (V)					
Minimum logic Vdd (V) - maximum ***[for maximum performance]***	WAS	0.9	0.6	0.42	
Minimum logic Vdd (V) - maximum [for maximum performance]	**IS**	0.9	0.6	**0.60**	
Minimum logic Vdd (V) - minimum ***[for lowest power]***	WAS	0.6	0.5	0.37	
Minimum logic Vdd (V) - minimum [for lowest power]	**IS**	0.6	0.5	**0.30**	
Maximum Power					
High-performance with heatsink (W)	WAS	170	175	183	
High-performance with heatsink (W) *(From AP TWG Table 43)*	**IS**	170	**174**	**???**	
From Test TWG Test Requirements Table for ASIC (Tables 3 and 4)	**IS**	170	175	183	
Battery (W) - (Hand-held)	WAS	2.8	3.2	3.7	
Battery (W) - (Hand-held *(From AP TWG Table 43)*	**IS**	**2.0**	**2.2**	**2.4**	

Cost—Near Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Cost									
"Affordable" cost/bit @ (packaged - microcents) @ samples/introduction	WAS/**IS**	**42**	30	21	15	11	7.5	5.3	
"Affordable" cost/bit @ (packaged - ucents) @ production Sc. 2**	**NEW**	**20**		**8.8**			**2.1**		
MPU Affordable cost/transistor @ (packaged - microcents) **(@introduction)**	WAS	1,735	1,204	836	580	441	335	255	
Cost Performance MPU (ucents/t) (including. on-chip SRAM) (@340 mm2 introduction. Target)	**IS**	1,735		868		434		217	
Cost Performance MPU (ucents/t) (including. on-chip SRAM) (@170 mm2 ramp target)	**NEW**	**1,050**		**525**		**263**		**131**	
Cost-Per-Pin (see Table 3 - Items 3.4.x)									
Logic (Low–Volume: ASIC)									
ASIC Non–recurring engineering cost/usable transistor (microcents)	WAS	25	21	18	15	13	11	10	
ASIC Non–recurring engineering cost/usable transistor (microcents)	**IS**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	**OMIT**	
Test									
Volume tester cost **Per High-Frequency** Signal Pin ($K/pin) (high-performance) **[ASIC] - Maximum**	WAS	8	7	7	6	6	5	5	
Volume tester cost Per High-Frequency Signal Pin ($K/pin) (high-performance) [ASIC] - Maximum	**IS**	8	7	7	6	6	5	5	
Volume tester cost Per High-Frequency Signal Pin ($K/pin) (high-performance) [ASIC] - Minimum	**NEW**	**4**	**3**	**3**	**3**	**3**	**2**	**2**	
Volume tester cost/pin ($K/pin) (cost-performance) **[MPU]**	WAS	4	4	3	3	3	2	2	
Volume tester cost/pin ($K/pin) (cost-performance) [MPU]	**IS**	**8**	**8**	**7**	**7**	**6**	**6**	**5**	

Cost—Long Term Years

YEAR OF INTRODUCTION "TECHNOLOGY NODE"		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Cost					
"Affordable" cost/bit @ (packaged - microcents) @ samples/introduction	WAS/**IS**	2	1	0	
"Affordable" cost/bit @ (packaged - ucents) @ production Sc. 2**	**NEW**		**0**	**0**	
MPU Affordable cost/transistor @ (packaged - microcents) **(@introduction)**	WAS	110	50	22	
Cost Performance MPU (ucents/t) (including. on-chip SRAM) (@340 mm2 introduction. Target)	**IS**		27		
Cost Performance MPU (ucents/t) (including. on-chip SRAM) (@170 mm2 ramp target)	**NEW**		**16**		
Cost-Per-Pin (see Table 3 - Items 3.4.x)					
Logic (Low–Volume: ASIC)					
ASIC Non–recurring engineering cost/usable transistor (microcents)	WAS	5	3	1	
ASIC Non–recurring engineering cost/usable transistor (microcents)	**IS**	**OMIT**	**OMIT**	**OMIT**	
Test					
Volume tester cost **Per High-Frequency** Signal Pin ($K/pin) (high-performance) **[ASIC] - Maximum**	WAS	5	5	5	
Volume tester cost Per High-Frequency Signal Pin ($K/pin) (high-performance) [ASIC] - Maximum	**IS**	5	5	5	
Volume tester cost Per High-Frequency Signal Pin ($K/pin) (high-performance) [ASIC] - Minimum	**NEW**				
Volume tester cost/pin ($K/pin) (cost-performance) **[MPU]**	WAS	2	2	2	
Volume tester cost/pin ($K/pin) (cost-performance) [MPU]	**IS**	**4**	2	2	

DESIGN

On the one hand, the design section of the ITRS is receiving increased attention. The wider range of consumer products with a greater mix of technologies, the realization of "system on a chip (SOC)" manufacturing capability, the increasing role of software, the shrinking of both time-to-market requirements and product lifetimes, and the barriers to traditional technology scaling all highlight design as a key enabler for growth. On the other hand, many design roadblocks continue to loom. The "design gap" between what can be fabricated and what can be designed with current and projected design teams, tools, and market requirements continues to grow and is a bottleneck to billions in potential revenue. Hardware and software design flows remain fragmented. There remains overwhelming verification complexity. The tradeoff analysis among numerous requirements and constraints is growing. The Design chapter of the ITRS describes these challenges and potential solutions.

Scope

The objective of the semiconductor business is to produce chips that create profit for integrated circuit manufacturers, their customers, and their suppliers and strategic partners. The increased difficulty in designing, verifying, and testing these chips has become a larger barrier to achieving this objective than providing the technology for manufacturing them. This chapter describes the challenges in producing correct, performing designs and potential solutions for meeting them. While test equipment and the test of manufactured chips is covered elsewhere, the Design chapter addresses design for testability (DFT), including built-in self test (BIST). As in the other areas covered, both advances in and roadblocks to technology solutions create problems and opportunities in design.

The increasing complexity of design requires highly skilled and more broadly trained designers, and an array of computer-aided design tools that take into account factors that could be ignored in previous technology generations. Tools, which earlier could concentrate on discrete parts of the design problem, now must be aware of a broader range of factors. For example, logic synthesis tools, which assembled a network of unit-delay gates and assumed negligible wire delay, now must not only take interconnect and physical placement into account, but increasingly must accommodate the transistor-level properties of dynamic circuit families and the noise effects at smaller feature sizes. And the design flow must assure not only functional correctness but timing, power, reliability, manufacturability, and signal integrity requirements. Thus design complexity increases superexponentially, but automated tools are handicapped by having to run on the previous generation of computing equipment. This complexity has a similar effect on designers, with distinctions being blurred between logic design, layout, and circuit design.

As designs move from digital microprocessors and application-specific integrated circuits (ASICs) to SOC, designers and design tools also encounter more heterogeneous systems and the challenges of providing a diverse range of components on a single chip. Analog and mixed-signal, radio frequency (RF), micro-electromechanical systems (MEMS), electro-optical, electro-biological, and other nontraditional elements arise from and give rise to changes in technology. With this rapid rise in heterogeneity, technology advancement, and new product requirements, reuse of already designed intellectual property (IP), once considered to be a mitigating factor in design productivity, becomes increasingly difficult. Moreover, incorporation of several separately-designed components on a chip requires significant integration and verification cost.

The rapidly changing technological environment also shrinks product life cycles, making time-to-market one of the most critical issues for semiconductor customers. This demand is driven by growth of personal information flow through wired and wireless voice and data communication and, especially, the internet. There is great pressure to reduce the total time to create a chip, in order to produce products that are not obsolete before they are brought to market, and this time is dominated by the design and verification phase. Investment in technology improvements has dominated product creation resources, and design productivity has not been able to keep pace with transistor density growth. There continues to be a growing productivity gap between transistors available and able to be designed in microprocessors. As pointed out above, design re-use addresses only part of the productivity gap, and increase in the sizes of design teams brings with it its own problems with respect to productivity of large groups.

As time-to-market issues and SOC become dominant, embedded software emerges as a key design problem. The software content of products, and its cost, continues to rise. Issues surrounding this include high-level architectural design space exploration; analysis of the tradeoffs (design cycle time, performance, cost) of doing designs in hardware and software; high level design planning and estimation; hardware/software co-design at all design levels; and difficult verification and analysis. Software reliability becomes a greater factor, especially in critical applications, and software, previously designed to run on a processor or other isolated application, now runs in a global, interconnected environment. High-level design, and the accompanying design automation tools, are often considered key to design productivity improvement, but decisions made at higher levels of design must be based on accurate estimation of the effects of lower level decisions, and/or permit adjustments to logical and physical factors without wholesale iteration.

Finally, it should be noted that the Design chapter of the Roadmap, while increasingly important to the overall effort and time-to-market required to produce products and profit, is fundamentally different from the technology roadmap chapters, especially regarding the alignment of required design techniques to technology nodes. While technology advances tend to occur in discrete increments when all needed elements can be put in place in manufacturing, improvements in design techniques or the design process can normally be put in place when developed and can lead to improved productivity or quality immediately.

Difficult Challenges

Design challenges occur because of increases in the complexity of the component being designed; the technology in which it is being designed, and the tools used to design it. The system size, in terms of number of transistors, is increasing exponentially, but in addition, the number factors that designers and design tools must take into account as system heterogeneity increases and feature size decreases also is going up.

The following table, describing the difficult challenges in design, is grouped according to the drivers giving rise to five different complexity scales, and is ordered by immediacy of need. *Silicon complexity* is brought about by technology advances – smaller feature sizes not only bring more devices, but bring effects previously able to be ignored to prominence. *System complexity* is enabled by, but not driven by, this increase in capacity – the driver is consumer demand for applications with increasing heterogeneity and shorter time-to-market. The complexity of the *design procedures* used to produce working silicon increases because of both technology and system factors. And the *verification and analysis*, and *test and testability*, of chips, packages, and entire products also become more complex.

Near Term Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	SUMMARY OF ISSUES
Silicon complexity	Large numbers of interacting devices and interconnects Impact of signal integrity, noise, reliability, manufacturability Power and current management; voltage scaling Need for new logic families to meet performance challenges Atomic-scale effects Alternative technologies (such as copper, low κ, SOI)
System complexity	Embedded software as a key design problem System-on-a-chip design with a diversity of design styles (including analog, mixed-signal, RF, MEMS, electro-optical) Greatly increased system and function size Integrated passive components
Design procedure complexity	Convergence and predictability of design procedure Core-based, IP-reused designs and standards for integration Large, collaborative, multi-skilled, geographically distributed teams Interacting design levels with multiple, complex design constraints Specification and estimation needed at all levels Technology remapping or migration to maintain productivity
Verification and analysis complexity	Formal methods for system-level verification System-on-a-Chip specification Early high-level timing verification Core-based design verification (including analog/mixed-signal) Verification of heterogeneous systems (including mixed-signal, MEMS)
Test/testability complexity	Quality and yield impact due to test equipment limits Test of core-based designs from multiple sources (including analog, RF) Difficulty of at-speed test with increased clock frequencies Signal integrity testability

SOI–silicon on insulator

Long Term Difficult Challenges

FIVE ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Silicon complexity	Uncertainty due to manufacturing variability Uncertainty in fundamental chip parameters (such as signal skew) Design with novel devices (multi-threshold, 3D layout, SOI, etc.) Soft errors
System complexity	Total system integration including new integrated technologies (such as MEMS, electro-optical, electro-chemical, electro-biological) Design techniques for fault tolerance Embedded software and on-chip operating system issues
Design procedure complexity	True one-pass design process supporting incremental and partial design specification Integration of design process with manufacturing to address reliability and yield
Verification and analysis complexity	Physical verification for novel interconnects (optical, RF, 3-D, etc.) Verification for novel devices (nanotube, molecular, chemical, etc.)
Test/testability complexity	Dependence on self-test solutions for SOC (RF, analog) System test (including MEMS and electro-optical components)

System-on-a-Chip

Historically, the Roadmap has emphasized the technological limits of silicon production, leading to the specification of the most complex chips that can be developed in the categories of memory, microprocessor, and ASIC at a particular technology node. With the growing importance of high-volume consumer markets and the ability to integrate almost all aspects of a system design on a single chip, the ITRS should include an additional vehicle to capture the requirements of this important area. We refer to this vehicle as a System-On-a-Chip (SOC, sometimes called System LSI), and we distinguish it by its application-oriented nature. We believe the community should consider two major classes of SOC: the mainstream, cost-driven SOC (C-SOC) targeted towards high-volume consumer markets, and the high-end, performance-oriented SOC (P-SOC), targeted towards lower-volume, high-performance markets (such as high-performance networks). This latter category subsumes the role of the high-end ASIC in the Roadmap.

There are a number of characteristics that distinguish an SOC, but the main consideration is that it is primarily defined by its cost rather than by technological limits. Rather than asking, "How complex a chip can I build?" and then asking, "How much will it cost?" (the P-SOC emphasis), in the C-SOC category the question most often asked is, "If my budget for this component is $N, how much capability (gates, memory, performance, etc.) can I expect to get?" Clearly, the answer to this question is a complex combination of many factors. If one assumes a high-volume consumer part and so ignores nonrecurring engineering (NRE) costs related to design, production costs include the fundamental technological factors contemplated in the Roadmap (feature size, yield, field size, metal layers, etc.) as well as such factors as the cost of packaging and the cost of testing the SOC.

Of course, SOCs are also distinguished by other factors. As a *system*-on-a-chip, they are often mixed-technology designs, including such diverse combinations as embedded DRAM, high-performance or low-power logic, analog, RF, and technologies like MEMS, and optical input/output.

In all categories of the Roadmap, design productivity is a key requirement and it is expected that design reuse will grow as a major tool in achieving the productivity requirements. This is particularly true for the SOC category, where time-to-market for a particular application-specific capability is a key requirement of the designs. One who has an idea for a SOC product thinks about the building blocks to be combined to form the SOC. These blocks may be a controller core, embedded SRAM memory, and some dedicated logic. In some cases specific components/technological features may be added such as embedded Flash, or embedded DRAM, or in a few years from now MEMs or chemical sensors, or FRAM.

TEST AND TEST EQUIPMENT

Summary

The Test Roadmap focus has been expanded in 1999. It will expand the number of tables for test equipment from two to eight and will address memory testing for the first time. The test challenge is growing with the ever-increasing device frequency, power, and pin count, while trying to reduce cost. The new tables will address the following technology requirements for testing:

- **High-performance ASICs**
- **High-performance microprocessors**
- **Low-end microcontrollers**
- **Mixed-signal and RF devices**
- **Commodity DRAMs**
- **Embedded DRAMs**
- **Embedded FLASH memories**
- **Devices designed with design for test (DFT) and built-in-self-test (BIST)**

The 1994 and 1997 Roadmaps presented BIST and DFT as potential solutions for achieving simpler and affordable test equipment. Without BIST and DFT it was predicted that the number of test patterns required to test digital ICs in the year 2012 would skyrocket to 8400 million, resulting in unacceptable vector load times, and very expensive automatic test equipment (ATE). Unfortunately, no predictions were made as to when DFT/BIST accompanied by low-cost ATE would be widely accepted. The progress toward lower cost testers has been slow, but the increased use of BIST and DFT IC designs will cause a change in test equipment requirements and reduced cost in the near future.

The 1999 Test and Test Equipment Roadmap chapter also contains a new section describing a break from the traditional path of developing higher frequency ATE about every three years, with higher pincounts and increased cost. If ATE development continues to follow that path, costs will rise to unacceptable levels within a few years. The 1999 Roadmap describes a new approach by listing the requirements for developing ATE specifically designed to test ICs designed with DFT and BIST. Although an IC may have one or two thousand pins, only a small number of high-frequency I/O signal pins are required in the ATE (perhaps < 64). On the other hand, low-cost pin electronics must be provided to ensure that all the remaining pins will switch states properly. ATE for testing ICs designed with DFT/BIST could reduce equipment costs by a factor of ten, and thereby avoid the cost of traditional high-frequency, high pincount ATE from approaching $20M as predicted in previous roadmaps. This new approach to testing will require the cooperation of IC design and test groups within the IC manufacturing companies. This is perhaps the most difficult task. Another problem area is the need for analog BIST. The ATE industry should prepare themselves for the sale of simpler, lower-cost test equipment.

Difficult Challenges

The Difficult Challenges highlight the above issue, together with other challenges that are making test difficult, especially with the introduction of systems on a chip (SOCs). Fundamental physics problems, timing inaccuracies, noise, along with escalating cost, demand a change in test methods. These are challenges that will present themselves before and after the year 2005 that require solutions to be developed by the ATE industry, the developers of fault models and test methods, and academia. The ten most important challenges are as follows:

- **BIST and DFT for digital and analog circuits**
- **Device under test (DUT) to ATE interface**
- **Mixed-signal instruments**
- **Failure analysis**
- **Test development**
- **SOC test methods**
- **MEMs, sensors, and new IC technologies**
- **New burn-in techniques**

One difficult challenge deserves special mention, because it is not covered in the Test Roadmap chapter. This is the whole area of the DUT-to-ATE interface. Increasing pincounts are leading to very large test heads in which the round-trip-delays for I/O pins are remaining in the vicinity of 6–8 ns. As frequencies increase above 500 MHz, this delay is unacceptable, which leads to the proposal that pin-electronics should have two transmission lines connected to each DUT pin to eliminate the problem. This creates the undesirable situation of loading the DUT outputs with 25 Ohm impedances. Fortunately, at these frequencies, data is often delivered in the form of packets, which allow more time for turn-around from O to I. Interface circuits must also be designed for low noise and matched delays on differential pins, while simulators should be developed for the path from the DUT through the package, the contactor, and across the loadboard to the pin electronics.

The trend of more system functionality on a single piece of silicon (SOCs) will increasingly blur the lines between traditional digital, analog, RF/microwave and mixed-signal devices. This trend will drive test equipment toward a single platform solution that can test whatever happens to find its way onto a single piece of silicon. The digital requirements for mixed-signal test equipment are the same as for purely digital chips and are shown in the Microprocessor and ASIC tables in the chapter.

The trend in test equipment is toward a modular high speed and high pincount, digital test platform where high performance analog/RF/microwave instruments can be added as needed. The analog test issues and test technology limiters are higher bandwidth, higher direct conversion sampling rates, higher dynamic range, lower noise floors, seamless integration of the digital and analog instruments and cost. Memory testing, previously excluded in the 1994 and 1997 SIA roadmaps, has been included for both commodity and embedded DRAMs, and for embedded FLASH memory testing. In future SOCs, memory testing will be challenging if external chip access is not readily available. BIST and built-in-self-repair for memories will be essential.

A section on high-frequency, serial communications device testing has been included, since this area is rapidly becoming important. Testing devices for applications such as SONET, Fibre channel and Firewire require test systems that have a small number of pins capable of generating and receiving differential signals up to 10 GHz with voltage swings as low as 100 mV. Differential DUT input signals must have timing skews as low as 10 ps. At the present time this kind of testing can only be done using expensive specialty instruments and not by general purpose ATE. It is almost impossible to predict how this fast moving field will develop through the Roadmap period to the year 2014, therefore a table showing test requirements was not attempted.

A section on the future of IDDQ testing has been included in the 1999 roadmap for the first time. This predicts that background leakage currents could result in IDDQ values approaching 1A by the year 2012. This will result in IDDQ ceasing to be a useful production test technique within the next few years, unless new IDDQ test techniques are developed. Some areas for R & D are listed.

The ultimate dream of test engineers is wafer-level testing and burn-in. Handling singulated die in a test and burn-in operation will always be cost prohibitive as compared to achieving the quality and reliability specifications at the wafer level. This leads to the concept of known-good-die (KGD) that is being actively studied by the Die Products Consortium (DPC) whose goals include reliability screens and test methods, developing an infrastructure for shipping and handling (waffle-pak, gel-pak, tape and reel). The DPC is also trying to overcome the perception that KGD technology is expensive, has little supportive manufacturing infrastructure, and cannot match the quality, reliability, and value of the equivalent packaged part. The development of wafer-level burn-in techniques is also an important goal. Unfortunately not much progress has been made in the area of wafer-level burn-in. Also, there are no known solutions to the problem of simultaneously probing thousands of pads at high frequencies.

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

Near Term Challenges

FIVE DIFFICULT CHALLENGES $\geq$100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Meeting device performance targets with available gate stack materials	Production worthy high-κ dielectrics and compatible gate materials will not be available.
Function integration at low V_{dd}	Crosstalk, substrate noise, and device performance difficult to optimize simultaneously at high clock rates and low V_{dd}.
Managing power, ground, signal, and clock on multilevel coupled interconnect	Despite the use of low–κ dielectrics, interconnect scaling is increasing coupling capacitance, crosstalk and signal integrity issues. Power, clock, and ground distribution will consume an increasing fraction of available interconnect.
Management of increasing reliability risks with the rapid introduction of new technologies.	Inadequate identification and modeling of failure modes in new materials, new operating regions (such as tunneling) and new SOC technologies (such as MEMS)
Integration of precision passive elements	Maintaining high Q, low noise, and tolerances of discrete components.

- **No gate dielectric available for 100 nm node (65 nm devices)**
- **Meeting device requirements at Low V_{dd}**
- **Management of reliability issues with many new materials**
- **Need for precision passive elements**

Long Term Challenges

FIVE DIFFICULT CHALLENGES *<100 nm / BEYOND 2005*	*SUMMARY OF ISSUES*
Overcoming fundamental scaling limits for current device structures	Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling
Integration choices for system on a chip	Cost effective process integration of many functions on a single chip
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variations
Design for manufacturability, reliability, and performance.	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, etc.
Low power, low voltage, high performance, and reliable nonvolatile memory element	NVM program and erase require voltages which are incompatible with highly scaled low voltage devices

- **Scaling limits will reduce performance of devices and memory cells.**
- **SOC issues will cause difficult integration problems as well as the need for smart design tools to design around process limitations.**
- **Atomic level fluctuations are causing unacceptable statistical variation.**

Analog and Mixed-signal Summary

- **Analog and mixed-signal difficulties are compounded at low voltages.**
- **Precision passive elements may require unique materials and more complex fabrication techniques.**
- **Crosstalk and noise issues will dominate at low voltages, high density, and high frequency.**

Analog and Mixed-signal Requirements

1	YEAR OF INTRODUCTION	*1999* *180 nm*	*2000* *165 nm*	*2001* *150 nm*	*2002* *130 nm*	*2003* *120 nm*	*2004* *110 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
2	Minimum Digital Supply Voltage (V)	**1.8–1.5**			**1.5–1.2**		**1.2–0.9**		**0.9–0.6**	**0.6–0.5**	**0.6–0.3**
3	Minimum Analog Supply Voltage (V)	**3.3–2.5**	**2.5–1.8**						**1.8–1.5**		**1.5**
4	RF Frequency (GHz)	**0.9–2.5**	**0.9–10**						**0.9–10**	**0.9–100**	

- **Excessive analog power dissipation under reduced signal swingconditions must be addressed.**

Memory and Logic Issues

- **Device scaling will end without new gate stack materials.**
- **SOC integration issues will put a greater demand on process innovation.**
- **Simultaneously satisfying I_{on} and I_{off} needs will require new materials and structures.**

Gate stack material is critical

Memory and Logic Requirements

Short Term Requirements

	Year of First Product Shipment Technology Generation	***1999 180 nm***	***2000 165 nm***	***2001 150 nm***	***2002 130 nm***	***2003 120 nm***	***2004 110 nm***	***2005 100 nm***	***Driver***
3	MPU / ASIC Half Pitch (nm)	230	210	180	160	145	130	115	
5	Min. Logic V_{dd} (V) (desktop)	**1.5 - 1.8**	**1.5 - 1.8**	**1.2 - 1.5**	**1.2 - 1.5**	**1.2 - 1.5**	**0.9 - 1.2**	**0.9 - 1.2**	**M Gate**
6	Tox equivalent (nm)	**1.9–2.5**	**1.9–2.5**	**1.5-1.9**	**1.5-1.9**	**1.5-1.9**	**1.2-1.5**	**1.2-1.5**	**M Gate**
7	Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] High Performance.	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**M Gate**
8	Maximum I_{off} @ 25 °C (nA/µm) (For min. L device) High Performance.	**5**	**7**	**8**	**10**	**13**	**16**	**20**	**M Gate**
9	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	**0**	**27**	**42**	**49**	**65**	**71**	**75**	**M Gate M & A 1/2**
10	Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] Low Power	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**490/230**	**A Gate**
11	Maximum I_{off} @ 25 °C (pA/µm) (For min. L device) Low Power	**5**	**7**	**8**	**10**	**13**	**16**	**20**	**A Gate**
12	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	**0**	**31**	**50**	**60**	**75**	**81**	**84**	**A Gate M & A 1/2**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Long Term Requirements

		2008 ***70 nm***	***2011*** ***50 nm***	***2014*** ***35 nm***	***Driver***
3	MPU / ASIC Half Pitch (nm)	80	55	40	
5	Min. Logic V_{dd} (V) (desktop)	**0.6 - 0.9**	**0.5 - 0.6**	**0.3 - 0.6**	**M Gate**
6	Tox equivalent (nm)	**0.8-1.2**	**0.6-0.8**	**0.5-0.6**	**M Gate**
7	Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] High Performance.	**750/350**	**750/350**	**750/350**	**M Gate**
8	Maximum I_{off} @ 25 °C (nA/µm) (For min. L device) High Performance.	**40**	**80**	**160**	**M Gate**
9	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	**87**	**95**	**97**	**M Gate** **M & A 1/2**
10	Nominal I_{on} @ 25 °C (µA/µm) [NMOS/PMOS] Low Power	**490/230**	**490/230**	**490/230**	**A Gate**
11	Maximum I_{off} @ 25 °C (pA/µm) (For min. L device) Low Power	**40**	**80**	**160**	**A Gate**
12	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	**92**	**97**	**98**	**A Gate** **M & A 1/2**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Device Reliability

- **Reliability infrastructure is not prepared for new material introductions.**
- **Lead time for new technologies is long for reliability evaluations.**

Reliability Needs

Reliability Short Term Technology Requirements

Year of Introduction	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
Customer Reliability Expectations (@85°C Junction Temperature)								
Early Failures (ppm) (First 4000 operating hours)	**50-2000**	**50-2000**	**50-2000**	**50-2000**	**50-2000**	**50-2000**	**50-2000**	
Long Term Reliability (FITs = Failures in 1E9 hours) (5-10 Years)	**10-100**	**10-100**	**10-100**	**10-100**	**10-100**	**10-100**	**10-100**	
Soft Error Rate (FITs)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	
Relative Failure Rate per Transistor (normalized to 180 nm)	**1**	**1**	**1**	**.62**	**.62**	**.62**	**.34**	
Relative Failure Rate per m of Interconnect (normalized to 180 nm)	**1**	**1**	**1**	**.51**	**.51**	**.51**	**.34**	
System on A Chip Reliability Prediction	**Logic & Memory**			**Micro Machine**			**Micro Optics**	
Failure Analysis Cycle Time (days)	**1-12**	**1-12**	**1-12**	**1-10**	**1-10**	**1-10**	**1-10**	Failure Location

Note: Reliability requirement includes chip and package failures. Additional parameters (such as temperature cycling and humidity) need to be specified for package reliability.

Reliability Long Term Technology Requirements

Year of Introduction	2008 70 nm	2011 50 nm	2014 35 nm	Driver
Customer Reliability Expectations (@85°C Junction Temperature)				
Early Failures (ppm) (First 4000 operating hours)	**50-2000**	**50-2000**	**50-2000**	
Long Term Reliability (FITs = Failures in 1E9 hours) (5-10 Years)	**10-100**	**10-100**	**10-100**	
Relative Failure Rate per Transistor (normalized to 180 nm)	**.16**	**.07**	**.03**	
Relative Failure Rate per m of Interconnect (normalized to 180 nm)	**.18**	**.10**		
Soft Error Rate (FITs)	**1000**	**1000**	**1000**	
System on A Chip Reliability Prediction	**Micro Biological**			
Failure Analysis Cycle Time (days)	**1-10**	**1-10**	**1-10**	

Solutions Exist	☐	*Solutions Being Pursued*	🟨	*No Known Solutions*	🟥

FRONT END PROCESSES

Summary

This international roadmap has identified the end of conventional scaling for CMOS structures unless new materials and devices are introduced on an aggressive time scale. The immediate grand challenge for FEP is the identification and introduction of new silicon compatible high κ dielectric and electrode materials for formation of the gate stack by the year 2004. Although these new materials will not guarantee scaling to the end of the present Roadmap, where new device structures will be needed, they will permit the realization of two nodes on the Roadmap. In addition, the knowledge base that will be developed by introducing these new silicon compatible materials will accelerate the learning curve for the introduction of new materials that will likely be required to realize the needed new device concepts for future scaling.

New, high-κ dielectric and associated electrode materials are also needed for DRAM storage capacitors, in order to permit continued scaling of the DRAM storage node area. In the long term continued memory scaling may require new storage concepts to replace the tradition stacked or trench storage capacitor structures now in use.

In the doping area, on a short-term basis (< 2004) the realization of ultra-shallow abruptly doped junctions is needed, as is the need to achieve very high, non-equilibrium degrees of dopant activation in the contact junctions and in the dual-doped polysilicon gate electrodes. The realization of these objectives will allow continued near-term device scaling in conjunction with the incumbent silicon oxynitride gate dielectric materials. In the longer term an important challenge is the achievement elevated contact structures with high degrees of dopant activation in the low thermal budget regime required for CMOS integration of high-κ gate stacks having dual metal gate electrodes.

In the etch area, future challenges are largely driven by decreasing critical dimensions (CDs) and new materials, notably metal gates and deposited high-κ dielectrics, that will be used in front end processing. The most challenging FEP etch technical requirements are maintaining low CD bias and high CD uniformity at continually larger wafer diameters, and obtaining the required etch selectivity and etch profiles for new front end materials. In addition, line edge roughness is expected to play an increasingly important role in overall transistor performance.

In the surface preparation area, the near-term challenges include the continued, cost-effective, reduction in post-clean particle, elemental, and structural defects. In the long term the challenges include the integration of both aqueous- and dry-surface preparation techniques with the new process architectures required for CMOS integration of the required new high-κ, elevated contact devices.

Starting materials faces the challenge of achieving future cost-effective large area silicon substrates, as well as alternative substrate materials such as SOI that may be required to achieve the continued performance and productivity gains historically associated with Moore's law.

These new materials and processing requirements have been identified and documented. The required process development and manufacturing integration needs present a challenge that will require the melding of efforts by university, national laboratory, semiconductor device, and semiconductor equipment industries. This is especially challenging when placed in the context of SOC. Here, the challenge is further complicated by the necessity to integrate memory (DRAM, FeRAM, Flash and etc.), analog, logic, RF, and other device technologies. The newly developed materials and processes must be compatible with SOC.

In the longer term (> 2008) it is anticipated that the continued scaling of the MOS transistor while still possible, will yield a device that is no longer capable complying with the anticipated low voltage high-speed IC chip level requirements. From this standpoint, scaling is anticipated to come to an end, dictated by fundamental physical limits. For this reason, it is anticipated that continued chip level scaling will require the development of innovative new device concepts. It is further anticipated that the materials knowledge base developed in the interim will greatly expand the scope of the innovative arena in which the invention of such new device concepts may take place.

In conclusion, new materials and processes are not the total solution to the future, but they will be required no matter what the approach. The industry has been able to squeeze the best out of a knowledge base developed during the past century. However, that knowledge base is limited and the time has come when new knowledge is needed and new solutions developed and engineered. In the area of front end processing, new resources will be required on an aggressive time scale to meet the new challenges. The challenges presented here are just that—*challenges*. Although fundamental limits are being approached for the materials and devices currently used, these same limits may not apply to new materials and devices.

High-risk approaches need to be combined with evolutionary approaches and the development of new knowledge to meet the challenge. This will require a partnership between the industry, universities and national laboratories on an international scale.

LITHOGRAPHY

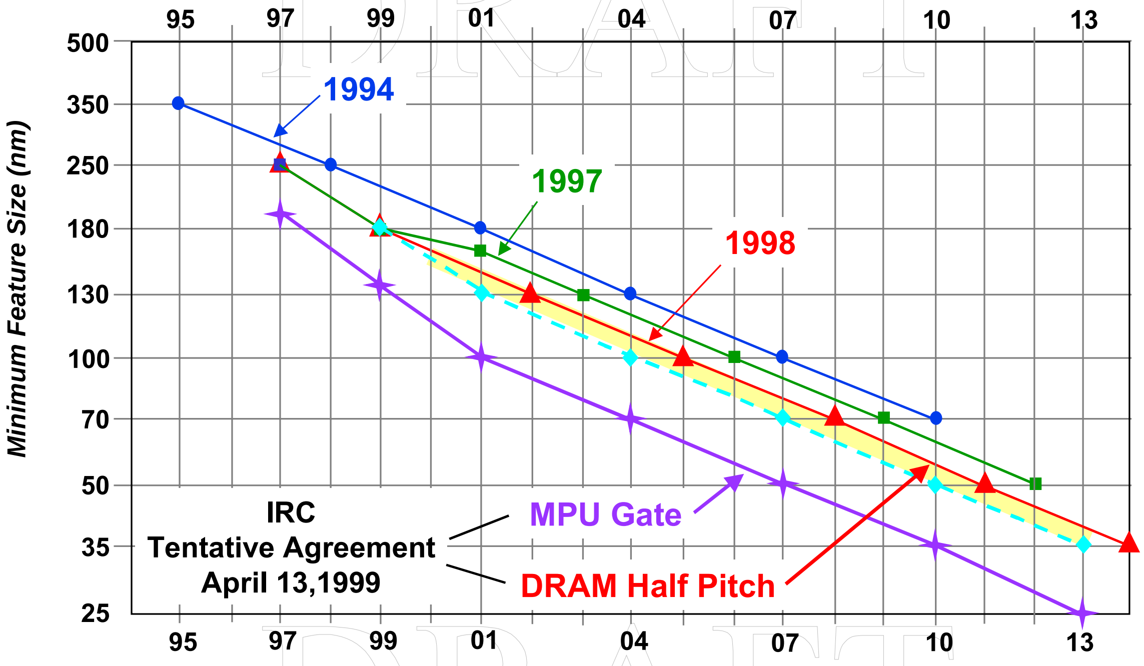
Roadmap Timing

- **Timing has been one of biggest concerns for the Lithography TWGs: 2-year versus a 3-year cycle.**
- **Discussed extensively at Japan and USA TWG meetings**
- **Tentative agreement reached in Munich, April 13th, with IRC:**

Feature size (printed in resist)	1999	2002	2005	2008	2011	2014
DRAM Half Pitch (nm)	180	130	100	70	50	35
MPU Gate (nm)	140	90	65	45	30	20

The key concern is the timing of the 130 nm node…
should it be 2002 or 2001?

SIA Roadmap Acceleration



Mask Capability

- **Mask capability is a major limiter to progress.**
    - Writers: Accuracy, CD Control, Feature Size, OPC, Data Volume, MEF, Image Placement
    - Inspection: Defect size, Actinic Capability and PSM
    - Repair: Lacking technology/supplier and PSM
    - Cost/Price: Rapid Escalation $5k ➨ $50k

Needs major focus, paradigm shift, global collaboration!

Chip Size

- **Chip sizes in 1997 and 1998 Roadmaps are much too large.**
- **Drives mask and stepper suppliers in wrong direction.**
- **RCG subcommittee formed 1Q99 to study issue and make recommendations. Findings are:**
  - Chip designs are driven by performance and cost.
  - Cost to first order is driven by chip size.
  - In DRAM and MPU business, next generation chips are introduced to production when cost/function approaches that of current generations. This drives constant chip size.
  - Recommended chip sizes are:

Area (mm^2)		Sample	Production	Ramp	Peak
DRAM (Flat)		300	150	75	38
MPU (Flat)	CP		340	160	75
	MP			195	92
	HP			440	215

22x22mm field captures all requirements.

- **Proposal affords significant relief for lithography tools and masks.**

Need industry feedback, IRC adoption!

Difficult Challenges

Five Difficult Challenges ≥ 100 nm Before 2005	**Summary of Issues**
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market
Lithography technology consensus (193 nm + RET, 157 nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes Achieving global consensus among technology developers and chip manufacturers
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks Achieving ROI for industry (chipmakers, equipment and materials suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option

NGL–Next generation lithography

Five Difficult Challenges < 100 nm Beyond 2005	**Summary of Issues**
Mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes
Metrology and inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection and characterization
Cost control and return on investment (ROI)	Development of innovative technologies, tools, and materials to maintain historic productivity improvements Achieving constant/improved throughput with post-optical technologies Achieving ROI for industry (chipmakers, equipment and materials suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements	Development of new and improved alig nment and overlay control methods independent of technology option

Technology Requirement Overview

Year of Introduction	**1999**	**2002**	**2005**	**2008**	**2011**
Minimum Feature Size (nm) Dense Lines (printed in resist)	180	130	100	70	50
Isolated Lines (nm) (printed in resist)	140	90	65	45	30
Gate CD Control (nm) (3 sigma post etch)	13	8	6	4	3
Overlay (nm) (mean + 3 sigma)	65	45	35	25	20
Minimum Field Size (mm x mm)	22 x 22	22 x 22	22 x 22	22 x 22	22 x 22
Mask Size (mm) (square / diameter)	152	152	152 / 200	152 / 200	152 / 200
Defect Density (Defects per layer/m^2 @ nm)	80 @ 60 nm	60 @ 40 nm	50 @30 nm	40 @20 nm	30 @15 nm

INTERCONNECT

The 1999 International Technology Roadmap for Interconnects addresses both short term (1999-2005) and long term (2008-2014) technology needs for three specific classes of products: Microprocessors (MPU), System-on-a-Chip (SOC) and Dynamic Memory (DRAM). For MPUs, local, intermediate and global wiring pitches/aspect ratios are highlighted to differentiate the performance and technology needs. Since local and intermediate wiring levels tend to scale in length, RC delay is dominated by global interconnects, and in the long term new design or technology solutions (such as coplanar waveguides, free space RF, optical interconnects) will be needed to overcome the performance limitations of traditional interconnects. Inductive effects will also become increasingly important as frequency of operation increases, and additional metal patterns or ground planes may be required for inductive shielding. As voltage continues to scale, crosstalk has become an issue for all clock and signal wiring levels, and the near term solution adopted by the industry is the use of thinner metallization to lower sidewall capacitance. This approach is particularly effective for lower resistivity copper metallization, where reduced aspect ratios can be achieved with less sacrifice in resistance as compared with aluminum metallization. The 1999 Roadmap reflects this design trend by featuring reduced aspect ratios and less aggressive scaling of dielectric constant (as an alternative means of reducing capacitance) in comparison with the 1998 Interconnect roadmap. The latter change is particularly welcome due to the difficulty in integrating low κ dielectrics into a damascene architecture.

System-on-a-Chip technology requirements reflect similar vertical scaling trends but less aggressive reduction in dielectric constant as compared with the MPU. Thus, new technologies developed for MPU products can be extended to next generation SOCs, providing shorter and lower cost development cycles. However, the need for merged memory and/or passive components in SOC applications presents significant material and process integration challenges. For DRAM interconnect technology, dense metal pitch and high aspect ratio (HAR) contacts will continue to provide the most significant challenges, while the introduction low κ dielectric materials and copper metallization lag MPU and SOC needs by several generations. However, the potential cost benefits of copper and improved linewidth control of damascene versus aluminum metallization could potentially accelerate copper insertion into DRAM products.

For the past decade, introduction of new interconnect materials and/or processes at each successive generation has become more the norm than the exception, and this trend is expected to continue in the race for improved performance, reliability and density. Near term dielectric needs include lower permittivity materials for wire insulators and copper diffusion barriers, higher permittivity materials for decoupling capacitors and materials with high remanent magnetization for ferroelectric memories. Integration of these new materials presents a formidable challenge as thermal, mechanical and electrical properties may be incompatible with current process techniques. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials may be required which have sufficient optical contrast to serve as low loss waveguides.

Conductor applications will be characterized by a rapid conversion to copper at the 130nm technology node and beyond to leverage improved resistivity and reliability. While current copper damascene processes utilize PVD barrier and seed deposition techniques, continued scaling of feature size requires CVD barrier and seed deposition solutions at the 100nm node. Electrochemical deposition (ECD) of copper is expected to extend to 100nm and beyond, but thinner barrier and seed layers will be needed to maintain effective resistivity and enable ECD fill. In the longer term, barrier-less or surface segregated barrier structures and CVD copper fill of minimum features may be necessary; breakthrough material and process solutions such as low k dielectrics which inhibit copper diffusion, electroless or seedless electrochemical deposition and PVD reflow approaches offer potential alternatives. DRAM applications are expected to utilize tungsten and aluminum alloy wiring until the 100nm node, driving a need for improvements in tungsten fill of HAR contacts and defect density learning.

In the near term, DRAM lithography requirements will place stringent demands on planarization, and continuous improvement in oxide CMP and post-CMP defect reduction will be needed. For copper CMP, minimization of erosion and dishing will become even more important as thickness is scaled and low k dielectrics with low density and poor mechanical strength are introduced. Low damage CMP and improvements in post-CMP cleanup will be critical to achieving the low defect densities required in future devices. The transition to copper and low k dielectrics will also drive a need for improved etch profile control and selectivity to etch stop and diffusion barriers. Etch, resist strip and post-etch cleans must be developed that do not degrade future low k dielectrics. Minimization of electrical damage to gate dielectrics during etch and deposition processes will also continue to be of concern, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

Dimensional control is one of the key challenges for present and future interconnect technology generations; for damascene architectures both pattern, etch and CMP must be tightly controlled. Metrology will play a critical role in the measurement of high aspect ratio feature size and process quality (e.g. residue removal) as well as endpoint for CMP; new techniques are needed for high throughput imaging of HAR structures and more accurate CMP endpoint determination. New metrology techniques are also needed for inline monitoring of adhesion and defectivity; in situ process control will become increasingly important as wafer size increases and more devices (e.g. revenue) are placed at risk in each process step.

Environment, safety and health (ESH) is another important crosscut issue for interconnects. Continuous improvement is needed in methods for treating and recycling CMP slurries and copper electroplating baths. Replacement of wet chemical cleans by dry processes will also continue to be emphasized; this conversion will be challenging due to the introduction of new metal/dielectric materials. The new materials, precursors and processes that will be required for future low k dielectrics and CVD metal depositions must also be carefully screened for ESH issues during the early phase of development, well before adoption by the industry.

In summary, the near-term most difficult challenges for interconnects include the rapid introduction and integration of new materials and processes, dimensional control, physical/electrical reliability of interconnect structures and back-end-of-line (BEOL) processes with low or no front-end-of-line (FEOL) impact. The introduction of new low k dielectrics, CVD metal barrier/seed layers, imbedded memory (especially ferroelectric) and passive elements for SOC provide significant BEOL process and process integration challenges. In the longer term, dimensional control and etch/measure/fill of higher aspect ratios features will become even more critical and new materials such as porous low k dielectrics and CVD metals will continue to play a key role at local and intermediate levels. At the 50nm node, feature size effects such as electron scattering will increase the effective resistivity and new conductor technologies may be required. For global wiring levels, new interconnect solutions such as rf or optical will be required, bringing even more material and process integration challenges.

MPU Interconnect Short Term Technology Requirements

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
MPU _ pitch	230	210	180	160	145	130	115	
MPU gate length (nm)	140	120	100	85	80	70	65	
Number of metal levels	6-7	7	7-8	7-8	7-8	8	8	
Number of optional levels – ground planes/capacitors	2	2	2	2	2	2	2	
Jmax (A)/cm^2 – wire	6E5							
Jmax (mA) – via	0.36							
Local wiring pitch (nm)	500	450	405	365	330	295	265	
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2			
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7	
Cu local dishing (nm), 5% x height	18	16	15	14	13	12	11	
Intermediate wiring pitch (nm)	640	575	520	465	420	375	340	
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6			
Intermediate wiring dual damascene A/R (Cu)	4.1	4.2	4.3	4.3	4.4	4.5	4.6	
Cu intermediate dishing (nm), 15 micron line, 20% x height	102	98	94	84	80	75	71	
Dielectric erosion, intermediate, 50% density, 15% x height	77	74	71	63	60	56	53	
Minimum global wiring pitch (nm)	1050	945	850	765	690	620	560	
Global wiring A/R (Al)	2	2.1	2.2	2.3	2.4			
Global wiring A/R (Cu)	1.5	1.6	1.7	1.7	1.8	1.9	2	
Cu global dishing (nm), 15 micron line, 20% x height	158	151	145	130	124	117	112	
Minimum metal effective resistivity (-cm) Al wiring*	3.3	3.3	3.3	3.3	3.3			
Minimum metal effective resistivity (-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2	
Barrier/cladding thickness (conformal) (nm)	23	19	16	13	11	7	3	
Interlevel metal insulator - effective dielectric constant (κ)	3.5 - 4.0	3.5 - 4.0	2.7 - 3.5	2.7 - 3.5	2.2 - 2.7	2.2 - 2.7	1.6 - 2.2	

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

MPU Interconnect Long Term Years Technology Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
MPU _ pitch	80	55	40	
MPU gate length (nm)	45	32	22	
Number of metal levels	9	10	11	
Number of optional levels – ground planes/capacitors	2	2	2	
Jmax (A)/cm^2 – wire				
Jmax (mA) – via				
Local wiring pitch (nm)	185	130	95	
Local A/R (for Cu)	1.9	2.1	2.3	
Cu local dishing (nm), 5% x height	9	7	5	
Intermediate wiring pitch (nm)	240	165	115	
Intermediate wiring dual damascene A/R (Cu)	4.8	5.1	5.4	
Cu intermediate dishing (nm), 15 micron line, 20% x height	55	43	33	
Dielectric erosion, intermediate, 50% density, 15% x height	0	0	0	
Minimum global wiring pitch (nm)	390	275	190	
Global wiring A/R (Cu)	2.4	2.7	3.0	
Cu global dishing (nm), 15 micron line, 20% x height	94	74	57	
Minimum metal effective resistivity (-cm) Cu wiring*	1.8	≤1.8	≤1.8	
Barrier/cladding thickness (conformal) (nm)	0	0	0	
Interlevel metal insulator - effective dielectric constant (κ)	1.5	≤1.5	≤1.5	

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

SOC Interconnect Short Term Technology Requirements

YEAR OF INTRODUCTION “TECHNOLOGY NODE”	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	*DRIVER*
MPU _ pitch (nm)	**230**	**210**	**180**	**160**	**145**	**130**	**115**	**m & a _**
ASIC gate (nm)	**180**	**165**	**150**	**130**	**120**	**110**	**100**	**A Gate**
Number of metal levels	**6**	**6**	**7**	**7**	**7-8**	**8**	**8**	
Number of optional levels – passive elements	**0**	**0**	**2**	**2**	**4**	**4**	**4**	
Jmax wire (A/cm^2)								
Jmax via (mA)								
Local wiring pitch (nm)	**450**	**405**	**360**	**325**	**290**	**260**	**230**	
Local wiring A/R (for Al)	**2**	**2**	**2.1**	**2.1**	**2.2**			
Local wiring A/R (for Cu)	**1.4**	**1.4**	**1.5**	**1.5**	**1.6**	**1.6**	**1.7**	
Intermediate wiring pitch (nm)	**560**	**505**	**450**	**405**	**360**	**325**	**285**	
Intermediate wiring A/R (Al)	**2.2**	**2.3**	**2.4**	**2.5**	**2.6**			
Intermediate via A/R (Al)	**2.8**	**2.8**	**2.9**	**2.9**	**3.0**			
Intermediate wiring dual damascene A/R (Cu)	**4.1**	**4.2**	**4.3**	**4.3**	**4.4**	**4.5**	**4.6**	
Global wiring pitch (nm)	**900**	**810**	**720**	**650**	**580**	**520**	**460**	
Global wiring A/R (Al)	**2.2**	**2.3**	**2.4**	**2.5**	**2.6**			
Global wiring A/R (Cu)	**1.6**	**1.6**	**1.7**	**1.7**	**1.8**			
Global wiring dual damascene A/R (Cu)	**3.8**	**3.9**	**4.0**	**4.0**	**4.1**	**4.2**	**4.3**	
Process control metric								
Xtalk metric								
Interlevel metal insulator - effective dielectric constant (κ)	**3.5 - 4.0**	**3.5 - 4.0**	**2.7 - 3.5**	**2.7 - 3.5**	**2.2 - 2.7**	**2.2 - 2.7**	**1.6 - 2.2**	

SOC Interconnect Long Term Technology Requirements

YEAR OF INTRODUCTION “TECHNOLOGY NODE”	*2008 70 nm*	*2011 50 nm*	*2014 35 nm*	*DRIVER*
MPU _ pitch (nm)	**80**	**55**	**40**	**M & A _**
ASIC gate (nm)	**70**	**50**	**35**	**A Gate**
Number of metal levels	**9**	**10**	**11**	
Number of optional levels – passive elements	**6**	**6**	**6**	
Jmax wire (A/cm^2)				
Jmax via (mA)				
Local wiring pitch (nm)				
Local wiring A/R (for Cu)				
Intermediate wiring pitch (nm)	**210**			
Intermediate wiring dual damascene A/R (Cu)	**4.8**			
Global wiring pitch (nm)	**330**	**240**		
Global wiring dual damascene A/R (Cu)	**4.5**	**4.9**		
Process control metric				
Xtalk metric				
Interlevel metal insulator - effective dielectric constant (κ)				

DRAM Interconnect Short Term Technology Requirements

YEAR OF INTRODUCTION “TECHNOLOGY NODE”	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM _ pitch	**180**	**165**	**150**	**130**	**120**	**110**	**100**	**D1/2**
Number of metal levels	**3**	**3**	**3**	**3-4**	**4**	**4**	**4**	
Contact A/R – stacked capacitor	**6.3**	**6.7**	**7.1**	**7.5**	**8.0**	**8.5**		
Local wiring pitch (nm) non-contacted	**360**	**330**	**300**	**260**	**240**	**210**	**200**	
Specific contact resistance (Ω-cm^2)	**6E-7**			**3E-7**			**2E-7**	
Specific via resistance (Ω-cm^2)	**7E-9**			**2E-9**			**1E-9**	
Metal effective resistivity	**3.3**	**3.3**	**3.3**	**3.3**	**3.3**	**3.3**	**2.2**	
Interlevel metal insulator - effective dielectric constant (κ)	**4.1**	**4.1**	**4.1**	**3.0 - 4.1**	**3.0 - 4.1**	**3.0 - 4.1**	**2.5 - 3.0**	

DRAM Interconnect Long Term Technology Requirements

YEAR OF INTRODUCTION “TECHNOLOGY NODE”	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DRAM _ pitch	**70**	**50**	**35**	
Number of metal levels	**4**	**4**	**4**	
Contact A/R – stacked capacitor				
Local wiring pitch (nm) non-contacted				
Specific contact resistance (Ω-cm^2)	**8E-8**	**3E-8**	**2E-8**	
Specific via resistance (Ω-cm^2)	**6E-10**	**3E-10**	**1.5E-10**	
Metal effective resistivity	**2.2**	**2.2**	**2.2**	
Interlevel metal insulator - effective dielectric constant (κ)	**2.5 - 3.0**	**2.0 - 2.5**	**2.0 - 2.3**	

FACTORY INTEGRATION

Scope

The factory turns ideas into products and delivers them taking full advantage of available technology and organizational efficiencies. It is the factory that must consider the realities of economic, ergonomic, and technology constraints and still continually increase productivity. The semiconductor industry has maintained steady productivity growth (25–30%/year reduction in cost/function of products) despite escalating factory costs (20%/year). The industry growth has been driven by improvements to feature size, wafer diameter, yield, and productivity (equipment and operations). However, annual gains from yield and wafer diameter are diminishing, thus requiring greater emphasis on the overall factory productivity. As a result, increased significance must be placed on fully exploiting equipment and operational productivity. Factory integration implies everything from product design to delivery and not just the wafer fabrication operations. It also implies that it is an integrated supply chain that works together to maintain this productivity growth, and no single link can be made responsible.

The semiconductor industry is currently entering a new era of manufacturing, enabled by the pending conversion of the industry to 300-mm wafers. This era is characterized by the confluence of historical needs with several new factors. The new factors include manufacture of increasingly complex technologies, subject to more demanding requirements (ESH, local codes, etc.), use of more highly segmented and diversified business models employing globally distributed resources, while simultaneously manufacturing an increasing array of complex products. The overarching drivers shaping this shift are economics, ergonomics, environment, safety, health, local codes, and availability of new manufacturing technologies.

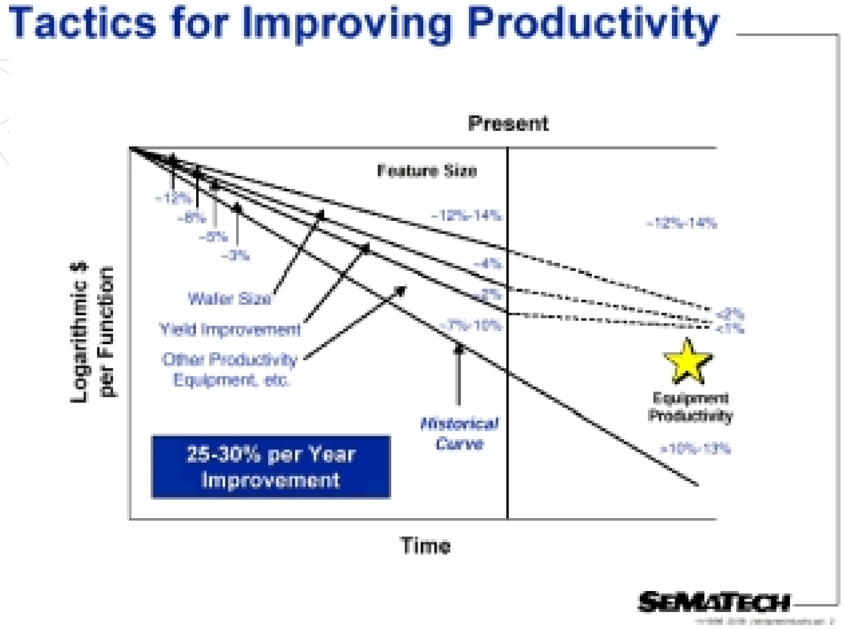
This understanding led to the mission statement: *To identify the "integrated" needs of factories that will be designing, fabricating, assembling, testing, and delivering semiconductor products based on technology successes at each node in the Roadmap within the constraints—time, cost, quality plus EHS*. The productivity improvement is expected for the product and not just the density of silicon devices on the wafer. Moore's law expects cleverness in design plus cleverness in production to increase the functionality and reduce the cost per function. To do this the two disciplines will work together, not in isolation. This may eventually lead to a repartitioning of the traditional matrix of design, process integration, and fab, assembly, and test organizations. The factory integration chapter should address both the economic and the staffing (people) issues that the availability of new technology creates. Difficult challenges for the factory come from change and where change is expected an increase in the pace of change. Economic and ergonomic requirements change, the environment, the market and customers expectations for service change. Technology changes both within the semiconductor community and outside of it. All these changes can affect productivity positively and negatively.

Factory Integration is the assembly of production equipment, people and facilties, aided by manufacturing systems with knowledge-based management tools and guided by factory operations policies to profitably produce complex products for a time-sensitive market. The conversion to 300 mm wafers and larger process chambers, will affect both operational and equipment maintenance tasks and increase the attention given to ergonomic solutions in more automated factories. Employee safety and compliance to local codes will continue to mold factory characteristics, as will availability of new manufacturing and information technologies.

Semiconductor factories addressed in this chapter will be limited to those facilities used for high-volume/high-product-mix and high-volume/low-product-mix business models. Attention will go primarily to wafer fabrication issues, but a challenge to the packaging and test technology working groups is to help add the assembly and testing aspects to round out the complete factory. The reason for addressing all aspects of manufacturing from design to delivery is to assure that all opportunities for productivity gains are addressed.

The following needs in pursuit of safe, flexible and productive factories will be to:

- **Increase factory extendibility, flexibility, and scalability**
- **Increase production tool reliability and availability**
- **Reduce ramp time for new and retrofitted factories**
- **Reduce factory costs**
- **Improve factory optimization for different business models (high-volume/high-product mix and low-volume/low-product mix)**



Difficult Challenges

The factory is composed of operations, production equipment (process and metrology), material handling systems, factory systems (software), and facilities. While including production equipment and process technologies that are strongly linked to the technology nodes, these *manufacturing systems* are more driven by subtle, time-dependent factors that disruptively impact factories during wafer-size changeovers. Thus, the Difficult Challenges associated with Factory Integration are grouped into three categories that span all technology nodes of the roadmap.

DIFFICULT CHALLENGES	SUMMARY OF ISSUES
Complexity Management	Rapidly changing business needs and globalization trends ♦ Increasing rate of new product and technology introductions ♦ Globally disparate factories run as “single –virtual factory” ♦ Need to meet regulations in different geographical areas Increasing process and product complexity ♦ Explosive growth of data collection/analysis requirements Large wafers and carriers driving ergonomic solutions ♦ Increasing expectations for material handling automation systems Increased reliance on integrated factory systems with increased capabilities ♦ Multiple system interdependencies ♦ Co-existence of new factory systems with existing systems
Factory Optimization	Meet customer on-time delivery ♦ Balance throughput and cycle time ♦ Reduction in time to ramp factories, products, and processes Improve Overall Factory Effectiveness (OFE) ♦ Need to improve production equipment, AMHS, factory systems, facilities, and factory operations effectiveness Improve factory yield ♦ Parametric variation reduction ♦ Control of production equipment and factory systems to improve yields Reducing product and operation cost ♦ Minimum waste and scrap And continue to satisfy all local, state and federal regulations
Extendibility, Flexibility, and Scalability	Reuse of building, production and support equipment and factory systems Factory designs that support rapid process and technology changes and retrofits without causing major downtimes to operations at reasonable cost. ♦ Understand up-front costs [model] to incorporate “EFS” ♦ Understanding features to include and not to include ♦ Minimize downtime to ongoing operations Increasingly tighter ESH/Code requirements Increasing purity requirements for process and materials

ASSEMBLY AND PACKAGING

Scope

- **Market sectors aligned with NEMI**
- **Expanded discussion on wafer level packaging**
- **Expanded reliability section**
- **Thermal management**
- **High density substrates**
- **RF and mixed-signal packaging**
- **Multi-chip packaging/modules**

New Material

- **System on chip (SOC)**
- **Electro-migration limits of eutectic flip chip bumps**

Key Difficult Challenges

- **Major categories maintained**
- **Additions**
  - Packaging of Cu/low κ IC
  - Thermal
  - Design for high density digital/mixed-signal packaging
  - Manufacturability/reliability of large body packages

Technology Requirements

- **Cost**
  - Widespread use of plastic ball grid array (PBGA) creates cost pressure on quad flat pack (QFP) and CBGA
  - 20-30% reduction
- **Chip size**
  - Cost performance, high performance and memory reduced substantially
- **Increased chip to board frequency**
  - Realization of PC133 BUS
- **Moderate change to pin count**
- **Removed pad count**
  - Large power/group connections available with area array
- **Overall package profile replaces package thickness**

Flip Chip Substrate Fan Out Technology Requirements

- **Cost Performance and high performance only**
  - Minimize pad pitch changes to avoid new test probe head at each generation
- **Depopulated outer row to increase fan out line width and spacing (such as 42 µm versus 34 µm for 1999)**

Summary

- **Invaluable input from international participants**
- **More work needed on cross-cut needs**
- **Industry feedback important**

ENVIRONMENT, SAFETY, AND HEALTH

Scope

BACKGROUND The semiconductor industry views responsible performance in environment, safety, and health (ESH) as critical to success. Continued ESH improvement is a major consideration for semiconductor manufacturers, whose integrated business approach to ESH employs strategies that are integrated with manufacturing technologies, products, and services. This integrated approach is structured around the belief that good business stewardship includes an active awareness and commitment to responsible environmental, safety, and health practices. Addressing these areas aggressively has resulted in the industry being an ESH leader as well as a technology leader. Now, as a result of global collaboration within this industry, the first International Roadmap for ESH in the semiconductor industry has been developed. This roadmap identifies R&D challenges that may impact ESH as new technology requirements are identified.

SIGNIFICANCE OF THE ROADMAP As the industry grows in size and its technology advances toward finer patterning and larger wafer sizes, the natural trend would be to see similar increases in use of chemicals and water and energy resources. For both engineers and research scientists in the industry, this Roadmap identifies ESH R&D challenges that occur as new design, wafer processing and assembly technologies are created. It also proposes possible technology and management systems to meet the challenges.

EXPECTATIONS Giving focus to research centers, suppliers and semiconductor manufacturers will provide direction toward solutions. Integration of ESH into manufacturing and business practices is clearly a priority. A high order of success and improvement requires that ESH must be integral to the thoughts and actions of process, equipment, facilities engineers, and university researchers. These improvements must meet local, national, and international needs, with positive impact on cost, technical performance, and product timing in conjunction with the minimization of risk, public and employee health, and the environment. Solutions must be timely, yet far reaching, if our long-term success is to be assured. The combined efforts of international initiatives and other notable ESH focused entities sponsored by the semiconductor industry, universities, and governments will be manifested in the internationalization of this Technology Roadmap for Semiconductors.

Difficult Challenges

There are five global ESH challenges that are essential to a synergistic ESH strategy and must be integrated into the technical thrust areas: *Chemicals, Materials and Equipment Management, Climate Change Mitigation, Resource Conservation, Worker protection, and ESH Design and Measurement Methods.*.

Chemicals, Materials, and Equipment Management must provide timely ESH information to equipment design engineers and equipment users regarding the environmental, safety, and health characteristics of potential new process chemicals and materials. This information is essential to the selection of optimal chemicals and materials for function and ESH impact with respect to reaction product emissions, health and safety properties, materials compatibility with both equipment and other chemical components, flammability and reactivity while minimizing unnecessary business impact after processes are developed and in production.

Climate Change Mitigation is a major consideration because it potentially could limit the use of energy and chemicals essential to the manufacturing process.

Worker Protection is always among the top priorities for our industry. As more is known world-wide about potential impacts of the work environment on health and safety, technology improvements need to be made in facilities, equipment, personal protective equipment, and training.

Resource Conservation (water, energy, chemicals, and materials) will grow in importance with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. To address the above issues in a cost-effective and timely way, improved

ESH Design and Measurement Methods are needed to enable a broader set of people to make sound, balanced, choices and decisions.

Near Term Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2005	SUMMARY OF ISSUES
Chemicals, Materials, and Equipment Management	**Chemical Data Collection** Need to document and make available environment, safety, and health characteristics of chemicals. **New Chemical Assessment** Need for quality rapid assessment methodologies to ensure that new chemicals can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation. **Environment Management** Need to develop effective management systems to address issues related to disposal of equipment, and hazardous and non-hazardous residue from the manufacturing process.
Climate Change Mitigation	**Reduce Energy Use Of Process Equipment** Need to design energy efficient larger wafer size processing equipment. **Reduce Energy Use Of The Manufacturing Facility** Need to design energy efficient facilities to offset the increasing energy requirements of higher class clean rooms. **Reduce High Global Warming Potential (GWP) Chemicals Emission** Need ongoing improvement in methods that will result in emissions reduction from GWP chemicals.
Worker Protection	**Equipment Safety** Need to design ergonomic and safe equipment. **Chemical Exposure Protection** Increase knowledge base on health and safety characteristics of chemicals and materials used in the manufacturing and maintenance processes, and of the process byproducts and implement safeguards to protect the users of the equipment and facility.
Resource Conservation	**Reduce Water , Energy, Chemicals, and Materials Use** Requirements for large amounts of water, energy, chemicals, and materials limit sustainable growth. **Waste Recycle** Increase in resource use as the result of increasing process complexity will require that efficient waste recycling methods be developed.
ESH Design and Measurement Methods	**Evaluate and Quantify ESH Impact** Need integrated way to evaluate and quantify ESH impact of process, chemicals, and process equipment, and to make ESH a design parameter in development procedures for new equipment and processes.

Long Term Difficult Challenges

FIVE DIFFICULT CHALLENGES *< 100 NM / BEYOND 2006*	
Chemicals, Materials and Equipment Management	**Chemical Use Information** Rapid introduction of chemicals and materials into new process requires the understanding of process fundamentals in order to reduce ESH impacts
Climate Change Mitigation	**Reduce High GWP Chemicals Emissions** No known alternatives and international regulatory pressure to reduce emissions of GWP chemicals.
Worker Protection	**Equipment Safety** Need ergonomic principles integrated into the processing and wafer moving equipment for both operation and maintenance aspects, and into the overall manufacturing facility.
Resource Conservation	**Reduce Water, Energy, Chemicals And Materials use** Need resource efficient processing and facility support equipment and improved water reclaim and recycling methods. Emphasis on resource sustainability will grow.
ESH Design and Measurement Methods	**Evaluate and Quantify ESH Impact** Need integrated ESH design in development of new equipment and processes.

DEFECT REDUCTION

Key Messages

- **Yield Model**
  - Defect budgets represent a broad set of tools and have been partially validated by a 1999 study of current defects levels among four SEMATECH Member Companies
  - Future technology node requirements extrapolated from median PID value of each process module by considering increase in area and complexity, and shrinking feature size
  - DRAM defect budgets have been comprehended
  - MPU is tending to greater levels of redundancy—will approach a DRAM (ala core versus periphery) based model
  - Need better definition of P-SoC and C-SoC (design blocks, redundancy, chip sizes) in order to estimate yield and D_0’s
- **Defect Detection**
  - no cost-effective solution exists for high aspect ratio inspection
  - need defect standard wafer—polystyrene latex (PSL) not relevant
  - Coordinate accuracy is critical—detected defects MUST appear in SEM FoV for review and classification
- **Systematic Limited Yield**
  - Major yield limiter in 1st year—model is needed for prediction and control of major contributors node to node
  - Advanced process control (feedforward and feedback) is critical to control variability—tools must incorporate control for self-monitoring and self-correcting
- **Integrated Yield Management (IYM)**
  - Rapid identification of yield detracting mechanisms is a must for defect sourcing and yield learning.
  - Circuit complexity and amount of data acquired will continue to grow exponentially—software solutions critical
  - IYM must comprehend integrated circuit design, visible and non-detectable defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms

DRAM Defect Density Assumptions

- **For $Y_{elec} = Y_s * Y_r$**
- **Chip Size = 150 mm^2**
- **Overall Sort Yield (Y_{elec} = 85%)**
- **Systematic Limited Yield (Y_s ~ 90%)**
- **Random Defect Limited Yield (Y_r ~ 94%)**
- **Random Defect Density (D_0 ~ 1300/m^2)**

MPU Defect Density Assumptions

- **For $Y_{elec} = Y_s * Y_r$**
- **Chip Size = 170 mm^2**
- **Overall Sort Yield (Y_{elec} = 75%)**
- **Systematic Limited Yield (Y_s ~ 80%)**
- **Random Defect Limited Yield (Y_r ~ 94%)**
- **Random Defect Density (D_0 ~ 400/m^2)**

Difficult Challenges ≥ 100 nm

- **Yield Models—**Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process induced defects, equipment generated particles and product/process measurements to yield
- **High Aspect Ratio Inspection—**High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/ vias/trenches, and especially defects near/at the bottom of these features.
- **Trace Impurity Specifications—**Test structures and advanced modeling are needed to determine the effect of trace impurities on device performance, reliability and yield**.**
- **Defect Sourcing—**Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test, and work-in-progress (WIP) data must be developed to enable rapid root cause analysis of yield limiting conditions.
- **Nonvisual Defects—**Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.

Difficult Challenges < 100 nm

- **Yield Models—**Defect “budgeting” must comprehend greater parametric sensitivities, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.
- **Defect Detection—**Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughputs.
- **Escalating Inspection Costs—**Equipment must effectively utilize real-time process and contamination control through integrated *in situ* process and product metrology.
- **Defect Characterization—**Defect data must include size, shape, composition, location all independent of “background,” for accelerated yield learning.
- **Defect Free Intelligent Equipment—**Advanced modeling (chemistry/contamination), materials technology, software, and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation.

METROLOGY

The 1999 Metrology Roadmap provides an expanded view into the measurement needs for future technology generations. However, there are several risks associated with the lack of funding for near and longer term metrology development.

- **Near term lack of metrology tools for accelerated technology cycle**
- **Important new approaches need additional funding so that long term R&D meets roadmap timeline (such as electron holography, arrayed atomic force microscopy (AFM) and scanning electron microscopy (SEM)**
- **Basic microscopy required for CD and detection will not be available without accelerated research and development**
- **Traditional metrology methods will not be ready for new materials and processes without more research and development**
- **Gaps in new approaches for statistically limited processes**

The Metrology Roadmap can serve as a guide for focusing future research and development activities and drive funding priorities.

Roadmap Introduction

Advances in metrology are essential to the reduction of feature size and introduction of new materials and processes for future technology generations. Metrology accelerates yield improvement at every stage of manufacturing. It enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The metrology community must accelerate cooperative research, development, and prototyping in order to meet the new roadmap timeline. The feature sizes at the end of the 1999 roadmap will greatly challenge both microscopy and thickness measurements.

Measurement technology combined with computer integrated manufacturing (CIM) and data management systems provides information-based process control. Metrology will slowly migrate from offline to inline and *in situ* to achieve Roadmap goals. In addition, over the next ten years, micro-electromechanical systems (MEMS) are expected to evolve into new types of metrology sensors and test structures. The combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning.

Roadmap Scope

The Metrology chapter topics covered in the 1999 Roadmap are *Microscopy*, *Critical Dimension (CD) and Overlay*, *Film Thickness and Profile*, *Materials and Contamination Analysis*, *Dopant Profile*, *In situ Sensors for Process Control*, *Reference Materials*, and *Correlation of Physical and Electrical Measurements*.

Metrology and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. The measurement precision to tolerance (P/T) ratio for evaluation of automated measurement capability for use in statistical process control relates the measurement variation (precision) of the metrology tool to the specified limits of the process. The determination of measurement tool variations is frequently carried out using reference materials that are not representative of the process of interest. Thus, the measurement tool precision information may not reflect measurement-tool induced variations on product wafers. Therefore, it is possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. There is a need for a metric that describes the resolution capability of metrology tools for use in statistical process control. Since the type of resolution (such as thickness requires spatial resolution, levels of metallics on the surface require resolution of atomic percent differences, etc.) depends on the process, topic-specific metrics may be required. Such a metric for distinguishing process variability from metrology tool variability also needs to receive more emphasis. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio.

Metrology Infrastructure Needs

A healthy industry infrastructure is required if suppliers are to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS are to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers does not occur until several years later. The present infrastructure cannot support this delayed return on investment (ROI). Funding that meets the investment requirements of the supplier community is needed to take new technology from proof-of-concept to prototype systems and finally to volume sales.

Difficult Challenges

Metrology needs by 2005 will be affected by new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect materials will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. The following presents the ten major challenges for metrology.

FIVE DIFFICULT CHALLENGES ≥100 nm / BEFORE 2005	*SUMMARY OF ISSUES*
Factory level and company wide metrology integration for *in situ* and in-line metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during rapid thermal anneal (RTA).
Impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials and reduced edge exclusion for metrology tools	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Detectivity of trace metals in bulk silicon or in the top silicon layer of SOI must be enhanced.
Measurement of the frequency-dependent dielectric constant of low κ interconnect materials at 5x to 10x base frequency.	Equipment, procedures, and test structures need to be reduced to practice and applied to low κ interconnect materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers.

Additional Long Term Challenges

ADDITIONAL DIFFICULT CHALLENGES *< 100 nm / BEYOND 2005*	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for Damascene process may require measurement of trench structures.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	The wearout mechanism for new, high gate and capacitor dielectric materials is unknown.
Statistical limits of sub-70 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
3D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Production worthy, physical inline metrology for transistor processes that provides SPC*** required to achieve consistent electrical properties	Presently, the combined physical metrology for gate dielectric, CD, and dopant dose and profile is not adequate for sub-70 nm design rules.

** FTIR—Fourier transform infrared spectroscopy*
*** SIMS—secondary ion mass spectroscopy*
**** SPC—statistical process control*

Issues

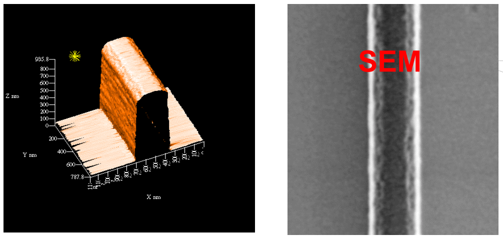
Scanning Electron Microscopy is very limited for sub 100 nm.

Microscopy

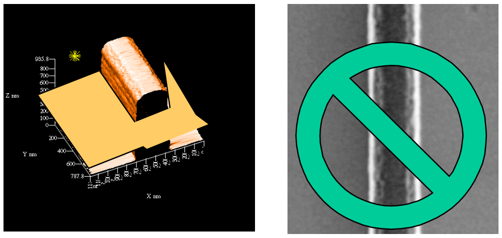
Issues:

CD and Detection require new microscopy

- **SEM with sub 100 nm Roadmap Resolution has poor Depth of Focus**
- **3D Information Required**
- **Improved throughput required**



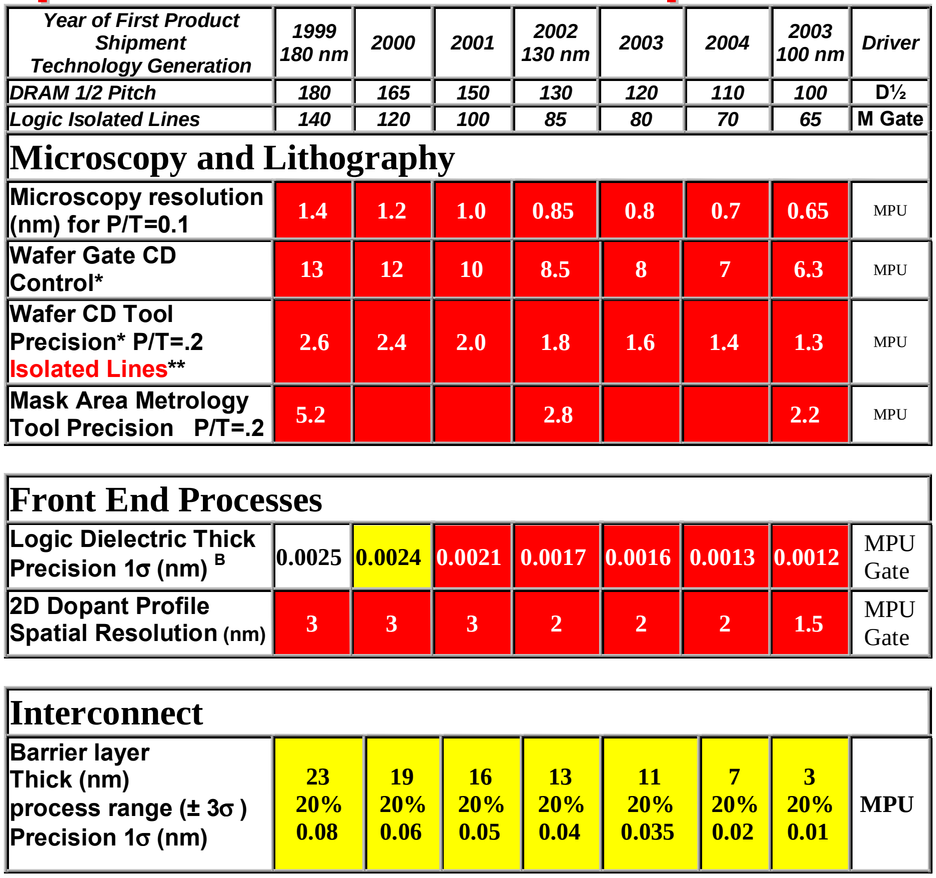
Today : Depth of focus > 1 micron



With Future Resolution:
Depth of focus << 1 micron

Metrology tools will not be able to meet the precision requirements required for process control.

Examples of Precision Requirements



Year of First Product Shipment Technology Generation	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2003 100 nm*	*Driver*
DRAM 1/2 Pitch	*180*	*165*	*150*	*130*	*120*	*110*	*100*	D½
Logic Isolated Lines	*140*	*120*	*100*	*85*	*80*	*70*	*65*	M Gate
Microscopy and Lithography								
Microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	MPU
Wafer Gate CD Control*	13	12	10	8.5	8	7	6.3	MPU
Wafer CD Tool Precision* P/T=.2 Isolated Lines**	2.6	2.4	2.0	1.8	1.6	1.4	1.3	MPU
Mask Area Metrology Tool Precision P/T=.2	5.2			2.8			2.2	MPU
Front End Processes								
Logic Dielectric Thick Precision 1σ (nm) B	0.0025	0.0024	0.0021	0.0017	0.0016	0.0013	0.0012	MPU Gate
2D Dopant Profile Spatial Resolution (nm)	3	3	3	2	2	2	1.5	MPU Gate
Interconnect								
Barrier layer Thick (nm) process range (± 3σ) Precision 1σ (nm)	23 20% 0.08	19 20% 0.06	16 20% 0.05	13 20% 0.04	11 20% 0.035	7 20% 0.02	3 20% 0.01	MPU

Metrology tools are not yet capable of measuring and controlling interfaces that are a key to gate stack and interconnect films.

MODELING AND SIMULATION

Difficult Challenges

For high frequency modeling, comprehending the gate transmission line effect is important.

Near Term Challenges

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (such as from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B); metastable states Implant damage, amorphization, re-crystallization
Unified package/die-level models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Model thin film and etch variation across die/wafer (Equipment/topography)	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Model alternative lithography technologies	Resolution enhancement effects and mask synthesis (such as OPC, PSM) 248 versus 193 versus 157 evaluation and tradeoffs Next-generation lithography system models
Reliability models for circuit design and technology development	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability, SER, ESD, latch-up
Model new interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy, low-κ dielectric materials)

CMP–chemical mechanical planarization

Long Term Difficult Challenges

DIFFICULT CHALLENGES *<100 nm / BEYOND 2005*	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (such as metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Accurate atomic scale models for process integration

Technology Requirements

The Technology Requirements tables are meant to give guidance to the Modeling and Simulation “vendors,” which include commercial tool suppliers, university research groups, and national laboratories. Whereas the main Technical Working Groups are giving requirements for the semiconductor technology itself, the Modeling and Simulation Technology Requirements are giving requirements to “models” or software. To give usable guidance Modeling and Simulation vendors, we have divided the requirements into “capabilities” and “accuracy.”

The “Capabilities” requirements table is meant to describe the technology requirements for modeling and simulation that cannot be easily captured as an accuracy requirement. For example, in making longer range technology decisions, the ability to model the essential features of two competing technology options can be an important contributor to the final decision; the development of the capability to model the key aspects of the two options is what we focus on, as such capabilities for new technologies may not exist.

In contrast, the “Accuracy” requirements table more properly describes the level of simulator accuracy needed for process/circuit design or optimization. This level of accuracy is needed to achieve the overall TCAD cost reduction goals listed in the first row of the table. In this case, we assume the basic capability exists, but we are placing accuracy (or perhaps speed) requirements on the models in order for them to be useful in the design/optimization of the technology. Note that accuracy requirements are specified only for the short term technology requirements; for the long term, investigation of new technologies is the overall priority.

Short Term Technology Requirements: Capabilities

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
EQUIPMENT/TOPOGRAPHY								
Equipment simulation		**Gate stack and interconnect uniformity models**			**Effect of processing conditions on material properties**			
Equipment/feature scale link		**Plasma etch: feature/equipment model**			**Within-die feature variation**			
LITHOGRAPHY								
Lithography		**Evaluate 248 nm versus 193 nm**			**Evaluate 193 nm versus 157 nm**			
Resist models		**193, 157 nm resist models**			**Detailed chemical resist developent model**			
PROCESS TCAD								
Gate Stack: evaluate materials		**Model alternate dielectrics**			**Model metal vs. poly gate**			
Diffusion coefficients		**Kinetics of diffusion and activation**			**Interface interactions with point defects and dopants**			
Stress/extended defects		**Front end stress model**			**Extended defects and disloactions**			
DEVICE MODELING (NUMERICAL)								
Gate stack models		**Gate current tunneling models**			**Full quantum gate stack models**			
Reliability models		**Transistor reliability models (gate oxide)**			**Interconnect reliability models (electromig., stress)**			
Noise/variation		**Dopant fluctuation**			**Noise models**			
CIRCUIT ELEMENT MODELING/ECAD								
New circuit element models		**SOI circuit model**			**Gate tunneling current**			
Interconnect models		**Full-chip RLC**			**On-chip inductance effects**			
System-on-chip		**Unified analog/digital**			**DRAM/Flash/embedded memory models**			
PACKAGE MODELING								
Package models		**Complex interconnect geometries; multiple power & ground planes**			**Thermo-mechanical models**			
Unified package/die models		**Unified package/die circuit models**			**Unified RLC extraction for package/die**			
NUMERICS								
	2D grid generation	**Robust, reliable 3D grid generation**			**Highly efficient optimization algorithms**			

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Short Term Technology Requirements: Accuracy/Speed

YEAR OF INTRODUCTION	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*Driver*
OVERALL COST REDUCTION TARGET (DUE TO TCAD)	**20%**			**25%**			**35%**	
EQUIPMENT/TOPOGRAPHY MODELING								
Etch/dep. cross wafer uniformity (% accuracy of the control spec)	**20%**			**10%**			**10%**	*M*
2D/3D topography accuracy	**36 nm** **(20%)**			**20 nm** **(15%)**			**10 nm** **(10%)**	*M*
LITHOGRAPHY MODELING								
Resist profile prediction accuracy	**27 nm** **(15%)**			**13 nm** **(10%)**			**10 nm** **(10%)**	
OPC model accuracy	**9 nm** **(5%)**			**6.5 nm** **(5%)**			**5 nm** **(5%)**	
PROCESS TCAD								
Vertical and lateral junction depth simulation accuracy	**18 nm** **(10%)**			**13 nm** **(10%)**			**10 nm** **(10%)**	
Total source/drain series resistance (accuracy)	**20%**			**20%**			**20%**	
Long-channel Vt (accuracy)	**3%** **(45-54mV)**			**3%** **(36-45mV)**			**3%** **(27-36mV)**	
DEVICE MODELING (NUMERICAL)								
Accuracy of ft at given ft (% of maximum chip frequency)	**10%**			**10%**			**10%**	
Gate leakage current accuracy (%) (decreases due to increase of Ig/Id)	**100%**			**70%**			**40%**	
Ioff accuracy	**100%**			**70%**			**40%**	
Vt rolloff accuracy (mV)	**25mV**			**20mV**			**20mV**	

Short Term Technology Requirements: Accuracy/Speed (continued)

Circuit Element Modeling/ECAD							
I-V error – compact model (accuracy)	**5%**			**5%**			**5%**
Sub-threshold current – compact model (accuracy)	**95%**			**50%**			**10%**
Intrinsic MOS C-V - compact model (accuracy)	**<5%**			**<5%**			**<5%**
Parasitic C-V – compact model (accuracy)	**5-10%**			**5-10%**			**5-10%**
Gm and r0 @Vt+150mV versus L, Vbs, and T	**3%**			**2%**			**2%**
Circuit delay accuracy (% of maximum chip frequency)	**10%**			**5%**			**5%**
RLC delay accuracy (% of maximum chip frequency)	**10%**			**5%**			**5%**
Package Modeling							
Package delay accuracy (% of off-chip clock frequency)	**1%**			**1%**			**1%**
Stress model accuracy (% of yield stress)	**10%**			**10%**			**10%**
Temperature versus position for chip and package (accuracy)	**5 C**			**5 C**			**5 C**
Numerical Methods							
Speed-up of algorithms for 3-D process/device	**1X**			**2X**			**4X**
Linear solvers (equations/minute)	**150K**			**300K**			**600K**
Parallel speedup	**1X**			**2X**			**4X**
MFLOPS required	**80**			**1000**			**4000**

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Long Term Technology Requirements: Capabilities

YEAR OF INTRODUCTION	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
EQUIPMENT/TOPOGRAPHY				
Equipment simulation	**Ab initio simulation of materials properties**	**Computer engineered materials and process recipes**		
LITHOGRAPHY				
Next generation lithography	**EUV and E-beam system**	**Beyond roadmap lithography models**		
Resist technology	**EUV resists**	**Finite polymer-size effects**	**Non-conventional photo-resist models**	
PROCESS TCAD				
Advanced process models	**Metastable activation (>solid solubility)**	**Alternative materials (such as SiGe)**		
NUMERICAL DEVICE MODELING				
Alternative device models	**2D quantum models for MOS**	**Single electron transistor**	**Quantum effect devices**	
CIRCUIT ELEMENT MODELING/ECAD				
Advanced circuit models	**Quantum effets/non-quasi-static**	**Circuit models for alternative devices**		
PACKAGE MODELING				
NUMERICS				
	Exploit parallel computation	**Efficient atomistic/ quantum methods**	**Multi-scale simulation (atomistic-continuum)**	

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ITRS WEBSITE INFORMATION

Online Conference Materials

Conference materials are also available online at the International Roadmap web site.
A discussion area is setup for feedback for the next few months.

The web site contains other information, such as schedules, and news bulletins regarding the Roadmap. Come visit us.

❖

The internet address is
http://www.itrs.net/roadmap/july99.nsf

Enter the passcode set as follows:

The user name is july meeting
The password is energy

❖

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