International Technology Roadmap for Semiconductors

Defect Reduction
Cross-Cut Technology Working Group

Overview

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Presented at International ITRS Workshop July 8-9, 1999, Santa Clara, CA

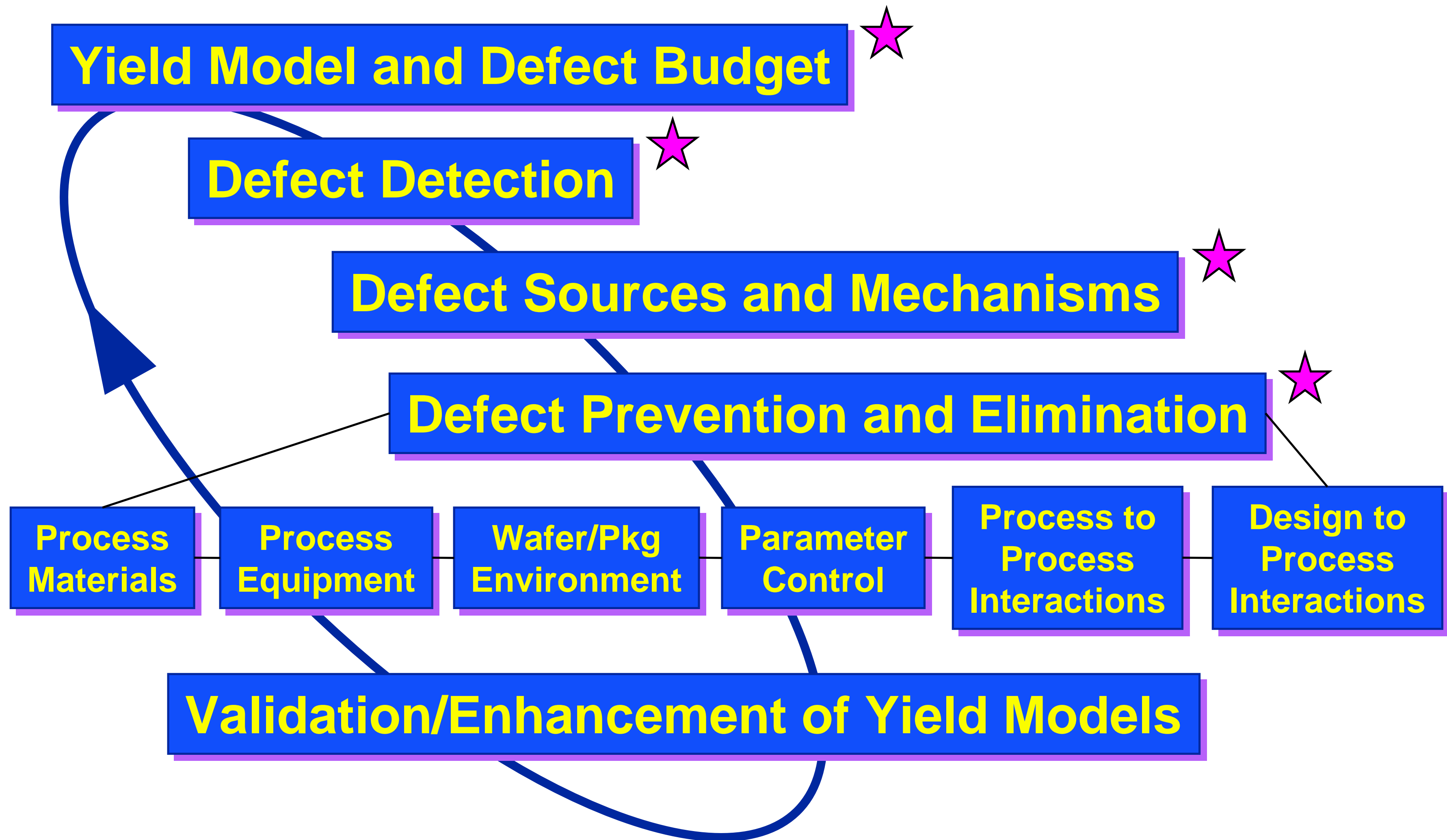
Outline

- Focus Topics
- Yield Cycle
- Key Messages
- Sort Yield and Defect Density Targets
- Difficult Challenges
- Yield Model and Defect Budget
- Defect Detection
- Defect Sources and Mechanisms
- Defect Prevention and Elimination
- Summary

Yield

ITRS

DR CCTWG Yield Learning Cycle



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Yield, Fault Density and Product Cycle

Optimal Range for Statistical Significance

Chip Yield as a Function of Fault Density

Yield (%)

100
90
80
70
60
50
40
30
20
10
0

100 50 20 10 5 2 1 0.5 0.2 0.1 0.05 0.02 0.01 0.005 0.002 0.001

Fault Density (Faults/cm^2)

Ys (A=0.5)
Yp (A=4)

Key Messages

- **Yield Model**
  - Defect budgets represent a broad set of tools and have been partially validated by a 1999 study of current defects levels among 4 SEMATECH Member Companies
  - Future technology node requirements extrapolated from median PID value of each process module by considering increase in area and complexity, and shrinking feature size
  - DRAM defect budgets have been comprehended
  - MPU is tending to greater levels of redundancy - will approach a DRAM (ala core versus periphery) based model
  - Need better definition of P-SoC and C-SoC (design blocks, redundancy, chip sizes) in order to estimate yield and D0's

- **Defect Detection**
  - no cost effective solution exists for high aspect ratio inspection
  - need defect standard wafer - PSL not relevant
  - Coordinate accuracy is critical - detected defects MUST appear in SEM FoV for review and classification

Key Messages

- **Systematic Limited Yield**
  - Major yield limiter in 1st year - model is needed for prediction and control of major contributors node to node
  - Advanced process control (feedforward and feedback) is critical to control variability - tools must incorporate control for self-monitoring and self-correcting
- **Integrated Yield Management**
  - Rapid identification of yield detracting mechanisms is a must for defect sourcing and yield learning.
  - Circuit complexity & amount of data acquired will continue to grow exponentially - software solutions critical
  - IYM must comprehend integrated circuit design, visible & non-detectable defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms

DRAM Defect Density Assumptions

	1999	2000	2001	2002	2003	2004	2005	2008	2011	2014
DRAM Technology Node (nm)	**180**			**130**			**100**	**70**	**50**	**35**
MPU Technology Node (nm)	**140**		**100**			**70**				
Critical Dimensions (nm)										
DRAM 1/2 Pitch	180			130			100	70	50	35
DRAM 1/2 Pitch (modeled)	180	161	145	130	119	107	100	71	50	35
Die Size (mm^2)										
Production (40% + 4 yrs)	132	138	145	152	159	166	174	199	229	262
Yield (@ production phase end)										
Sort	85%	85%	85%	85%	85%	85%	85%	85%	85%	85%
Random Do (killer defects/m^2)	917	816	780	745	712	680	650	567	494	431
Do (@ 90nm)	917	657	505	388	311	239	201	87	38	17
Overall Electrical Do (faults/m^2)	1228	1174	1121	1071	1024	978	934	815	711	620

- **For $Y_{elec} = Y_s * Y_r$**
- **Overall Sort Yield (Y_{elec} = 85%)**
- **Systematic Limited Yield (Y_s ~ 90%)**
- **Random Defect Limited Yield (Y_r ~ 94%)**

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MPU Defect Density Assumptions

- For $Y_{elec} = Y_s{*}Y_r$
- Chip Size = $170mm^2$
- Overall Sort Yield (Y_{elec} = 75%)
- Systematic Limited Yield (Y_s ~ 80%)
- Random Defect Limited Yield (Y_r ~ 94%)
- Random Defect Density (D_0 ~ $400/m^2$)

Defect Reduction Difficult Challenges ≥ 100 nm

- **Yield Models -** Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process induced defects, equipment generated particles and product/process measurements to yield
- **High Aspect Ratio Inspection -** High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/vias/trenches, and especially defects near/at the bottom of these features.
- **Trace Impurity Specifications -** Test structures and advanced modeling are needed to determine the effect of trace impurities on device performance, reliability and yield.
- **Defect Sourcing -** Automated, intelligent analysis and reduction algorithms which correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions.
- **Nonvisual Defects -** Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.

Defect Reduction Difficult Challenges < 100 nm

- **Yield Models -** Defect "budgeting" must comprehend greater parametric sensitivities, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.
- **Defect Detection -** Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughputs.
- **Escalating Inspection Costs -** Equipment must effectively utilize real-time process and contamination control through integrated in-situ process and product metrology.
- **Defect Characterization -** Defect data must include size, shape, composition, location all independent of "background," for accelerated yield learning.
- **Defect Free Intelligent Equipment -** Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation.

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Yield Model and Defect Budget

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Daren Dance
Wright, Williams and Kelly

Presented at US Domestic ITRS Workshop June 2-3, 1999, Austin, TX

Technology Requirements:
Yield Model and Defect Budget

- **Defect budget requirements for the 1999 180nm technology node will use results of a 1999 study of current process-induced defects (PID) at SEMATECH Member Companies.**
  - Based on the negative binomial yield model
  - Microprocessor random electrical fault densities are calculated for 75% yield in yield ramp years 2-4, and a chip area =170mm^2
  - Future technology node requirements extrapolated from median PID value of each process module by considering increase in area, increase in complexity, and shrinking feature size.
- **Key assumption: No new process, material, or tool will be acceptable with a larger PID budget than prior processing methods.**
- **Defect budgeting method tends to be a worst case model since all process steps are assumed to be at minimum device geometry.**
  - Many processes allow process zones with more relaxed geometries. However, manufacturing uses tools at both minimum and relaxed geometries. Thus a worst case defect budgeting model is prudent.

Technology Requirements:
Yield Model and Defect Budget

- **Previous iterations of the NTRS have assumed that Systematic Limited Yield (Y_S) was 100%.**
  - Based on inputs from the chip die size table, microprocessor systematic limited yield (Y_S) is defined to be 80% at the yield ramp phase.
  - Using this and the defined chip area, the microprocessor random defect density (D_0) is calculated.
  - Given the number of mask layers allows for the calculation of allowed random faults per microprocessor mask level.
- **From the faults per mask level, random PID budgets for process zones at various technology nodes are calculated.**
- **PID Numbers will be projected in more detail in generic tool list table.**
- **For the first time, random fault targets specifically for DRAMs are stated.**

Technology Requirements:Yield Model and Defect Budget

Table 56-A Yield Model and Defect Budget MPU Technology Requirements

Short Term Requirements / ***Long Term Requirements***

Year of Introduction *"Technology Node"*	*1999* *180nm*	*2000*	*2001*	*2002* *130nm*	*2003*	*2004*	*2005* *100nm*	*Driver*	*2008* *70nm*	*2011* *50nm*	*2014* *35nm*	*Driver*
MPU												
Critical Defect Size	115	103	92	82	73	65	58		41	29	21	
Random D0 *	382	303	242	192	152	120	96		47	24	12	
Mask Levels	23	23	23	24	24	24	25		27	28	29	
Faults/Mask	17	13	11	8	6	5	4		1.8	0.9	0.4	
Logic Random PID Budget (defects/m2) at Critical Defect Size or Greater ***												
FEOL @												
Doping	164	104	66	40	25	16	9		2.2	0.5	0.1	
Interconnect	200	126	80	48	30	19	12		2.6	0.7	0.2	
Surface Prep	162	102	65	39	24	15	9		2.1	0.5	0.1	
Thermal/Thin Film	147	93	59	36	22	14	8		1.9	0.5	0.1	
BEOL #												
Interconnect	141	89	57	34	21	13	8		1.9	0.5	0.1	
Planarization	132	83	53	32	20	12	8		1.7	0.4	0.1	
Surface Prep	90	57	36	22	14	9	5		1.2	0.3	0.1	
FEOL/BEOL												
Lithography	59	37	23	14	9	6	3		0.8	0.2	0.0	
Metrology/Inspection	54	34	22	13	8	5	3		0.7	0.2	0.0	
Wafer Handling	9	6	4	2	1	1	1		0.12	0.03	0.01	

** Logic Random D0 normalized to 115nm Logic Half Pitch Critical Defect Size at Ramp Phase End*

@ FEOL - front end of line

 # BEOL - back end of line

**** Random PID Budget Numbers are based on 1999 SEMATECH 150nm RDLY Model Project*

1997 Budget Allocation

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Defect Budget Generic Tool List

CMP Clean		Litho Stepper
CMP Insulator		Measure CD
CMP Metal		Measure Film
Coat/Develop/Bake		Measure Overlay
CVD Insulator		Metal CVD
CVD Oxide Mask		Metal Electroplate
Dielectric Track		Metal Etch
Furnace CVD		Metal PVD
Furnace Fast Ramp		Plasma Etch
Furnace Oxide/Anneal		Plasma Strip
Implant High Current		RTP CVD
Implant Low/Med Current		RTP Oxide/Anneal
Inspect PLY		Test
Inspect Visual		Vapor Phase Clean
Litho Cell		Wafer Handling
		Wet Bench

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Tool Requirements: Yield Model and Defect Budget

Table 56-C Yield Model and Defect Budget Tool Technology Requirements

Short Term Requirements									***Long Term Requirements***			
Year of Introduction	*1999*	*2000*	*2001*	*2002*	*2003*	*2004*	*2005*		*2008*	*2011*	*2014*	
"Technology Node"	*180nm*			*130nm*			*100nm*	*Driver*	*70nm*	*50nm*	*35nm*	*Driver*
MPU												
Critical Defect Size	115	103	92	82	73	65	58		41	29	21	
Random D0 *	382	303	242	192	152	120	96		47	24	12	
Mask Levels	23	23	23	24	24	24	25		27	28	29	
Faults/Mask	17	13	11	8	6	5	4		1.8	0.9	0.4	
Logic Random Tool PID Budget (defects/m2) at Critical Defect Size or Greater ***												
CMP Clean	578	364	231	140	87	55	33		2.0	0.5	0.1	
CMP Insulator	832	525	334	201	126	79	48		2.9	0.7	0.2	
CMP Metal	604	381	242	146	92	57	35		2.1	0.5	0.1	
Coat/Develop/Bake	233	147	93	56	35	22	13		0.8	0.2	0.0	
CVD Insulator	1070	675	429	259	162	101	62		3.7	0.9	0.2	
CVD Oxide Mask	993	627	398	240	150	94	57		3.4	0.9	0.2	
Dielectric Track	311	197	125	75	47	30	18		1.1	0.3	0.1	
Furnace CVD	1107	699	444	268	168	105	64		3.8	1.0	0.2	
Furnace Fast Ramp	388	245	156	94	59	37	22		1.3	0.3	0.1	
Furnace Oxide/Anneal	530	334	212	128	80	50	30		1.8	0.5	0.1	
Implant High Current	911	575	365	220	138	86	52		3.1	0.8	0.2	
nplant Low/Med Current	796	502	319	192	121	75	46		2.7	0.7	0.2	
Inspect PLY	327	206	131	79	49	31	19		1.1	0.3	0.1	
Inspect Visual	369	233	148	89	56	35	21		1.3	0.3	0.1	
Litho Cell	360	227	144	87	54	34	21		1.2	0.3	0.1	

1999 Budget Allocation Recalculate

Tool Requirements: Yield Model and Defect Budget cont.

Table 56-C Yield Model and Defect Budget Tool Technology Requirements

Short Term Requirements									*Long Term Requirements*			
Year of Introduction "Technology Node"	*1999 180nm*	*2000*	*2001*	*2002 130nm*	*2003*	*2004*	*2005 100nm*	*Driver*	*2008 70nm*	*2011 50nm*	*2014 35nm*	*Driver*
MPU												
Critical Defect Size	115	103	92	82	73	65	58		41	29	21	
Random D0 *	382	303	242	192	152	120	96		47	24	12	
Mask Levels	23	23	23	24	24	24	25		27	28	29	
Faults/Mask	17	13	11	8	6	5	4		1.8	0.9	0.4	
Logic Random Tool PID Budget (defects/m2) at Critical Defect Size or Greater ***												
Measure CD	358	226	144	87	54	34	21		1.2	0.3	0.1	
Measure Film	398	251	160	96	60	38	23		1.4	0.3	0.1	
Measure Overlay	327	206	131	79	49	31	19		1.1	0.3	0.1	
Metal CVD	520	328	208	126	79	49	30		1.8	0.5	0.1	
Metal Etch	1206	761	483	291	182	114	69		4.1	1.0	0.3	
Metal PVD	773	488	310	187	117	73	44		2.7	0.7	0.2	
Plasma Etch	1138	718	456	275	172	108	65		3.9	1.0	0.2	
Plasma Strip	791	499	317	191	120	75	45		2.7	0.7	0.2	
RTP CVD	337	213	135	81	51	32	19		1.2	0.3	0.1	
RTP Oxide/Anneal	234	148	94	57	35	22	13		0.8	0.2	0.0	
Test	127	80	51	31	19	12	7		0.4	0.1	0.0	
Wafer Handling	50	32	20	12	8	5	3		0.2	0.0	0.0	
Wet Bench	880	555	353	213	133	83	51		3.0	0.8	0.2	

1999 Budget Allocation
Recalculate

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International Technology Roadmap for Semiconductors

Defect Reduction

Cross-Cut Technology Working Group

Defect Detection

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Presented at US Domestic ITRS Workshop June 2-3, 1999, Austin, TX

1999 Technology Requirements Updated Table 57(Draft)

Short Term Years									*Long Term Years*			
Year of Introduction "Technology Node"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER	2005 100 nm	2005 100 nm	2005 100 nm	DRIVER
*Patterned Wafer Inspection, PSL spheres at 90% capture, Equivalent Sensitivity (nm) *See Footnotes A, B*												
Process R&D at 300cm2/hr	54	49	44	39	36	33	30	0.3xDR	21	15	11	0.3xDR
Yield ramp at 3000cm2/hr	72	65	59	52	48	44	40	0.4xDR	28	20	14	0.4xDR
Volume production at 10000cm2/hr	90	81	73	65	60	55	50	0.5xDR	35	25	18	0.5xDR
High Aspect Ratio Feature Inspection: Defects other than residue, Equivalent Sensitivity in PSL diameter(nm)												
at 90% capture rate. See Footnote C for a description of the following numbers												
All stages of manufacturing	54	49	44	39	36	33	30	0.3xDR	21	15	11	0.3xDR
*Unpatterned, PSL spheres at 90% capture, Equivalent Sensitivity (nm) *See Footnotes D, E*												
Metal film	69	63	57	51	47	43	39	0.3xMCP	29	21	14	0.3xMCP
Nonmetal films	54	49	44	39	36	33	30	0.3xDR	21	15	11	0.3xDR
Bare Si	54	49	44	39	36	33	30	0.3xDR	21	15	11	0.3xDR
Wafer backside	200	180	180	130	130	130	100	DR	70	50	35	DR
Defect Review												
Resolution (nm) See Footnote H	9	9	8	7	7	6	5	0.05xDR	4	3	2	0.05xDR
Coordinate accuracy (µm) @ above resolution	3	3	2	2	2	1	1	*	1	1	0.5	*
Automatic Defect Classification on a Defect Review Platform; See Footnotes F, G												
Redetection:Minimum defect size (nm)	72	65	59	52	48	44	40	0.4xDR	28	20	14	0.4xDR
Number of defect types	5	5	5	10	10	10	15	**	20	20	25	**
Speed (sec/defect)	10	10	7	5	5	5	5	***	5	5	5	***
Speed — w/elemental (sec/defect)	25	25	20	15	15	13	10	***	10	10	10	***

DR=Design Rule; MCP=Minimum Contacted Pitch (Table 32)

*** Assume 0.67x1024x1024 pixels at stated resolution**

**** Trend to indicate coarse-fine classification**

*****Defect density from FEOL at Surface Prep (Table 56) 100% inspected 5000 wfr starts per month**

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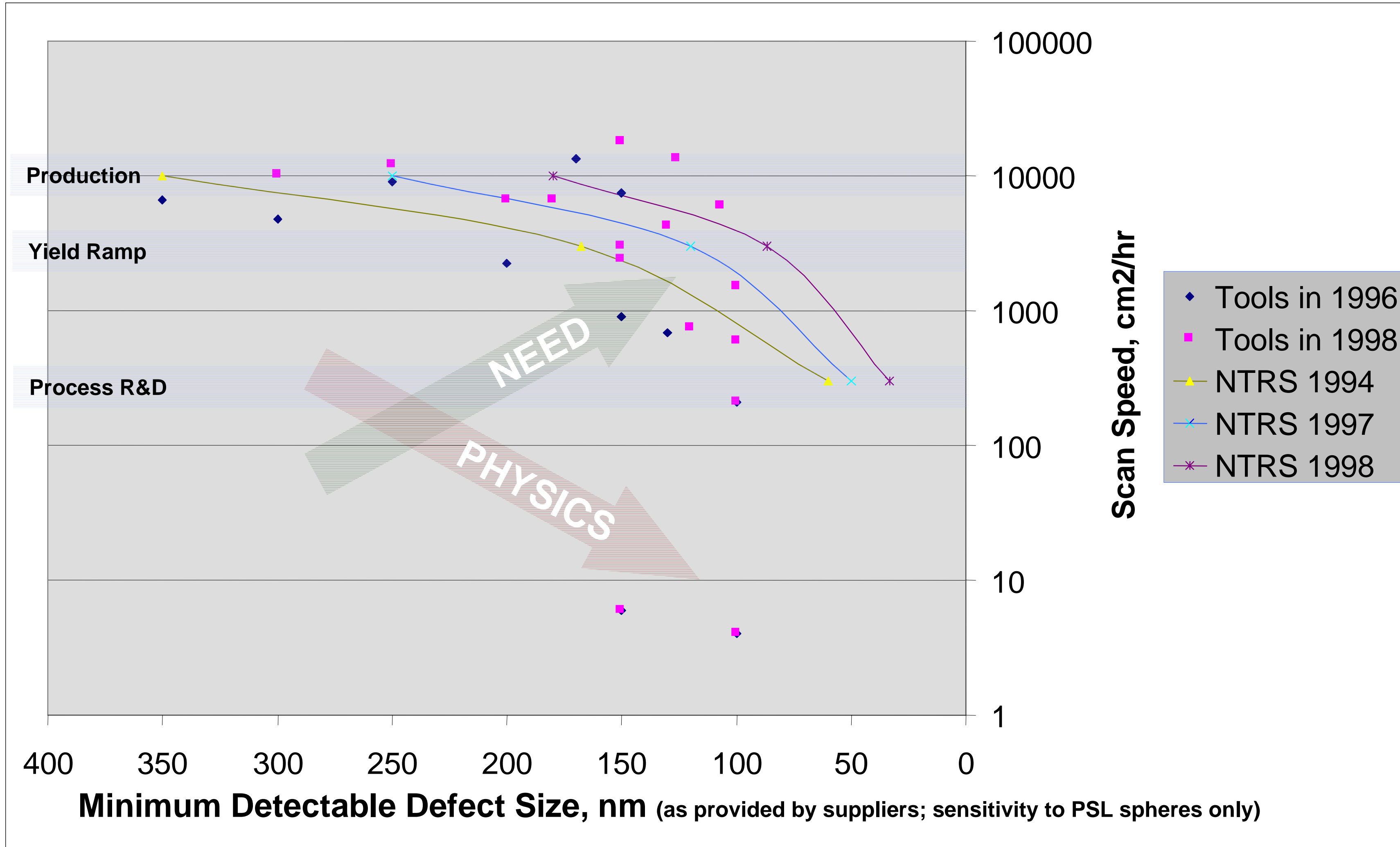
Patterned Wafer Inspection Tools
- Throughput vs. Minimum Detectable Defect Size



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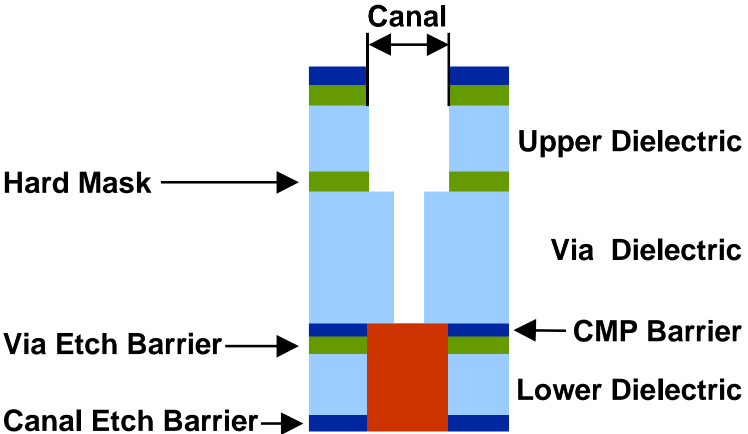
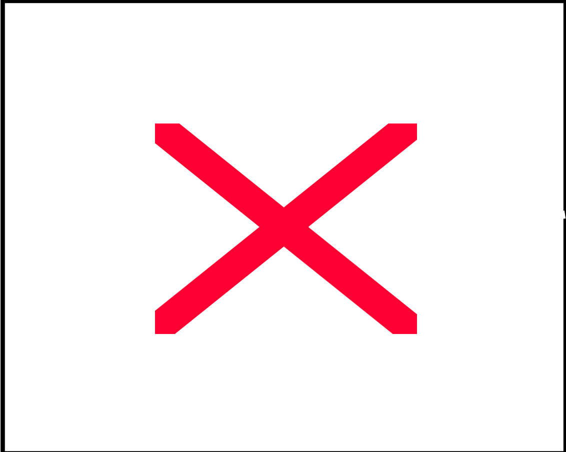
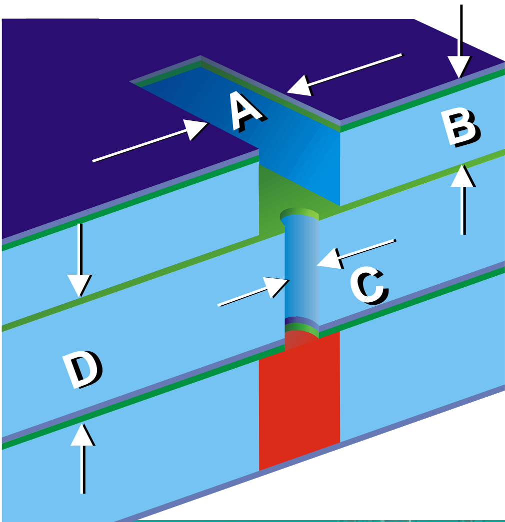
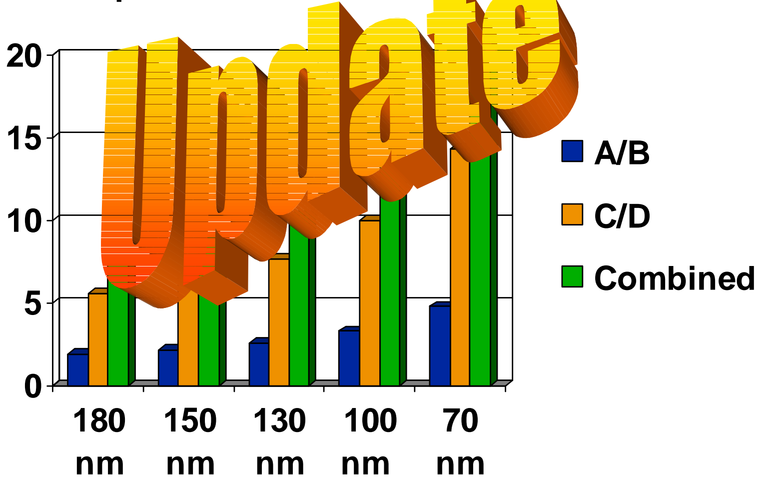
High-Aspect Ratio Inspection (HARI)





Void caused by residue left behind after via etch process step





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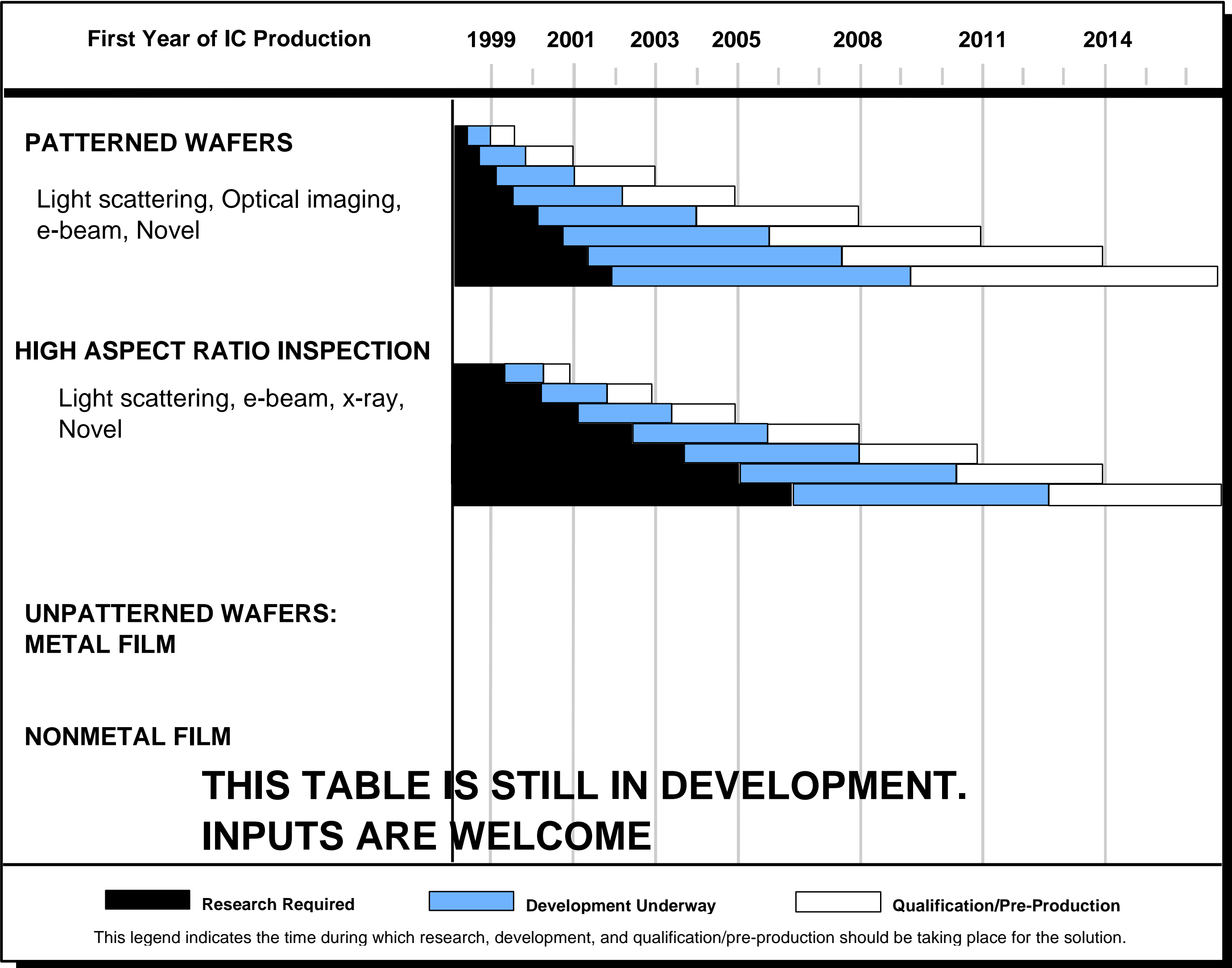
Updated technology requirements

- **Patterned Wafer Scan Speed is required to be at least 300 cm2/hr for Process R&D mode, 3000 cm2/hr for Yield Ramp mode, and at least 10000 cm2/hr for Volume Production mode**
- **HARI defects are already considered "killers" at any process stage. Hence minimum defect sensitivity was stipulated as 0.3 times technology node at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more should also be detected.**
- **Unpatterned Wafer Defect Detection Tools will be required to scan 150 (200 mm or equivalent) wafers per hour at nuisance defect rates lower than 5%**

Potential Solutions



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Defect Sources and Mechanisms

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Presented at US Domestic ITRS Workshop June 2-3, 1999, Austin, TX

Defect Sourcing Complexity

	1999	2002	2005	2008	2011	2014
DRAM Technology Node (nm)	180	130	100	70	50	35
Transistor Density (M/cm^2)						
Logic	7	19	53	150	425	1201
Defect Sourcing Complexity						
No of Processing Steps	380	430	480	530	580	630
Sourcing Complexity (E6)	25	81	255	796	2462	7565
Sourcing Complexity Trend	1.0	3.2	10	32	98	300

Defect Sourcing Complexity (E6)

8000
7000
6000
5000
4000
3000
2000
1000
0

180 130 100 70 50 35

DRAM Technology Node

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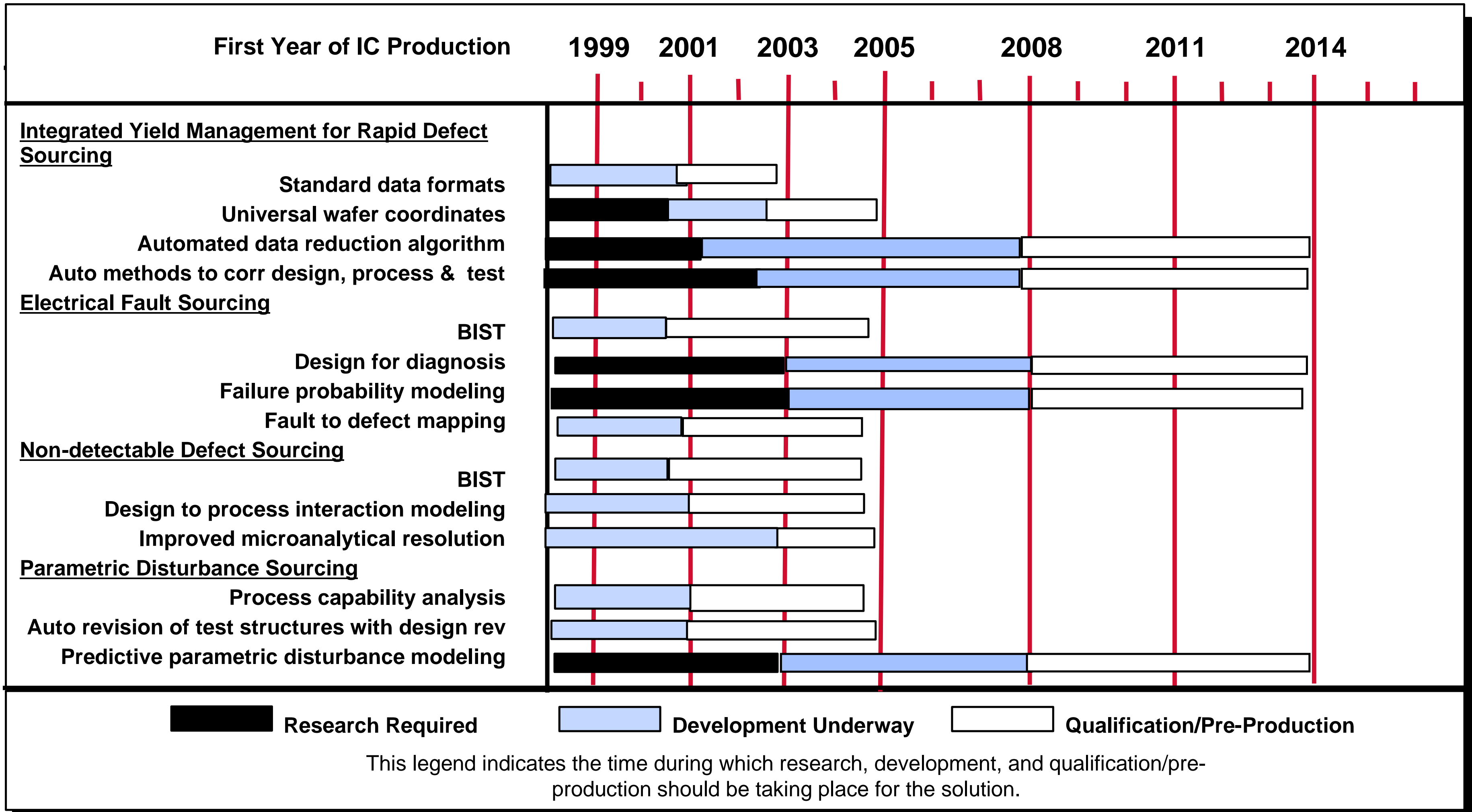
Defect Sourcing Definitions

- Defect sourcing complexity factor = (logic transistor / mm^2)x(# processing steps)
- Defect sourcing complexity trend is normalized to 180nm technology node.
- Defect sourcing means identifying point of occurrence (i.e. identify process tool, design, test or process integration issue causing a visible or non-detectable defect, parametric problem or electrical fault).
- Defect data volume (DV) is the product of wafer size & defect sourcing complexity factor.
- DV trend is normalized to 180nm technology node.

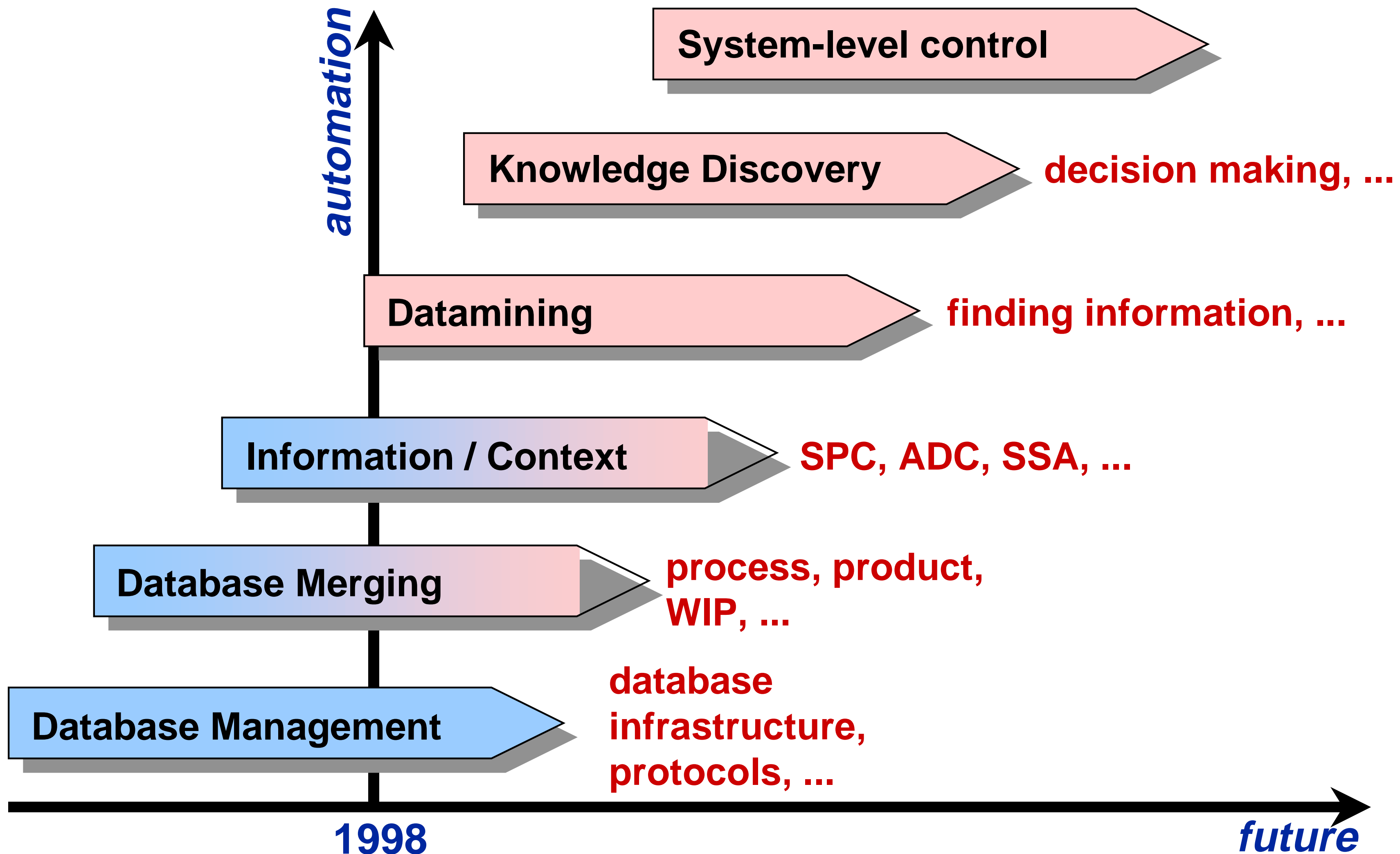
Defect Sourcing Assumptions

- **Keep yield ramp constant at current benchmark level for successive technology nodes despite the increasing complexity and data volumes. This implies a need for increasingly sophisticated integrated yield management (IYM) tools.**
- **Keep time to source yield detractors to <=50% of theoretical cycle time.**
- **New material introduction should not increase defect sourcing time.**
- **Focus defect sourcing on ramp portion of yield learning curve.**
- **Data collection, retention and retrieval will go up exponentially and significant improvement will be required in the IYM tools to enable the above assumptions.**

Potential Solutions
Defect Sources and Mechanisms



Evolution of Automated Yield Management Technologies



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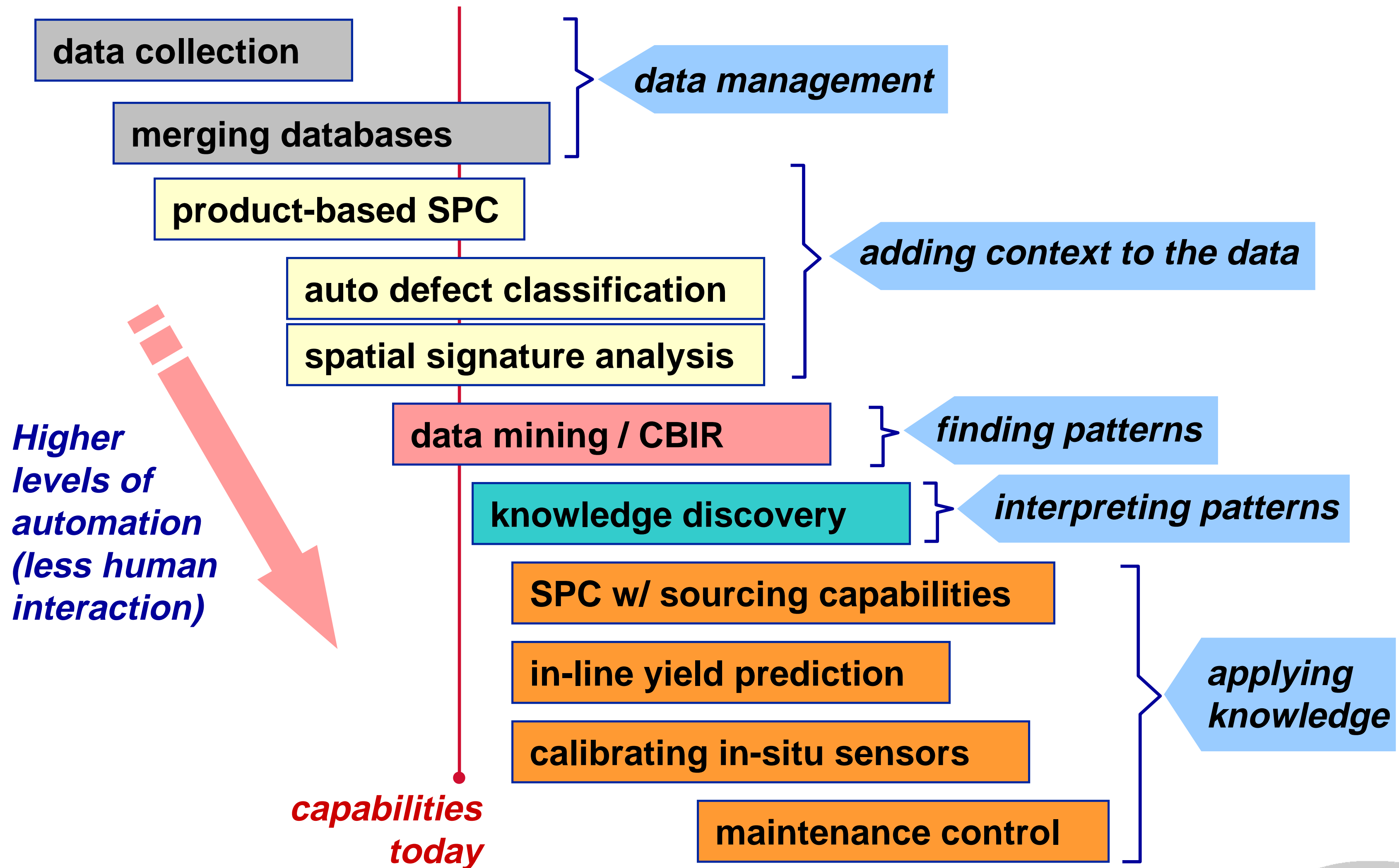
What is the Current Technology Capability of Yield Management Systems ?



Technology Requirements
Defect Sources and Mechanisms

- Rapid identification of yield detracting mechanisms through integrated yield management (IYM) is the essence of defect sourcing and yield learning.
- Software solutions for IYM will be critical for maintaining productivity.
- IYM must comprehend integrated circuit design, visible & non-detectable defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms.
- Visible defect sourcing requirement: Improvement in signal to noise for differentiating real defects from nuisance defects and ability to characterize elemental composition of continuously shrinking visible defects.
- Non-detectable defect sourcing requirement: Tools and methodologies which rapidly isolate electrical failures and partition them into visible defects, non-detectable defects and parametric issues.
- Parametric defect sourcing requirement: Tools are needed which help assess the impact of parametric disturbance on systematic component of the integrated circuit yield.

International Technology Roadmap for Semiconductors

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Defect Prevention and Elimination

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Presented at US Domestic ITRS Workshop June 2-3, 1999, Austin, TX

Table 59: Definitions and Footnotes

- **Critical particle size is based on 1/2 design rule. All defect densities are ‘normalized’ to critical particle size. Critical particle size does not necessarily mean ‘killer.’**
- **The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination . In general molecular weights <250 are not considered detrimental due to the higher volatility of these compounds.**
- **Particle targets apply at POU, not incoming chemical.**
- **Dopants Include P, B, As, Sb**
- **Critical metals and ions include: Ca, Co, Cu, Cr, Fe, Mo, Mn, Na, Ni, W**

Table 59: Defect Prevention Update

Table 59 Defect Prevention and Elimination Technology Requirements *Update: 7/6/99*

Year of First Product Shipment Technology Generation	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	*2008 70 nm*	*2011 50 nm*	*2014 35nm*
Wafer Environment Control										
Critical particle size (nm) (A)	**90**	**75**	**70**	**65**	**60**	**55**	**50**	**35**	**25**	**18**
Particles ³ crit size (/m3) (B)	**12**	**8**	**6**	**5**	**4**	**3**	**2**	**1**	**1**	**1**
Airborne Molecular Contaminants (pptM) (C)										
Litho—Bases (as amine, amide, or NH3)	**1000**	**1000**	**1000**	**750**	**750**	**750**	**750**	**<750**	**<750**	**<750**
Gate—Metals (as Cu, E=2 x 10–5) (C)	**0.3**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	**0.1**	**0.07**	**<0.07**	**<0.07**
Gate—Organics (as MW greater than or equal to 250, E=1 x 10–3) (D)	**200**	**200**	**200**	**100**	**100**	**100**	**70**	**70**	**50**	**<50**
--- Organics(as - CH2-)	**3600**	**3000**	**2000**	**1800**	**1500**	**1300**	**1260**	**1260**	**900**	**<900**
Sal/Cont—Acids (as Cl–, E=1 x 10–5)	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
Sal/Cont—Bases (as NH3, E=1 x 10–6)	**40**	**30**	**25**	**20**	**20**	**15**	**10**	**4**	**<4**	**<4**
Dopants (P or B) (F)	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**

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Table 59: Defect Prevention Update

Table 59 Defect Prevention and Elimination Technology Requirements *Update: 7/6/99*

Year of First Product Shipment Technology Generation	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	*2008 70 nm*	*2011 50 nm*	*2014 35nm*
Process Critical Materials										
Critical Particle Size (nm) (B)	**90**	**75**	**70**	**65**	**60**	**55**	**50**	**35**	**25**	**18**
Ultrapure Water										
Total oxidizable carbon (ppb)	**2**	**1**	**1**	**1**	**1**	**1**	**<1**	**<1**	**<1**	**<1**
Bacteria (CFU/ liter)	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**< 1**	**<1**
Total Silica (ppb)	**0.05**	**0.05**	**0.05**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**	**0.01**
Dissolved oxygen (ppb)	**10**	**1-10**	**1-10**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Particles ³ critical size (/ml)	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.2**	**< 0.2**	**<0.2**
Critical cation, anion, metals (ppt, each)	**< 20**	**< 15**	**< 15**	**< 10**	**< 8**	**< 6**	**< 5**	**< 1**	**< 1**	**<1**
Liquid Chemicals (E)										
Particles ³ crit size (/ml)	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**< 0.5**	**<0.5**
HF-, H2O2, NH4OH: Fe, Cu (ppt, each)	**< 250**	**< 200**	**< 180**	**< 150**	**< 130**	**< 110**	**< 100**	**< 50**	**< 50**	**<50**
Critical cation, anion, metals (ppt, each)	**< 20**	**< 15**	**<12**	**< 10**	**< 8**	**< 6**	**< 5**	**< 1**	**< 1**	**<1**
Note: Delete category of "Other Metals" consistent with Surface Preparation										
HF-only TOC* (ppb)	**< 60**	**< 40**	**< 35**	**< 30**	**<27**	**<24**	**< 20**	**< 15**	**< 10**	**<10**
HCl, H2SO4: All impurities (ppt)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**<1000**
BEOL Solvents, Strippers K, Li, Na (ppt, each)	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**< 1000**	**<1000**

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Table 59: Defect Prevention Update

Table 59 Defect Prevention and Elimination Technology Requirements *Update: 7/6/99*

Year of First Product Shipment Technology Generation	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	*2008 70 nm*	*2011 50 nm*	*2014 35nm*
Process Critical Materials										
Bulk Ambient Gases										
N2,O2,Ar,H2: H2O,O2,CO2,CH4 (ppt,each)	**100-1000**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**<100**
Particles > critical size (liter)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**<0.1**
Specialty Gases										
POU Particles ³ crit size (/liter) (D)	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Corrosives—metal etchants										
O2 (ppbv)	**100-500**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**<100**	**<100**	**<100**	**<100**
H2O (ppbv)	**< 500**	**< 500**	**< 500**	**100-500**	**100-500**	**100-500**	**<100**	**<100**	**<100**	**<100**
Inerts—Oxide/PR Etchants/Strippers										
O2 (ppbv)	**< 1000**	**500-1000**	**500-1000**	**500-1000**	**500-1000**	**500-1000**	**< 500**	**100-500**	**< 100**	**<100**
H2O (ppbv)	**500-1000**	**< 500**	**< 500**	**< 500**	**< 500**	**100-500**	**100-500**	**< 100**	**< 100**	**<100**
SiHx(Cly)										
Total metallics (pptwt)	**100-500**	**< 100**	**< 100**	**< 100**	**< 100**	**< 100**	**50-100**	**< 50**	**< 50**	**<50**

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Defect Reduction Summary

- **Systematic component of yield is major yield limiter during yield ramp - must be focus of yield related research and development**
  - The ability to rapidly optimize process parameters and prevent excursions through integrated and automatic process control is essential for achieving and maintaining high yields
- **Equipment defect budget is key to minimizing yield excursions in high volume production**
- **High-speed inspection tools which detect defects associated with high aspect ratio features do not currently exist - high aspect ratio inspection will be critical to yield ramp and process control in dual damascene processing**
- **Capture rate of most defect detection tools at high throughput falls off rapidly as we approach the 130nm node - significant investment will be required to bridge this gap**
- **Advancement of tools and techniques are critical to achieving integrated yield management - (i.e. accelerated yield learning)**

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