1999 Assembly & Packaging Roadmap

CHAIR, DTWG & ITWG: Bob Werner, SEMATECH

DTWG MEMBERSHIP

Jim Hayward, AMD
Bill Bottoms, Consultant
Rao Tummala, Ga. Tech.
Jack Fisher, ITRI
Ed Fulcher, LSI
Bob Pfahl, Motorola
Larry Marcanti, Nortel
Chi Shih Chang, SEMATECH
Peter Elenius, Flip Chip Technologies
Ron Bracken, SRC (Co-Chair)
Peter Krusius, Cornell
Dan Radack, DARPA
Ken Brown, Intel
Scott Kulicke, K&S
Dave Munro, Lucent
George Harman, NIST
Paul Dressendorfer, Sandia
John Prince, Univ. of Az.
Mark Bird, Amkor Technology

ITWG MEMBERSHIP

EUROPE

Co van Veen, Philips
Max-Gerhard Seitz, Infineon
Jean-Pierre Moscicki, STMicroelectronics

TAIWAN

Hsiang-Wei Wu, First Int’l. Computer
Enboa Wu, ERSO/ITRI

KOREA

Mark Bird, ANAM Semiconductor, Inc.

JAPAN

Hisao Kasuga, NEC
Henry Utsunomiya, MITI Consultant

U.S.

Chi Shih Chang, SEMATECH
Bob Werner, SEMATECH

1999 Overview

UPDATED

- Market sectors aligned with NEMI
- Expanded discussion on wafer level packaging
- Expanded reliability section
- Thermal management
- High density substrates
- RF and mixed signal packaging
- Multi-chip packaging/modules

ADDED

- System on chip (SOC) & System in a Package (SiP)
- Electro-migration limits of eutectic flip chip bumps

Challenges (Table 42)

- Major categories maintained
- Additions
  - Packaging of Cu/low κ IC
  - Thermal
  - Design for high density digital/mixed signal packaging
  - Manufacturability/reliability of large body packages

Requirements (Table 43)

- Cost
  - Widespread use of PBGA creates cost pressure on QFP & CBGA
  - 20-30% reduction
- Chip size
  - High performance, Cost performance, and Memory reduced substantially
- Increased chip to board frequency
  - Realization of PC133 BUS
- Moderate change to pin count
- Removed pad count
  - Large power/ground connections available with area array
- Overall package profile replaces package thickness

Table 43A. Technology Requirements

Year of First Product Shipment Technology Generation	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*
Cost (Cents/Pin)							
Low cost	🟨 **0.40–0.90**	🟨 **0.38–0.86**	🟨 **0.36–0.81**	🟨 **0.34–0.77**	🟨 **0.33–0.73**	🟨 **0.31–0.70**	🟥 **0.29–0.66**
Hand-held	**0.50–1.30**	**0.48–1.24**	🟨 **0.45–1.17**	🟨 **0.43–1.11**	🟨 **0.41–1.06**	🟨 **0.39–1.01**	🟨 **0.37–0.96**
Cost-performance	**0.90–1.90**	**0.86–1.81**	🟨 **0.81–1.71**	🟨 **0.77–1.63**	🟨 **0.73–1.55**	🟨 **0.70–1.47**	🟥 **0.66–1.40**
High-performance	**3.10**	**2.95**	🟨 **2.80**	🟨 **2.66**	🟨 **2.52**	🟨 **2.40**	🟥 **2.28**
Harsh	**0.50–1.00**	**0.48–0.95**	**0.45–0.90**	🟨 **0.43–0.86**	🟨 **0.41–0.81**	🟨 **0.39–0.77**	🟨 **0.37–0.74**
Memory	**0.40–1.90**	**0.38–1.71**	🟨 **0.36–1.54**	🟨 **0.34–1.39**	🟨 **0.33–1.25**	🟨 **0.31–1.12**	🟥 **0.29–1.01**
Chip Size (mm2)							
Low cost	**53**			**59**			**65**
Hand-held	**53**			**59**			**65**
Cost-performance	**170**			**170**			**170**
High-performance	**340**			**340**			**340**
Harsh	**53**			**59**			**65**
Memory	**80**			**80**			**80**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43A (con’t.)

Year of First Product Shipment Technology Generation	***1999 180 nm***	***2000***	***2001***	***2002 130 nm***	***2003***	***2004***	***2005 100 nm***
Power: Single-Chip Package (Watts)							
Low cost	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Hand-held	1.4		1.7	2.0			2.4
Cost-performance	48		61	75			96
High-performance	88		108	129			160
Harsh	14		14	14			14
Memory	0.8			1.5			2
Core Voltage (Volts)							
Low cost	1.8	1.8	1.8	1.5	1.5	1.2	1.2
Hand-held	1.5-1.8	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2
Cost-performance	1.8	1.8	1.8	1.5	1.5	1.2	1.2
High-performance	1.8	1.8	1.8	1.5	1.5	1.2	1.2
Harsh	5.0	3.3	3.3	2.5	2.5	2.5	2.5
Memory	1.8	1.8	1.8	1.5	1.5	1.2	1.2

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43A (con’t.)

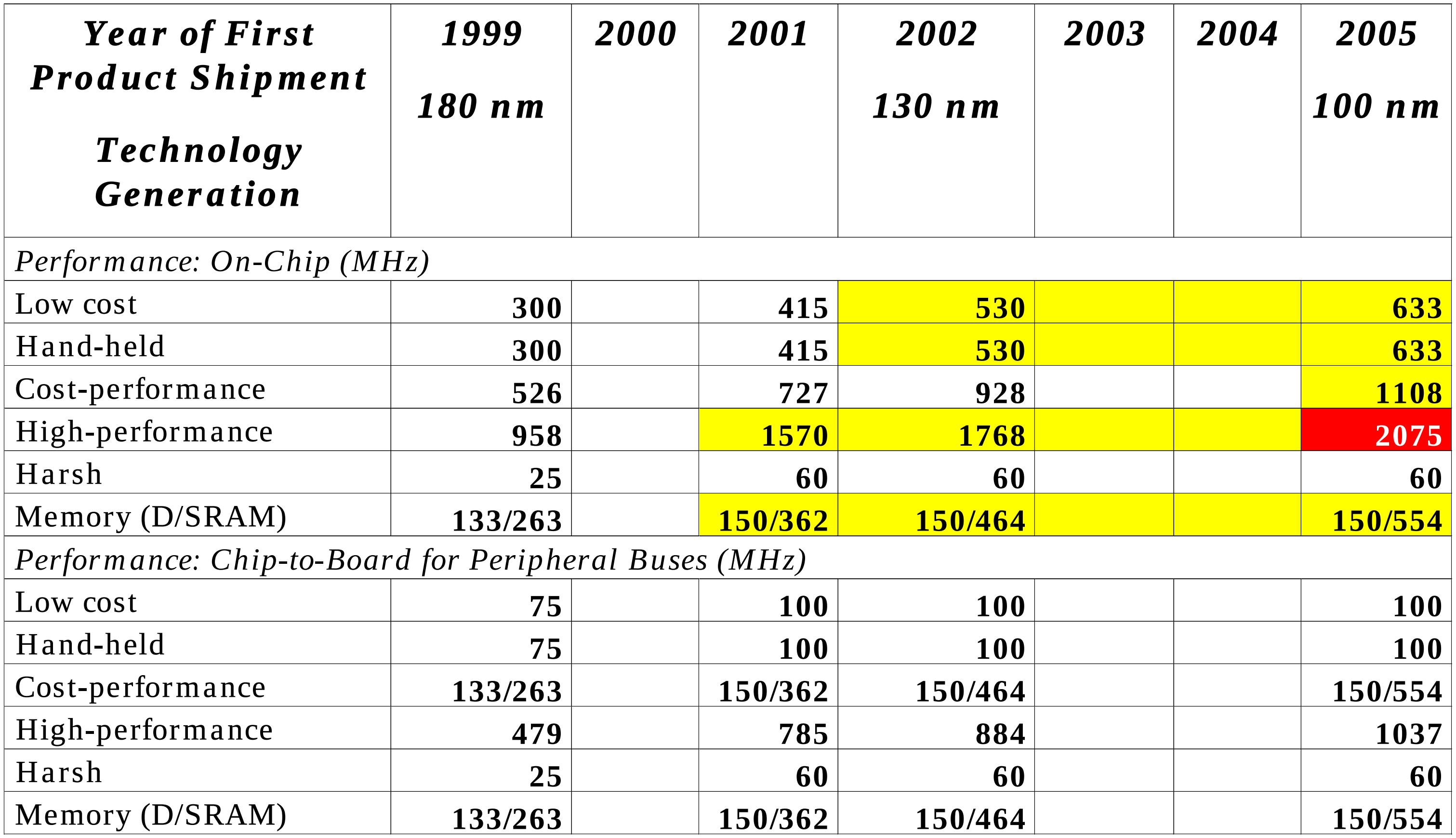
Year of First Product Shipment Technology Generation	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Package Pin Count							
Low cost	**80–290**	**86–313**	**90–338**	**101–365**	**109–395**	**118–426**	**127–460**
Hand-held	**128–368**	**138–397**	**149–429**	**161–464**	**174–501**	**188–541**	**203–584**
Cost-performance *	**370-740**	**400–821**	**432–912**	**466–1012**	**503–1123**	**544–1247**	**587–1384**
High-performance **	**1600**	**1792**	**2007**	**2248**	**2518**	**2820**	**3158**
Harsh	**40–240**	**40–259**	**40–280**	**40–302**	**40–327**	**40–353**	**40–381**
Memory	**44–128**	**44–128**	**44–128**	**44–144**	**44–144**	**48–160**	**48–160**
Overall Package Profile (mm)							
Low cost	**1.7**	**1.7**	**1.2**	**1.2**	**1.2**	**1.0**	**1.0**
Hand-held	**1.2**	**1.2**	**1.0**	**1.0**	**1.0**	**0.8**	**0.8**
Cost-performance	**1.2 – 1.7**	**1.2-1.7**	**1.0 – 1.2**	**1.0 – 1.2**	**1.0 – 1.2**	**0.8 –1.0**	**0.8 –1.0**
High-performance	**n/a**	**n/a**	**n/a**	**n/a**	**n/a**	**n/a**	**n/a**
Harsh	**1.4**	**1.4**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Memory	**1.2**	**1.2**	**1.0**	**1.0**	**1.0**	**0.8**	**0.8**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

* *Red – To meet package profile -> smaller ball -> coplanarity problem*

** *.65mm ball pitch*

Table 43A (con’t.)



Year of First Product Shipment	*1999*	*2000*	*2001*	*2002*	*2003*	*2004*	*2005*
Technology Generation	*180 nm*			*130 nm*			*100 nm*
Performance: On-Chip (MHz)							
Low cost	**300**		**415**	**530**			**633**
Hand-held	**300**		**415**	**530**			**633**
Cost-performance	**526**		**727**	**928**			**1108**
High-performance	**958**		**1570**	**1768**			**2075**
Harsh	**25**		**60**	**60**			**60**
Memory (D/SRAM)	**133/263**		**150/362**	**150/464**			**150/554**
Performance: Chip-to-Board for Peripheral Buses (MHz)							
Low cost	**75**		**100**	**100**			**100**
Hand-held	**75**		**100**	**100**			**100**
Cost-performance	**133/263**		**150/362**	**150/464**			**150/554**
High-performance	**479**		**785**	**884**			**1037**
Harsh	**25**		**60**	**60**			**60**
Memory (D/SRAM)	**133/263**		**150/362**	**150/464**			**150/554**

Solutions Exist	☐	*Solutions Being Pursued*	🟨	*No Known Solutions*	🟥

Table 43A (con't.)

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Junction Temperature Maximum (◦C)							
Low cost	**125**		**125**	**125**	**125**	**125**	**125**
Hand-held	**115**		**115**	**115**	**115**	**115**	**115**
Cost-performance	**100**		**90**	**85**	**85**	**85**	**85**
High-performance	**100**		**90**	**85**	**85**	**85**	**85**
Harsh	**155**		**155**	**155**	**155**	**155**	**175**
Memory	**100**		**100**	**100**	**100**	**100**	**100**
Operating Temperature Extreme: Ambient (◦C)							
Low cost	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Hand-held	**55**	**55**	**55**	**55**	**55**	**55**	**55**
Cost-performance	**45**	**45**	**45**	**45**	**45**	**45**	**45**
High-performance	**45**	**45**	**45**	**45**	**45**	**45**	**45**
Harsh	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 150**	**-40 to 170**
Memory	**55**	**55**	**55**	**55**	**55**	**55**	**55**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43B. Technology Requirements

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Cost (Cents/Pin)			
Low cost	**0.25–0.57**	**0.22–0.49**	**0.19–0.42**
Hand-held	**0.32–0.82**	**0.27–0.70**	**0.23–0.60**
Cost-performance	**0.57–0.74**	**0.49–0.54**	**0.42–0.88**
High-performance	**1.95**	**1.68**	**1.44**
Harsh	**0.32–0.63**	**0.27–0.54**	**0.23–0.46**
Memory	**0.25–0.74**	**0.22–0.54**	**0.19–0.39**
Chip Size (mm^2)			
Low cost	**59**	**65**	**70**
Hand-held	**59**	**65**	**70**
Cost-performance	**170**	**170**	**170**
High-performance	**340**	**340**	**340**
Harsh	**59**	**65**	**70**
Memory	**80**	**80**	**80**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43B (con't.)

Year of First Product Shipment Technology Generation	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Power: Single-Chip Package (Watts)			
Low cost	**n/a**	**n/a**	**n/a**
Hand-held	**2.0**	**2.2**	**2.4**
Cost-performance	**104**	**109**	**???**
High-performance	**170**	**174**	**???**
Harsh	**14**	**14**	**14**
Memory	**2.5**	**3.0**	**3.5**
Core Voltage (Volts)			
Low cost	**0.9**	**0.6**	**0.5-0.6**
Hand-held	**0.6-0.9**	**0.5-0.6**	**0.3-0.6**
Cost-performance	**0.9**	**0.6**	**0.5-0.6**
High-performance	**0.9**	**0.6**	**0.5-0.6**
Harsh	**2.5**	**2.5**	**2.5**
Memory	**0.9**	**0.6-0.9**	**0.5-0.6**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43B (con’t.)

Year of First Product Shipment Technology Generation	***2008 70 nm***	***2011 50 nm***	***2014 35 nm***
Package Pin Count			
Low cost	**160–580**	**201–730**	**254–920**
Hand-held	**256–736**	**322–027**	**406–1167**
Cost-performance	**740–1893**	**932–2589**	**1174–3541**
High-performance	**4437**	**6234**	**8758**
Harsh	**40–480**	**40–604**	**40–761**
Memory	**48–182**	**48–200**	**48–220**
Overall Package Profile (mm)			
Low cost	**1.0**	**1.0**	**1.0**
Hand-held	**0.65**	**0.65**	**0.5**
Cost-performance	**0.65 – 0.8**	**0.65 – 0.8**	**0.5 – 0.65**
High-performance	**n/a**	**n/a**	**n/a**
Harsh	**1.0**	**1.0**	**1.0**
Memory	**0.65**	**0.65**	**0.5**

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43B (con't.)

Year of First Product Shipment Technology Generation	***2008 70 nm***	***2011 50 nm***	***2014 35 nm***
Performance: On-Chip (MHz)			
Low cost	840	1044	???
Hand-held	840	1044	???
Cost-performance	1468	1826	???
High-performance	2574	3081	???
Harsh	100	100	100
Memory (D/SRAM)	175/734	200/913	225/???
Performance: Chip-to-Board for Peripheral Buses (MHz)			
Low cost	125	125	150
Hand-held	125	125	150
Cost-performance	175/734	200/913	225/???
High-performance	1287	1540	???
Harsh	100	100	125
Memory (D/SRAM)	175/734	200/913	225/???

Solutions Exist ☐ *Solutions Being Pursued* 🟨 *No Known Solutions* 🟥

Table 43B (con’t.)

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Junction Temperature Maximum (∘C)			
Low cost	**125**	**125**	**125**
Hand-held	**115**	**115**	**115**
Cost-performance	**85**	**85**	**85**
High-performance	**85**	**85**	**85**
Harsh	**185**	**185**	**185**
Memory	**100**	**100**	**100**
Operating Temperature Maximum: Ambient (∘C)			
Low cost	**55**	**55**	**55**
Hand-held	**55**	**55**	**55**
Cost-performance	**45**	**45**	**45**
High-performance	**45**	**45**	**45**
Harsh	**-40 to 180**	**-40 to 180**	**-40 to 180**
Memory	**55**	**55**	**55**

Solutions Exist	⬜	*Solutions Being Pursued*	🟨	*No Known Solutions*	🟥

Table 44. Current Limits of 63Sn/37Pb Flip Chip Solder Bumps

		Current Limits for 100,000 hr MTTF at Average Bump Temperatures of		
Bump Pitch	Passivation Opening	100°C	90°C	80°C
250 μm	85 μm	75 mA	110 mA	165 mA
200 μm	80 μm	66 mA	97 mA	145 mA
150 μm	65 μm	45 mA	65 mA	95 mA

Table 45A. Chip-to-Next Level Interconnect Needs - Short Term

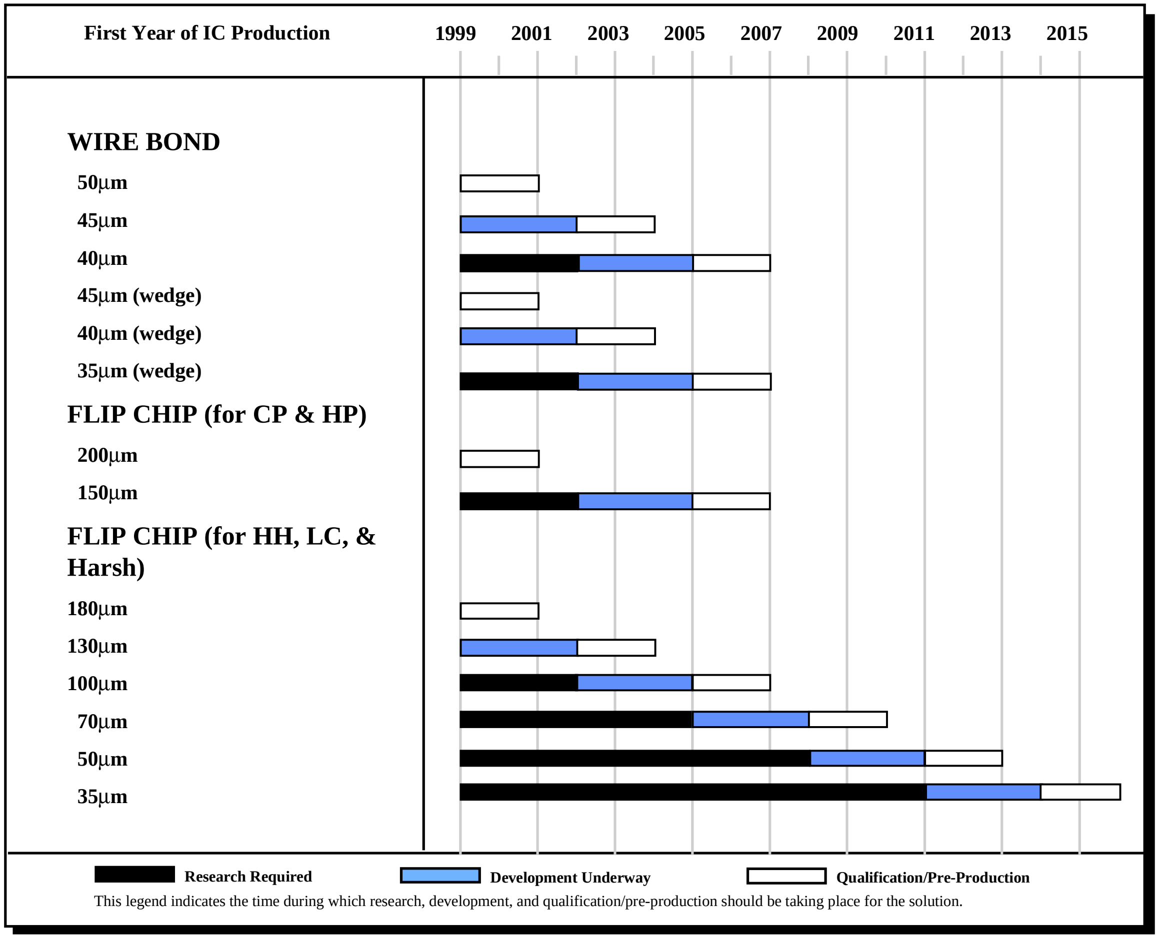
Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Chip Interconnect Pitch (µm)							
Wire bond—ball	**50**	**49**	**47**	**45**	**42**	**41**	**40**
Wire bond—wedge	**45**	**44**	**42**	**40**	**37**	**36**	**35**
TAB*	**50**	**50**	**40**	**40**	**40**	**40**	**30**
Flip chip (area array) **for C/P & H/P**	**200**	**200**	**200**	**200**	**200**	**200**	**150**
Flip chip for HH, LC & Harsh	**180**	**165**	**150**	**130**	**120**	**110**	**100**

Table 45A. Chip-to-Next Level Interconnect Needs - Long Term

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Chip Interconnect Pitch (µm)			
Wire bond—ball	**40**	**40**	**40**
Wire bond—wedge	**35**	**35**	**35**
TAB*	**30**	**30**	**30**
Flip chip (area array) **for C/P & H/P**	**150**	**150**	**150**
Flip chip for HH, LC & Harsh	**70**	**50**	**35**

**TAB— tape automated bonding*

Figure 36. Chip-to-Next Level Interconnect Potential Solutions



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Table 46A. Single Chip Packages Ball Grid Array Packages - Short Term

Year of First Product Shipment	*1999*	*2000*	*2001*	*2002*	*2003*	*2004*	*2005*
Technology Generation	*180 nm*			*130 nm*			*100 nm*
BGA ***solder ball*** *Pitch (mm)*							
Low cost	**1.27**	**1.27**	**1.27**	**1.27**	**1.00**	**1.00**	**1.00**
Hand-held	**1.27**	**1.27**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**
Cost-performance	**1.27**	**1.27**	**1.00**	**1.00**	**1.00**	**1.00**	**1.00**
High-performance	**1.00**	**0.80**	**0.80**	**0.80**	**0.80**	**0.80**	**0.65**
Harsh	**1.27**	**1.27**	**1.27**	**1.27**	**1.00**	**1.00**	**1.00**
BGA Possible Pin Count							
Low cost	**312**	**312**	**392**	**392**	**420**	**512**	**512**
Hand-held	**392**	**420**	**512**	**512**	**512**	**576**	**684**
Cost-performance	**840**	**840**	**1012**	**1012**	**1200**	**1352**	**1568**
High-performance	**1680**	**1860**	**2112**	**2380**	**2664**	**2964**	**3280**
Harsh	**312**	**312**	**392**	**392**	**420**	**512**	**512**

A = integer (BGA size/pitch); R = integer (A/3); pincount = (A–R) × R × 4; body sizes rounded to nearest JEDEC size

Table 46B. Single Chip Packages
Ball Grid Array Packages - Long Term

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
BGA ***solder ball*** *Pitch (mm)*			
Low cost	**1.0**	**0.8**	**0.8**
Hand-held	**0.8**	**0.8**	**0.65**
Cost-performance	**0.8**	**0.8**	**0.65**
High-performance	**0.65**	**0.5**	**0.5**
Harsh	**1.0**	**0.8**	**0.8**
BGA Possible Pin Count			
Low cost	**684**	**800**	**968**
Hand-held	**800**	**968**	**1200**
Cost-performance	**2112**	**2664**	**3612**
High-performance	**3612**	**6844**	**8448 ***
Harsh	**684**	**800**	**968**

A = integer (BGA size/pitch); R = integer (A/3); pincount = (A–R) × *R* × *4; body sizes rounded to nearest JEDEC size*

** This is the I/O limit for the 50 mm BGA package, and is not sufficient for the 8758 pins shown in Table 43.*

Table 47A. Single Chip Packages Examples - FBGA/CSP (Short Term)

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
FBGA/CSP area array pitch (mm)	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
FBGA/CSP size (mm/side)	**10**	**10**	**10**	**10**	**10**	**10**	**0.4**
# Rows/# leads (one fan-out layer)	**3/192**	**3/192**	**3/252**	**3/252**	**3/252**	**3/252**	**3/252**
# Rows/# leads (two fan-out layers)	**4/420**	**4/240**	**4/320**	**4/320**	**4/320**	**4/320**	**5/380**
FBGA/CSP size (mm/side)	**21**	**21**	**21**	**21**	**21**	**21**	**21**
# Rows/# leads (one fan-out layer)	**3/……**	**3/…..**	**3/…..**	**3/…..**	**3/…..**	**3/…..**	**3/…..**
# Rows/#leads (two fan-out layers)	**4/…..**	**4/…..**	**4/…..**	**4/…..**	**4/…..**	**4/…..**	**5/…..**

A = integer (CSP size/pitch - 1); R = # rows, # leads = (A–R) × R × 4

Table 47B. Single Chip Packages Examples - FBGA/CSP (Long Term)

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
FBGA/CSP area array pitch (mm)	**0.3**	**0.3**	**0.3**
FBGA/CSP size (mm/side)	**10**	**10**	**10**
# Rows/# leads (one fan-out layer)	**3/348**	**3/348**	**3/432**
# Rows/# leads (two fan-out layers)	**5/540**	**6/624**	**6/792**
FBGA/CSP size (mm/side)	**21**	**21**	**21**
# Rows/# leads (one fan-out layer)	**3/…..**	**3/…..**	**3/…..**
# Rows/# leads (two fan-out layers)	**5/…..**	**6/…..**	**6/…..**

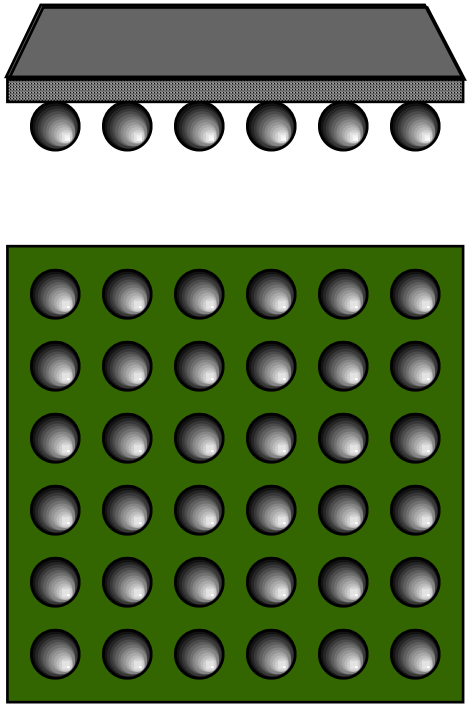
A = integer (CSP size/pitch - 1); R = # rows, # leads = (A–R) × R × 4

What is FBGA ?

- * FBGA is an IC with dimensions equal to or slightly larger than those of the silicon die it contains.
- Specifically, a package with size (L x W) equal to the size of the chip is called a Real Chip Size Package.

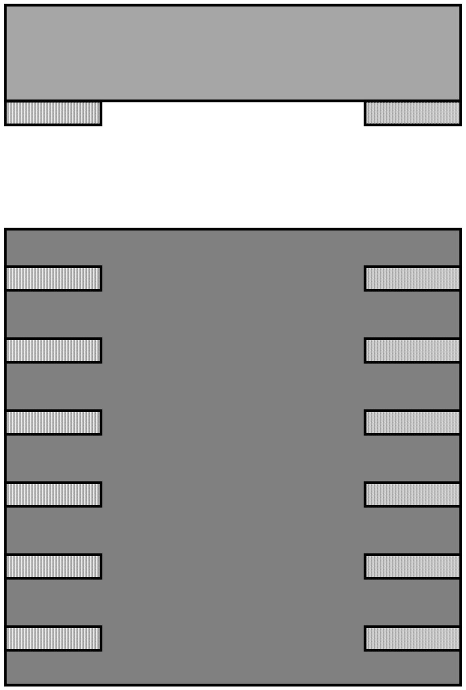
CSP Shape

Area Array CSP



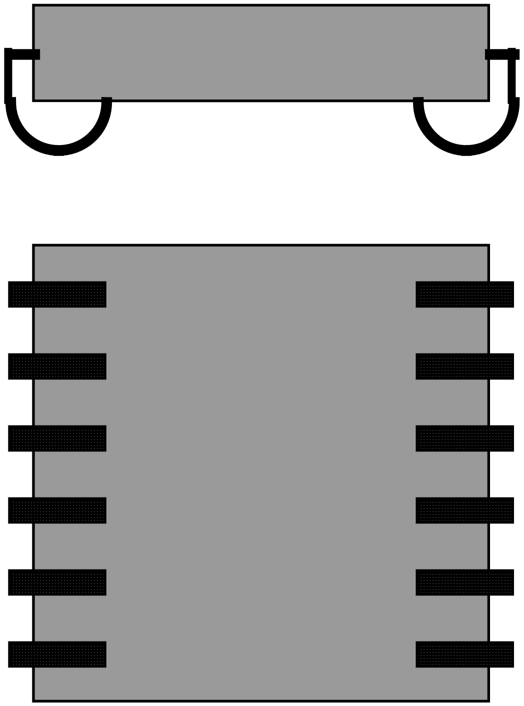
FBGA
FLGA

Peripheral CSP



SON
QFN

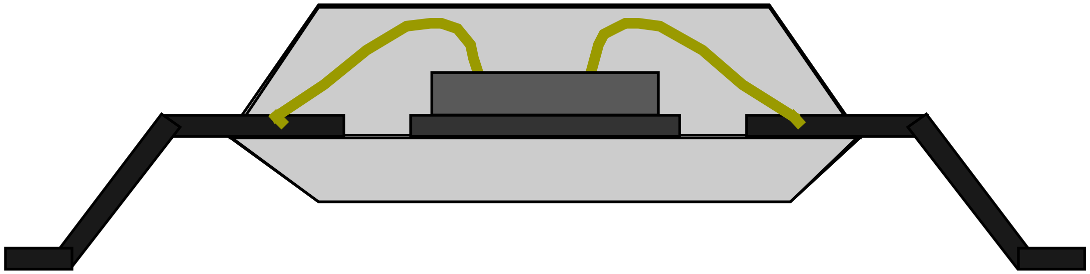
Very Small Size
Package with
Outer Lead



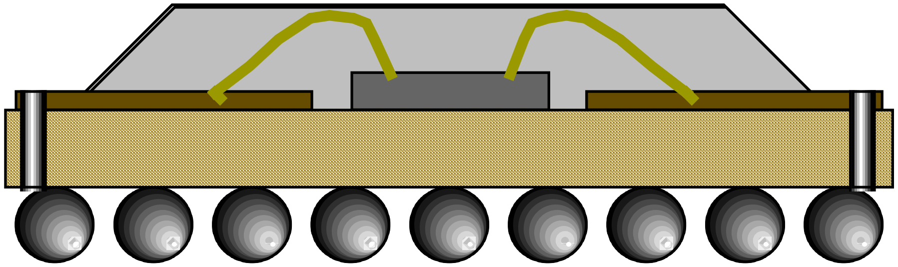
TSOJ
SOC

What is FBGA?

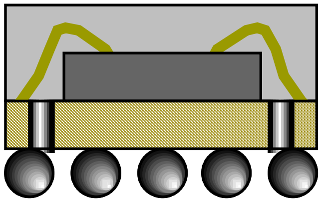
QFP



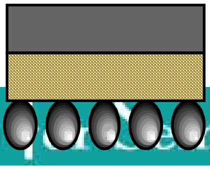
BGA



FBGA (CSP)
Wire Bonding Type



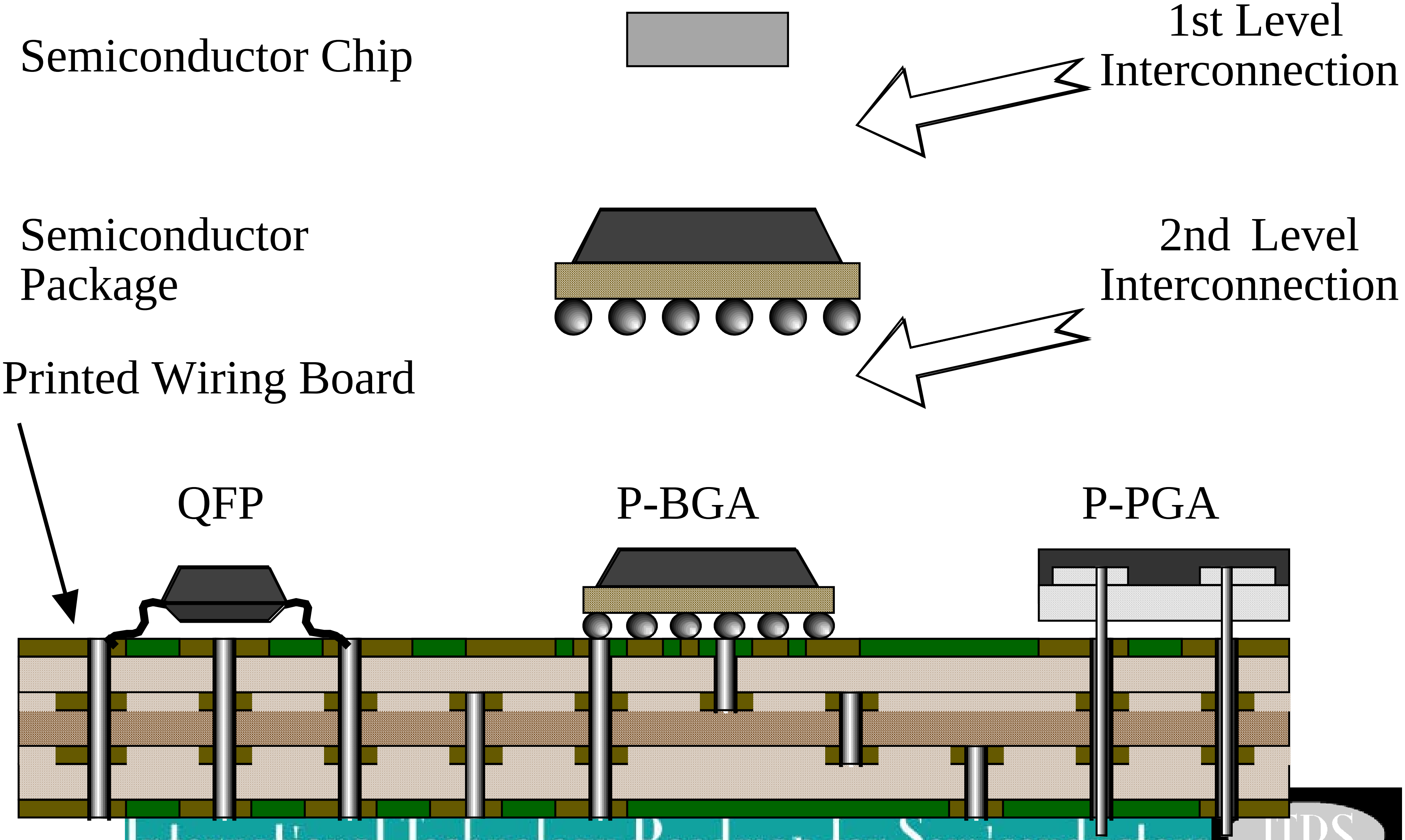
FBGA (CSP)
Wireless Bonding Type
Real Chip Size



FBGA Definition by EIAJ

- FBGA is the BGA type CSP package which includes FBGA, FLGA, SON & QFN
- Size of Package: Less than 21 mm
- Solder Ball Pad Pitch: Less than 0.8 mm
- “CSP” is a general naming for package with size equal to or slightly larger than chip size

Ä.æò (Jisso)



Semiconductor Chip

1st Level
Interconnection

Semiconductor
Package

2nd Level
Interconnection

Printed Wiring Board

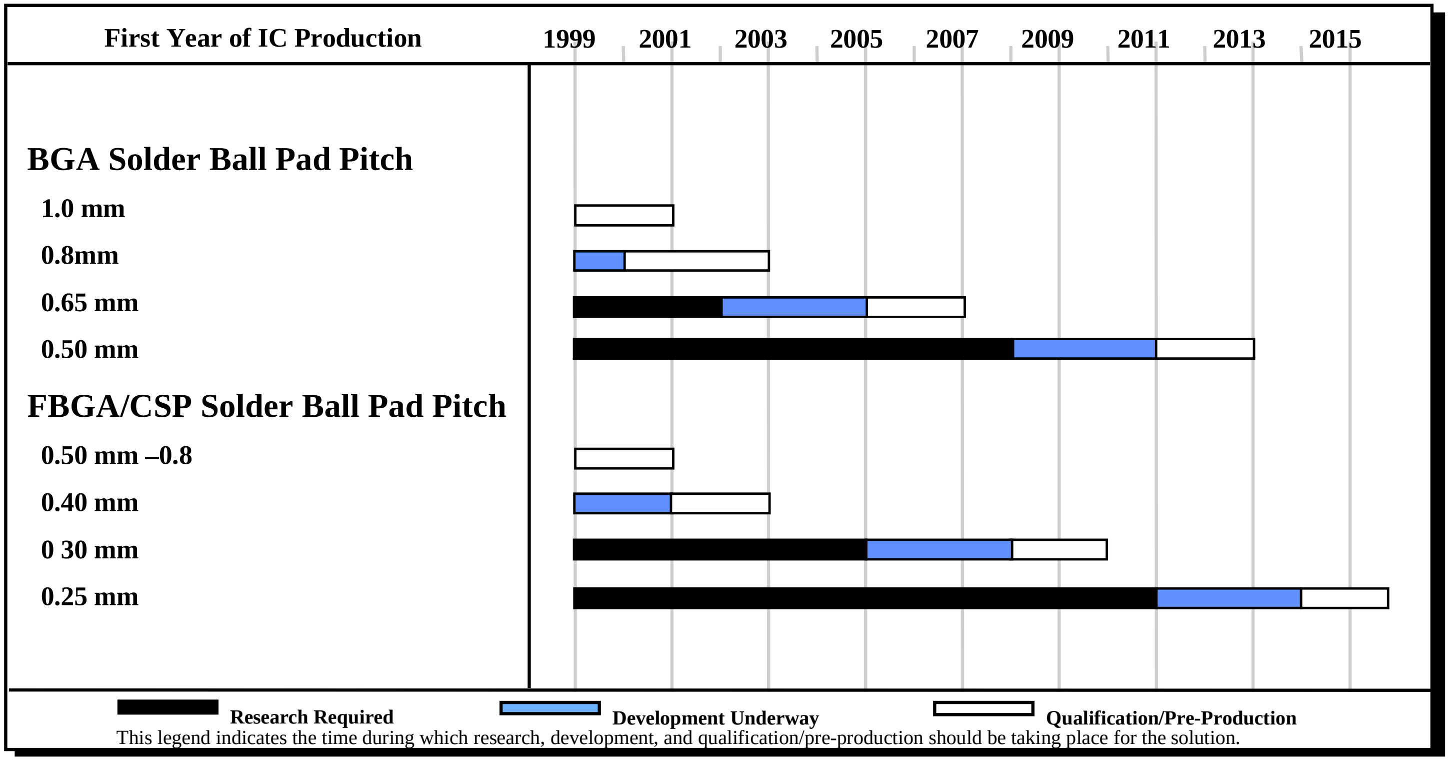
QFP

P-BGA

P-PGA

Printed Circuit Board

Figure 37. Potential PWB Solutions for BGA and FBGA/CSP Packages



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

* FBGA assumes fraction of PTH pitch requires fan-out on PWB surface

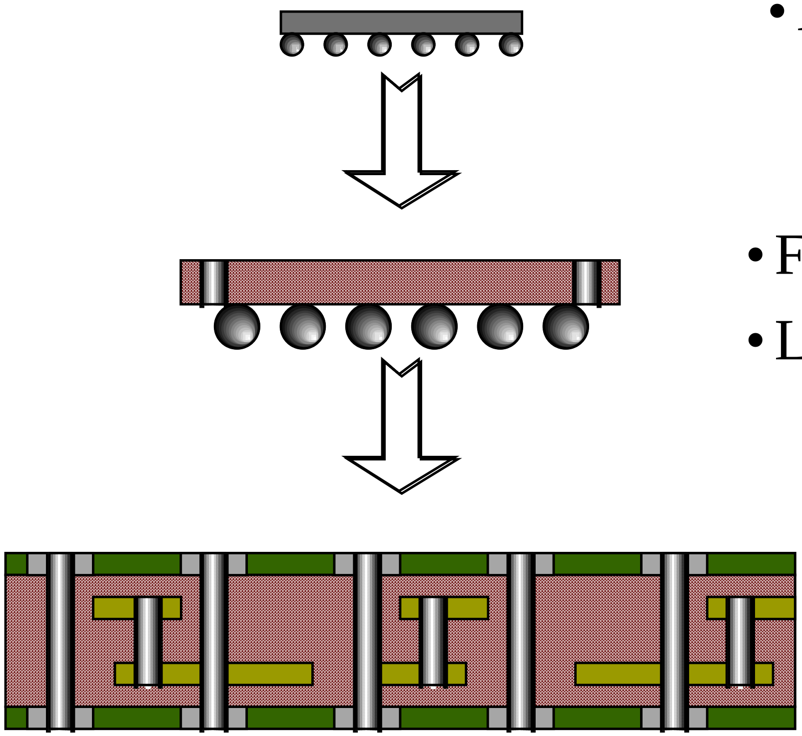
Table 48A. Potential PWB Solutions for BGA and FBGA/CSP Pkg. (Short Term)

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
FBGA/CSP solder ball pad pitch (mm)	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Pad size (µm)	**200**	**200**	**160**	**160**	**160**	**160**	**160**
Line width (µm)	**60**	**60**	**48**	**48**	**48**	**48**	**48**
Line spacing (µm)	**60**	**60**	**48**	**48**	**48**	**48**	**48**
# Rows accessed	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Table 48B. Potential PWB Solutions for BGA and FBGA/CSP Pkg. (Long Term)

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
FBGA/CSP solder ball pad pitch (mm)	**0.3**	**0.3**	**0.25**
Pad size (µm)	**120**	**120**	**100**
Line width (µm)	**36**	**36**	**30**
Line spacing (µm)	**36**	**36**	**30**
# Rows accessed	**3**	**3**	**3**

Key Role of Substrate



Bare Die

- High pad density
- High operation frequency

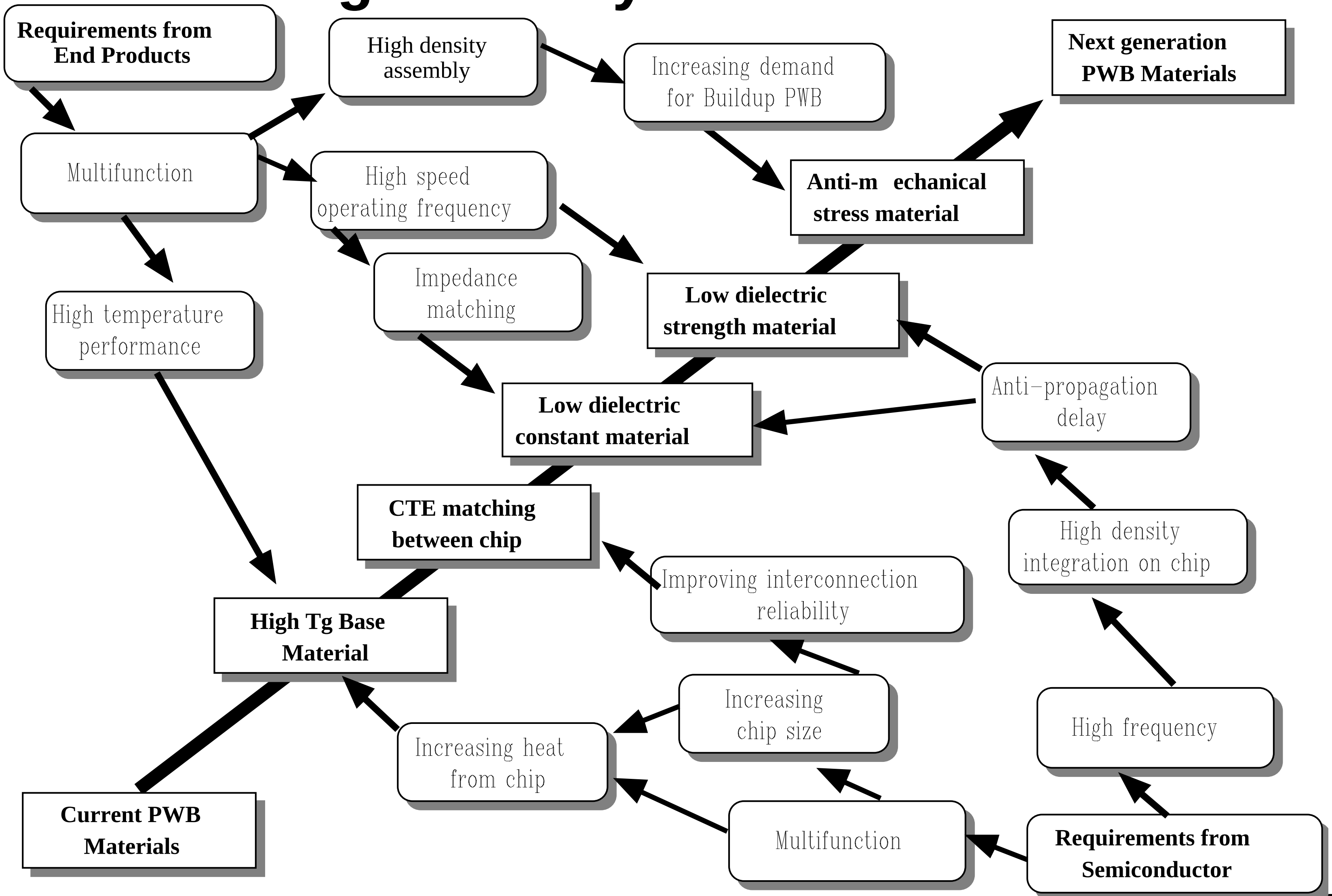
Substrate
(Interposer)

- Fine pitch interconnection
- Low capacity

Mother Board

- Fine density interconnection
- Same foot print as of Substrate

Figure 38. A Possible Solution for the Development of the High Density Substrate Materials



Requirements from End Products

High density assembly

Increasing demand for Buildup PWB

Next generation PWB Materials

Multifunction

High speed operating frequency

Anti-mechanical stress material

Impedance matching

Low dielectric strength material

High temperature performance

Low dielectric constant material

Anti–propagation delay

CTE matching between chip

High density integration on chip

Improving interconnection reliability

High Tg Base Material

Increasing chip size

High frequency

Increasing heat from chip

Current PWB Materials

Multifunction

Requirements from Semiconductor

Flip Chip Substrate Fan Out Requirements (Table 49)

- Cost Performance and high performance only
  - Only one pad pitch change at the 100 nm generation to minimize test probe head cost
- Depopulated outer row to increase fan out line width and spacing (e.g., 42µm vs. 34µm for 1999)

Table 49A. Flip Chip Substrate Top-Side Fan-Out Requirements (Short Term)

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Flip Chip Pad Pitch (µm)	**200**	**200**	**200**	**200**	**200**	**200**	**150**
Pad Size (µm) @	**100**	**100**	**100**	**100**	**100**	**100**	**75**
Chip Size (mm/side)							
Cost-performance	**12**	**12**	**12**	**12**	**12**	**12**	**12**
High-performance	**17**	**17**	**17**	**17**	**17**	**17**	**17**
Array size = # pads along chip edge							
Cost-performance (maximum)	**59**	**59**	**59**	**59**	**59**	**59**	**79**
Cost-performance (needed)	**51**	**56**	**51**	**56**	**53**	**58**	**75**
High-performance (maximum)	**84**	**84**	**84**	**84**	**84**	**84**	**112**
High-performance (needed)	**73**	**81**	**79**	**79**	**79**	**81**	**107**
# Outer Rows Accessed (will determine # fan-out layers needed)							
Cost-performance	**4**	**4**	**5**	**5**	**6**	**6**	**5**
High-performance	**6**	**6**	**7**	**8**	**9**	**10**	**8**
Effective Total Wiring Density for Fan-out Need (cm/cm^2)							
Cost-performance	**200**	**200**	**250**	**250**	**300**	**300**	**333**
High-performance	**300**	**300**	**350**	**400**	**450**	**500**	**533**
Wiring Substrate (Three or more lines replacing one depopulated pad—accessing 2.0 or more rows per fan-out layer)							
Line width (µm)	**42.5**	**42.5**	**33.0**	**33.0**	**27.0**	**27.0**	**25.0**
Line spacing (µm)	**43.1**	**43.1**	**33.6**	**33.6**	**27.5**	**27.5**	**25.0**
Wiring Substrate (Five or more lines replacing one depopulated pad—accessing 3.0 or more rows per fan-out layer)							
Line width (µm)	**27.0**	**27.0**	**23.0**	**20.0**	**17.5**	**15.5**	**15.0**
Line spacing (µm)	**27.5**	**27.5**	**23.1**	**20.0**	**17.7**	**16.0**	**15.0**
# Leads Accessed							
Cost-performance	**752**	**832**	**920**	**1020**	**1128**	**1248**	**1400**
High-performance	**1608**	**1800**	**2016**	**2272**	**2520**	**2840**	**3168**
A = array size, R = # rows, # leads = (A-R) × R × 4; via pitch must be ≤ pad pitch							

Table 49B. Flip Chip Substrate Top-Side Fan-Out Requirements (Long Term)

Year of First Product Shipment *Technology Generation*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Flip Chip Pad Pitch (µm)	**150**	**150**	**150**
Pad Size (µm)	**75**	**75**	**75**
Chip Size (mm/side)			
Cost-performance	**12**	**12**	**12**
High-performance	**17**	**17**	**17**
Array size = maximum # pads along chip edge			
Cost-performance (maximum)	**79**	**79**	**79**
Cost-performance (needed)	**75**	**75**	**78**
High-performance (maximum)	**112**	**112**	**112**
High-performance (needed)	**112**	**109**	**111**
# Outer Rows Accessed (will determine # fan-out layers needed)			
Cost-performance	**7**	**10**	**14**
High-performance	**11**	**17**	**26**
Effective Total Wiring Density for Fan-out Need (cm/cm^2)			
Cost-performance	**467**	**667**	**933**
High-performance	**733**	**1133**	**1733**
Wiring Substrate (Six or more lines replacing one depopulated pad—accessing 3.5 or more rows per fan-out layer)			
Line width (µm)	**17.0**	**11.5**	**8.0**
Line spacing (µm)	**17.5**	**12.1**	**8.6**
Wiring Substrate (Ten or more lines replacing one depopulated pad—accessing 5.5 or more rows per fan-out layer)			
Line width (µm)	**10.5**	**6.5**	**4.0**
Line spacing (µm)	**10.9**	**7.1**	**4.8**
# Leads Accessed			
Cost-performance	**1904**	**2600**	**3584**
High-performance	**4444**	**6256**	**8840**
A = array size, R = # rows, # leads = (A-R) × R × 4; via pitch must be ≤ pad pitch			

Figure 39. High Density Polymer Substrate Potential Solutions

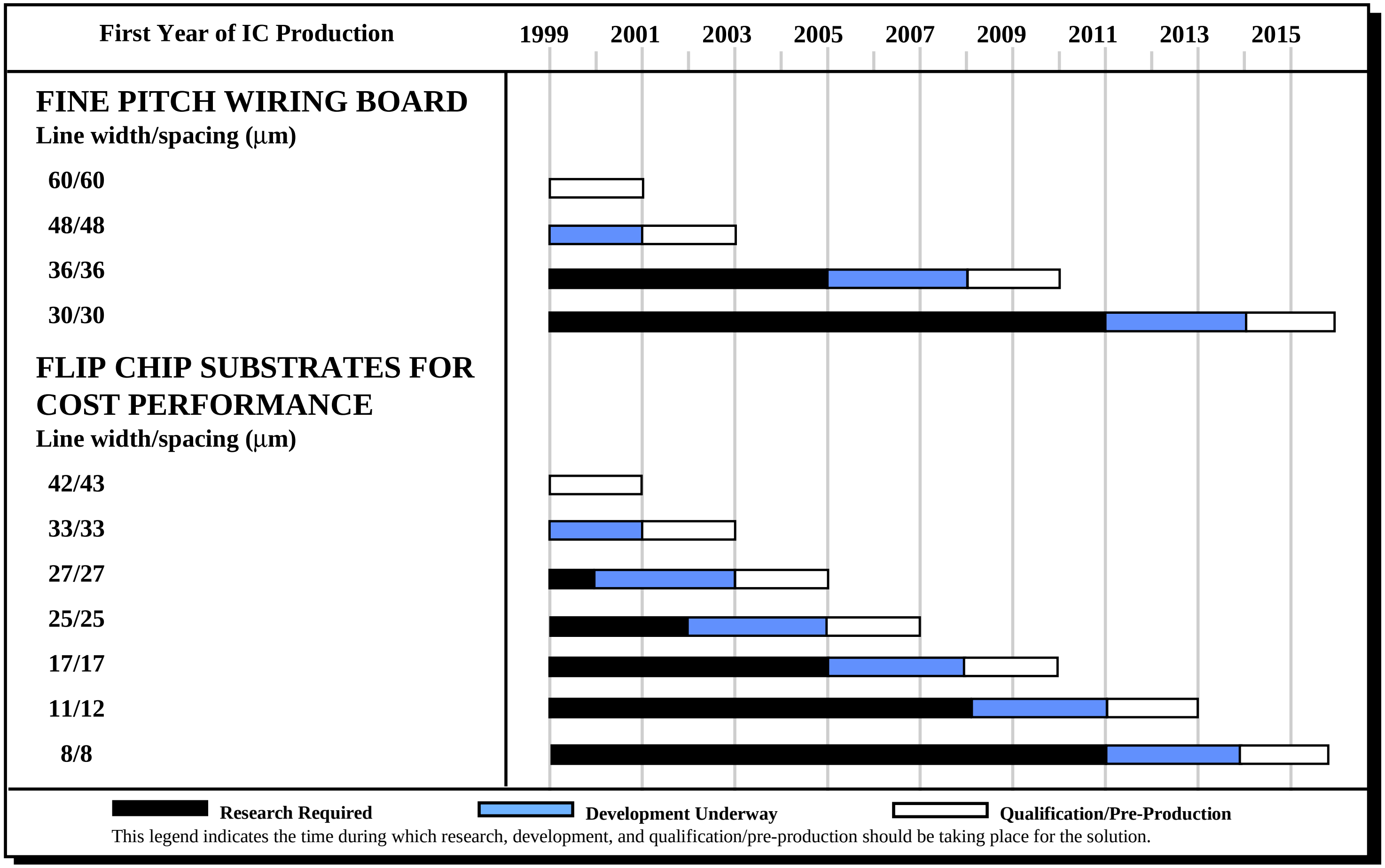


Table 51. Assembly & Packaging Modeling and Metrology Crosscut Issues

ASSEMBLY AND PACKAGING METROLOGY NEEDS	*SUMMARY OF ISSUES*
Coordinated electrical modeling and simulation tools for chip, package and system	Run-time and input preparation efficiency (results in minutes, not days) Efficient noise modeling and simulation, including radiated noise SPICE-compatible time domain simulation capability utilizing mixed RLCG-active device frequency domain models Simulation-efficient modeling algorithms and techniques which allow extraction of either element values or frequency domain models and subsequent network or order reduction Efficient full-wave analysis techniques which generate models instantiated as "stamps" in time domain simulators Integration of electrical, thermal and cost modeling and simulation tools
Improved interpretation of accelerated stress tests for process and product qualification	Modeling and simulation of accelerated stress test techniques needed to qualify manufacturing processes, and to improve the lifetime and successful operation of the product

Summary

- Invaluable input from international participants
- More work needed on cross-cut needs
- Industry feedback important