

# SIA TEST TWG ROADMAP

- **COMPANIES REPRESENTED ON THE TEST TWG**

• IBM	4	PHILIPS	1
• INTEL	3	JAPAN TWG	9 COMPANIES
• LUCENT	2	INFINEON	1
• HP	2		
• TERADYNE	2		
• MOTOROLA	1		
• TI	1		
• COMPAQ	1		
• ADVANTEST	1		
• STANFORD U	1		

# SIA TEST TWG ROADMAP

- HISTORY
  - THE 1992 ROADMAP DID NOT DISCUSS TESTING
  - THE 1994 ROADMAP HAD 4.5 PAGES WITH ONE TABLE FOR ASICs & MICROPROCESSORS.
    - THERE WAS NO MIXED-SIGNAL OR MEMORY TESTING.
    - IT PREDICTED THAT TEST VECTORS WOULD CLIMB TO 32 MILLION BY THE YEAR 2001 AND THEN FALL TO 4 MILLION BY 2010 AS BUILT-IN-SELF-TEST (BIST) DID MOST OF THE TESTING.
    - THE PREDICTION WAS CRITICIZED IN THE PRESS.

# SIA TEST TWG ROADMAP

- **THE 1997 TEST SECTION OCCUPIED ONLY 5 PAGES.**
- **IT CONTAINED TWO EQUIPMENT TABLES**
  - **DIGITAL AND MIXED-SIGNAL / WIRELESS**
- **THE DIGITAL TABLE PREDICTED THAT TEST VECTORS WOULD RISE TO 8400 MILLION BY THE YEAR 2012 UNLESS DFT / BIST WAS INTRODUCED ..... WHEN???**
- **AUTOMATIC TEST EQUIPMENT (ATE) TIMING ACCURACY IS NOT TRACKING REDUCED CLOCK CYCLES OF HIGH SPEED INTEGRATED CIRCUITS.**
  - **WAFER YIELDS COULD FALL TO 80% BY 2001!**

# SIA TEST TWG ROADMAP

- **THE 1997 ROADMAP ALSO PREDICTED THAT ATE COSTS COULD RISE TO \$20 M BY THE YEAR 2010 UNLESS DEVICE DESIGN INCORPORATED MORE DFT & BIST.**
- **THE DESIGN TWG HAS NOT BEEN ADDRESSING THIS ISSUE.**
- **DFT & BIST MUST BE INCORPORATED IN DIGITAL DESIGNS TO SOLVE THE PROBLEMS OF RISING ATE COST AND FALLING IC YIELDS DUE TO POOR TIMING ACCURACY.**

# SIA TEST TWG ROADMAP

- **THE 1999 EDITION WILL PROBABLY APPROACH 20 PAGES.**
- **PARTICIPATION BY KOREA & TAIWAN HAS BEEN ZERO.**
- **JAPANESE PARTICIPATION BEGAN IN MUNICH.**

# SIA TEST TWG ROADMAP

- **2 TEST EQUIPMENT TABLES HAVE BEEN EXPANDED TO 9.**
  - **HIGH-END MICROPROCESSORS**
  - **HIGH-END SOC**
  - **LOW-END ASICs AND MICROCONTROLLERS**
  - **MIXED-SIGNAL & WIRELESS**
  - **MEMORY TESTING**
    - **STANDARD DRAM MEMORIES**
    - **EMBEDDED DRAMs**
    - **FLASH**
  - **ATE FOR ICs WITH DFT/BIST**
  - **EQUIPMENT FOR HANDLING ICs & INTERFACING TO ATE**

# SIA TEST TWG ROADMAP

- **NEW SECTIONS IN 1999**
  - **KNOWN-GOOD-DIE TESTING**
    - REQUESTED BY THE ROADMAP COORDINATING GROUP
    - ADDRESSES FUTURE ISSUES SUCH AS FULL WAFER TESTING AND WAFER-LEVEL BURN-IN etc.
  
  - **IDDQ TESTING**
    - IMPROVES IC QUALITY BY REDUCING DEFECTIVE PPM
    - PROBLEMS OCCUR BY YEAR 2001 AS LARGE NUMBERS OF 130nm TRANSISTORS GENERATE 10 mA BACKGROUND CURRENTS.

# SIA TEST TWG ROADMAP

- **NEW SECTIONS IN 1999 ( CONT)**
- **HIGH-FREQUENCY SERIAL COMMUNICATIONS**
  - FIREWIRE, SONET, LVDS, ETHERNET etc
  - **MUST TEST 50 mV SIGNALS ON DIFFERENTIAL PAIRS OF CONDUCTORS WITH 10 ps ACCURACY AT FREQUENCIES UP TO 10 GB/s.**

# SIA TEST TWG ROADMAP

- **MAJOR CONCERNS**

- **TEST TWG MAY NOT BE ABLE TO COMPLETE SECTION BY JULY.**
- **DIFFICULT TO HAVE FACE-TO-FACE MEETINGS**
  - **PEOPLE SEEM TO HAVE TRAVEL RESTRICTIONS.**
  - **WE HAVE NO FUNDING FOR MEETINGS AT HOTELS.**
  - **MUST HOLD MEETINGS IN SEMATECH OR SRC FUNDED FACILITIES.**
  - **NOT MANY TEST TWG MEMBERS ATTEND TEST CONFERENCES BETWEEN NOW AND ITC IN SEPT 28, 1999**
- **MOST EFFECTIVE COMMUNICATIONS SEEM TO BE E-MAIL AND TELECONFERENCES WITH PRE-DISTRIBUTION OF DISCUSSION MATERIAL.**

# TEST TWG

- What is the impact of SOC on pin count?
- Are 9000 pads in the year 2014 realistic?
- Japanese ATE group has completed memory testing table but the embedded DRAM and FLASH table may not be ready for July.

# TEST TWG

- Japanese test group has generating tables for memory test and DFT, which STRJ is planning to publish in November 1999. It is not clear how much of this material should be published in the ITRS.
- DESIGN TWG only has one page briefly describing DFT and BIST.

# TEST TWG

- European TEST TWG will generate a roadmap for low cost SOC.