Metrology ITWG Participants

Europe

- Alec Reader (Philips)
- Patrick Dussouillez (ST Microelectronics)

Japan

- Fumio Mizuno (Hitachi)

US

- Bob Scace (NIST)
- Alain Diebold (SEMATECH)

Metrology Roadmap Reporting Areas

- Microscopy (Imaging)
- CD & Overlay
- Film Thickness and Profile
- Materials and Contamination Analysis
- Dopant Profile (Dose/Junct./Shape)
- In-Situ Sensors for Process Control
  (Sensor Based Metrology for Integrated Manufacturing)
- Reference Materials
- Correlation of Physical and Electrical Measurements

Highlights

* Accuracy vs Precision
- regional interpretations

* Lithography Requirements table expanded to include mask needs

* FEP tables include DRAM capacitors

Five Difficult Metrology Challenges 70 nm /Beyond 2005?

Table 60 Metrology Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 70 nm / BEFORE 2005	*SUMMARY OF ISSUES*
Factory level and company wide metrology integration for in-situ and in-line metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during RTA.
Impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials and reduced edge exclusion for metrology tools	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Detectivity of trace metals in bulk silicon or in the top silicon layer of SOI must be enhanced.
Measurement of the frequency-dependent dielectric constant of low κ interconnect materials at 5x to 10x base frequency.	Equipment, procedures, and test structures need to be reduced to practice and applied to low k interconnect materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers.

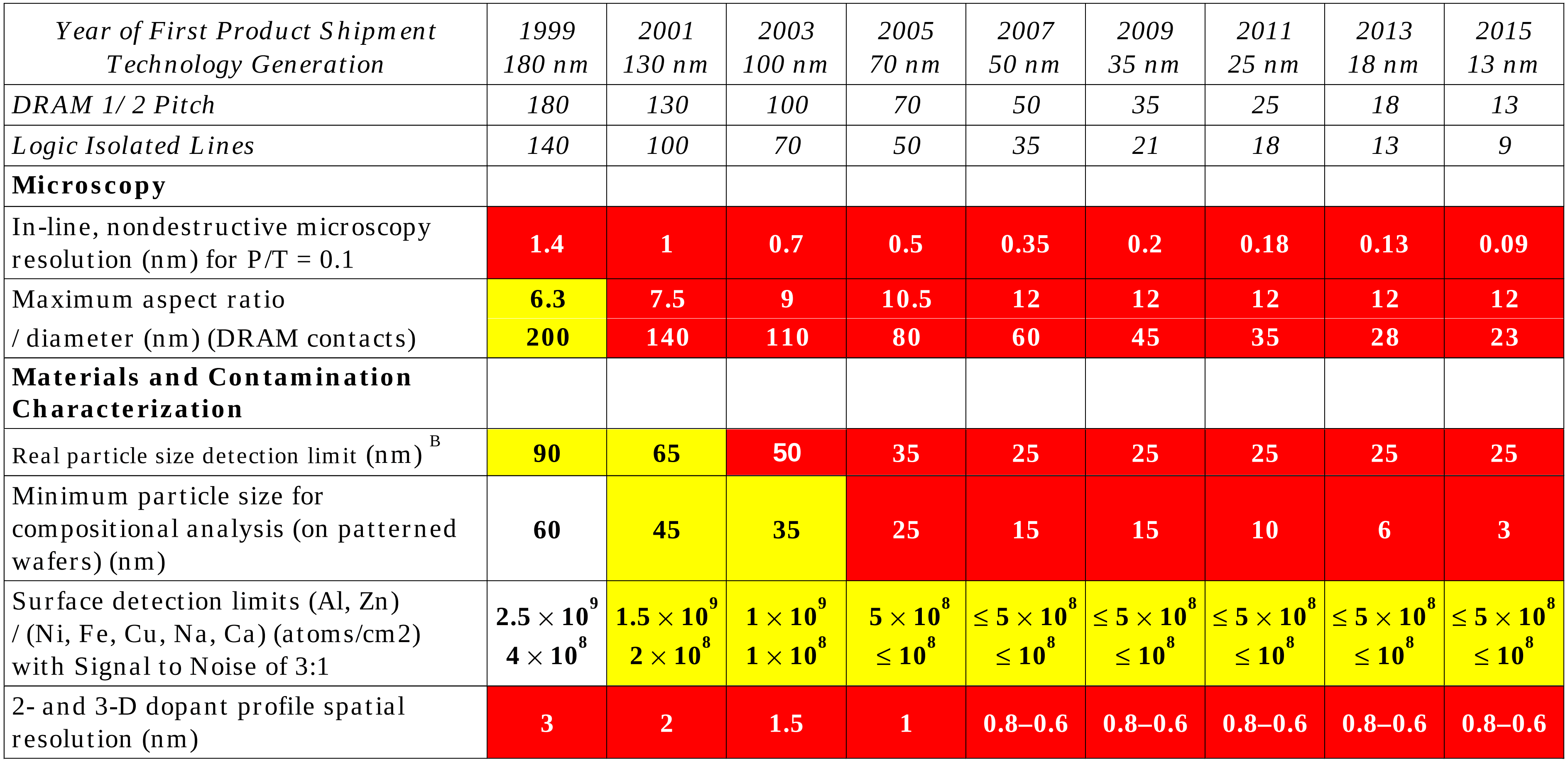
ADDITIONAL DIFFICULT CHALLENGES < 70 nm / BEYOND 2005	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement, overlay, defect detection, and analysis MOVE UP TO NEXT SECTION	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for Damascene process may require measurement of trench structures.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	**The wearout mechanism for new, high κ gate and capacitor dielectric materials is unknown.**
Statistical limits of sub-70nm process control	**Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.**
3-D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Production worthy, physical inline metrology for transistor processes that provides SPC*** required to achieve consistent electrical properties	Presently, the combined physical metrology for gate dielectric, CD, and dopant dose and profile is not adequate for sub-70nm design rules.

** FTIR—Fourier transform infrared spectroscopy*

***** SIMS—secondary ion mass spectroscopy***

****SPC—statistical process control*

Table 61a Metrology Technology Requirements



Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2001* *130 nm*	*2003* *100 nm*	*2005* *70 nm*	*2007* *50 nm*	*2009* *35 nm*	*2011* *25 nm*	*2013* *18 nm*	*2015* *13 nm*
DRAM 1/ 2 Pitch	*180*	*130*	*100*	*70*	*50*	*35*	*25*	*18*	*13*
Logic Isolated Lines	*140*	*100*	*70*	*50*	*35*	*21*	*18*	*13*	*9*
Microscopy									
In-line, nondestructive microscopy resolution (nm) for P/T = 0.1	**1.4**	**1**	**0.7**	**0.5**	**0.35**	**0.2**	**0.18**	**0.13**	**0.09**
Maximum aspect ratio	**6.3**	**7.5**	**9**	**10.5**	**12**	**12**	**12**	**12**	**12**
/ diameter (nm) (DRAM contacts)	**200**	**140**	**110**	**80**	**60**	**45**	**35**	**28**	**23**
Materials and Contamination Characterization									
Real particle size detection limit (nm) [B]	**90**	**65**	**50**	**35**	**25**	**25**	**25**	**25**	**25**
Minimum particle size for compositional analysis (on patterned wafers) (nm)	**60**	**45**	**35**	**25**	**15**	**15**	**10**	**6**	**3**
Surface detection limits (Al, Zn) / (Ni, Fe, Cu, Na, Ca) (atoms/cm2) with Signal to Noise of 3:1	2.5×10^9 4×10^8	1.5×10^9 2×10^8	1×10^9 1×10^8	5×10^8 $\leq 10^8$	$\leq 5 \times 10^8$ $\leq 10^8$	$\leq 5 \times 10^8$ $\leq 10^8$	$\leq 5 \times 10^8$ $\leq 10^8$	$\leq 5 \times 10^8$ $\leq 10^8$	$\leq 5 \times 10^8$ $\leq 10^8$
2- and 3-D dopant profile spatial resolution (nm)	**3**	**2**	**1.5**	**1**	**0.8–0.6**	**0.8–0.6**	**0.8–0.6**	**0.8–0.6**	**0.8–0.6**

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[A] *Metal and via aspect ratios are additive for dual-Damascene process flow.*

[B] *This value depends on surface microroughness and layer composition.*

Table 28 (61b ?) Lithography Metrology Requirements

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2001* *130 nm*	*2004* *100 nm*	*2007* *70 nm*	*2010* *50 nm*	*2013* *35nm*	*2016* *25nm*
Wafer Gate CD control*	**13**	**9.0**	**6.3**	**4.5**	**3.2**	**2.2**	**1.8**
Wafer Dense Line CD control*	**18**	**13**	**10**	**7.0**	**5.0**	**3.5**	**2.5**
Wafer Contact CD control*	**20**	**15**	**12**	**8.0**	**5.5**	**4.0**	**3.0**
Wafer CD metrology tool Precision* P/T = .2 for Isolated lines **	**2.6**	**1.8**	**1.3**	**0.90**	**0.64**	**0.44**	**0.36**
Wafer CD metrology tool Precision* P/T = .2 for Dense Lines**	**3.6**	**2.6**	**2.0**	**1.2**	**1.0**	**0.70**	**0.50**
Wafer CD metrology tool Precision* P/T = .2 for Contacts	**4.0**	**3.0**	**2.3**	**1.6**	**1.1**	**0.80**	**0.60**
Maximum CD measurement bias	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**
Mask CD control Isolated Lines *	**16**	**10**	**7.0**	**6.0**	**3.5**		
Mask CD control Dense Lines*	**24**	**13**	**10**	**9.0**	**6.0**		
Mask Contact Area Control Normalized to √ of Area*	**26**	**14**	**11**	**8.0**	**8.0**		

Mask CD metrology tool Precision* P/T = .2 for Isolated Lines**	3.2	2.0	1.4	1.2	0.7	🟥	🟥
Mask CD metrology tool Precision* for P/T = .2 for Dense Lines**	4.8	2.6	2.0	1.8	1.2	🟥	🟥
Mask Area metrology tool precision for contact Normalized to √ of Area - √ of Target for P/T = .2	5.2	2.8	2.2	1.6	1.6	🟥	🟥
Wafer Overlay control (nm)	65	45	35	25	20	15	10
Wafer Overlay output metrology Precision (nm, 3 sigma)* P/T = .1	6.5	4.5	3.5	2.5	2.0	1.5	1.0
Final Mask Image Placement	36	28	20	16	12	9	6
Mask Image Placement Metrology Precision P/T = .1	3.6	2.8	2.0	1.6	1.2	0.9	0.6
Mask Phase	2°	2°	2°	1°	🟥	🟥	🟥
Phase Metrology Precision P/T = .2	.4°	.4°	.4°	.2°		🟥	🟥
Variation in Attenuated Mask Film Transmission % of Deviation from Nominal	4%	4%	4%	4%	🟥	🟥	🟥
Transmission Metrology Precision % of Nominal Attenuated PSM Transmission P/T = .2	.8%	.8%	.8%	.8%	🟥	🟥	🟥

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**All precision values are 3 sigma in nm and include metrology tool matching.*

*** Measurement tool performance needs to be independent of line shape, line materials, and density of lines*

Metrology Roadmap

Table 61c Front End Processes Metrology Technology Requirements

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2001* *130 nm*	*2003* *100 nm*	*2005* *70 nm*	*2007* *50 nm*	*2009* *35 nm*	*2011* *25 nm*	*2013* *18 nm*	*2015* *13 nm*
DRAM 1/2 Pitch	*180*	*130*	*100*	*70*	*50*	*35*	*25*	*18*	*13*
Logic Isolated Lines	*140*	*100*	*70*	*50*	*35*	*21*	*18*	*13*	*9*
Oxygen range (ASTM '79 [A]) in heavily doped substrates; measurement precision ± 0.5 ppma	**19–31**	**18–31**	**18–31**	**18–31**	**18-31**	**18-31**	**18-31**	**18-31**	**18-31**
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**	**<1 x 10^{10}**
Logic dielectric equivalent thickness (nm) ± 3σ process range	**1.9-2.5** **± 4%**	**1.5-1.9** **± 4%**	**1.1-1.5** **± 4 %**	**0.8-1.2** **± 4%**	**0.6-0.8** **± 4%**	**0.5-0.6** **± 4%**	**<0.5** **± 4%**	**< 0.5** **± 4%**	**< 0.5** **± 4%**
Logic dielectric measurement precision 1σ (nm) [B]	**0.0025**	**0.0020**	**0.0016**	**0.0011**	**0.0008**	**0.0007**	**<0.0006**	**<0.0006**	**<0.0006**
DRAM capacitor structure dielectric material equivalent thickness (nm) ± 3σ process range Measurement precision 1σ (nm) [B]	**Cyl. MIS** **Ta_2O_5** **8.5** **± 4%** **0.011**	**STD MIM** **BST** **27.5** **± 4%** **0.037**	**STD MIM** **BST** **27.4** **± 4%** **0.037**	**STD MIM** **Epi-BST** **27.3** **± 4%** **0.036**	**STD MIM** **PZT?** **19.8** **± 4%** **0.026**	**STD MIM** **PZT?** **12.8** **± 4%** **0.017**	**± 4%**	**± 4%**	**± 4%**
2- and 3-D dopant profile spatial resolution (nm)	**3**	**2**	**1.5**	**1**	**0.8–0.6**	**0.8–0.6**	**0.8–0.6**	**0.8–0.6**	**0.8–0.6**
At-line dopant concentration precision (across concentration range) [C]	**5%**	**4%**	**3%**	**2%**	**2%**	**2%**	**2%**	**2%**	**2%**

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[A] *IOC '88 value obtained by multiplying ASTM value by 0.65.*

[B] *Precision calculated from P/T = 0.1 = 6 * precision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielctric constant materials such as* Ta_sO_5 will be used at and after the 70 nm logic generation. *The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants* $(\varepsilon_{high\ \kappa} / \varepsilon_{ox})$ *by the effective oxide thickness. For example, a 6.4 nm thick* Ta_sO_5 $(\kappa=25)$ *layer has a 1 nm equivalent oxide* $(\kappa=3.9)$ *thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.*

[C] *High precision measurements with low systematic error are required.*

Table 61d Interconnect Metrology Technology Requirements

Year of First Product Shipment *Technology Generation*	*1999* *180 nm*	*2001* *130 nm*	*2003* *100 nm*	*2005* *70 nm*	*2007* *50 nm*	*2009* *35 nm*	*2011* *25 nm*	*2013* *18 nm*	*2015* *13 nm*
DRAM 1/2 Pitch	*180*	*130*	*100*	*70*	*50*	*35*	*25*	*18*	*13*
Logic Isolated Lines	*140*	*100*	*70*	*50*	*35*	*21*	*18*	*13*	*9*
Planarity requirements within litho field for minimum interconnect CD (nm)	**250**	**200**	**175**	**175**	**175**	**175**	**175**	**175**	**175**
Measurement of deposited barrier layer at Thickness (nm) / process range (± 3σ) Precision 1σ (nm) for P/T= 0.1 Require profile characterization on patterned wafers[A]	**23/20%** **0.08**	**16/20%** **0.05**	**11/20%** **0.04**	**3/20%** **0.01**	**1/20%** **0.003**				
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)						1	1	1	1
Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5x to 10x clock frequency (GHz)[B]	**2.5–4.1** **1**	**2.0–2.5** **1.6**	**1.5–2.0** **2.7**	**≤ 1.5** **4.6**	**≤ 1.5** **7.7**	**≤ 1.5** **13**	**≤ 1.5** **22**	**≤ 1.5** **37**	**≤ 1.5** **62**

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*[A] *Roadmap predicts barrier for 35 nm Technology Generation will be formed by reactive processes in metal or dielectric or both instead of by deposition.*

[B] *Minimum effective dielectric constant is listed. Due to divergence of DRAM and Logic requirements ,minimum listed number is associated with logic requirements. The development of a measurement technique for low k dielectric constant and anisotropy is nearly complete up to 40 GHz. Technology transfer to industry will take place from 1999 to 2000.*