

ITRS Design Section

Munich

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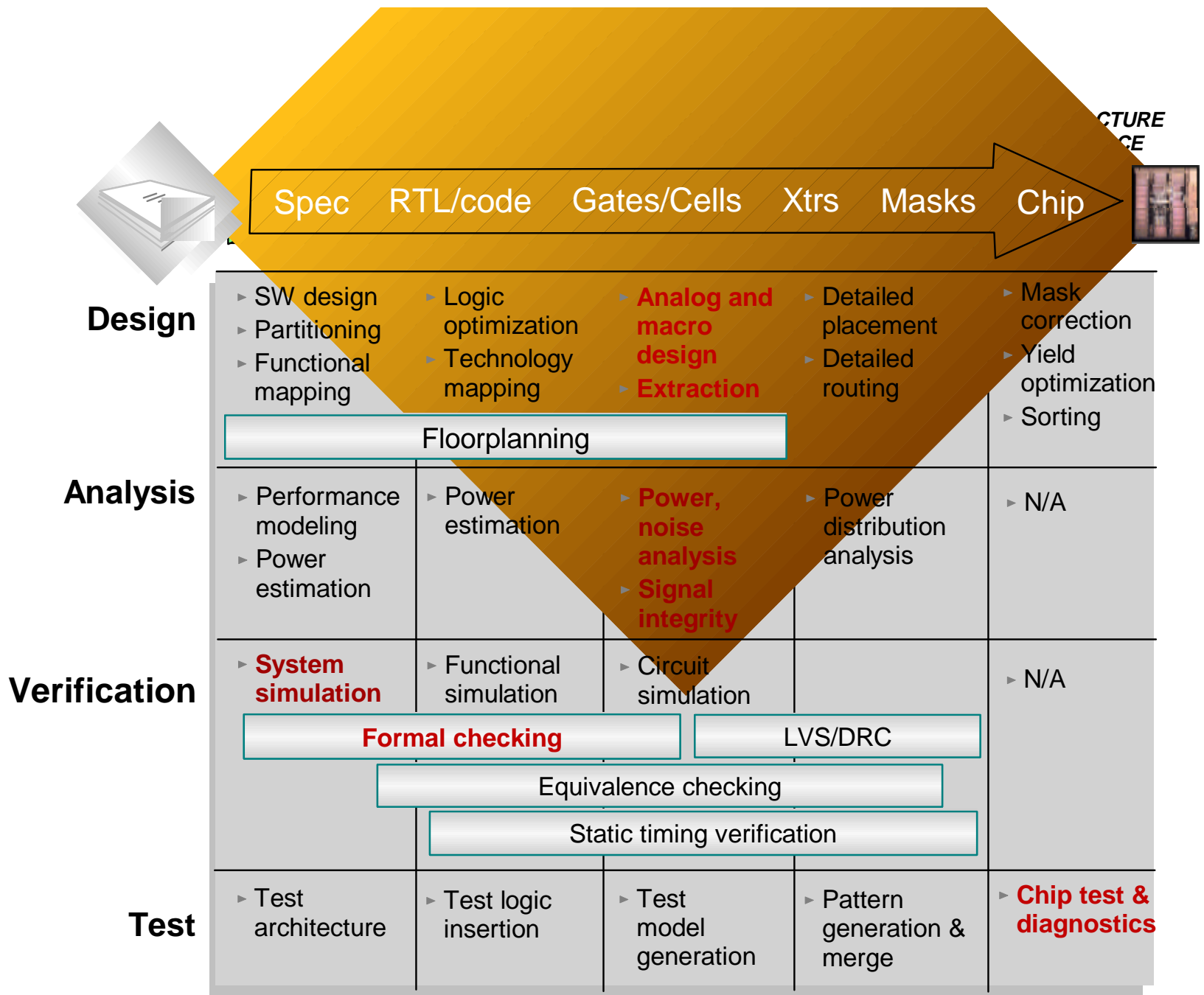
SRC/IBM

International Feedback

- ◆ System-on-a-Chip
- ◆ Analog/Mixed Signal/CMOS RF
- ◆ Design Productivity Metric
- ◆ Embedded software

Changes from 1997 NTRS

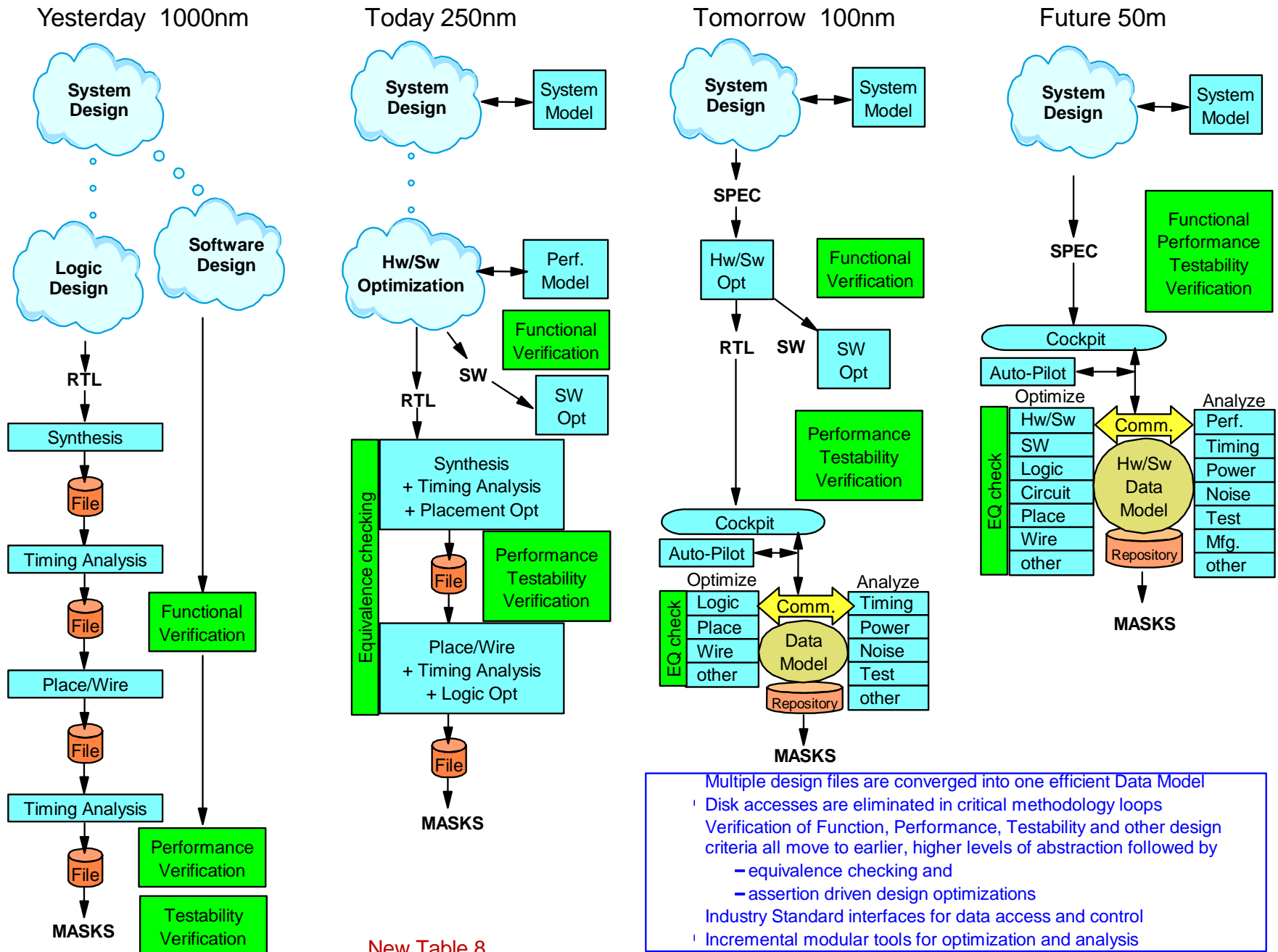
- ◆ Relate “potential solutions” figures to “difficult challenges”
- ◆ Use meaningful figures:
 - “speed/performance issue”
 - “productivity gap”
 - “D&T technology requirements”
- ◆ Replace “laundry list” of needs by:
 - specific priorities (what, when, why, cost, consequences)
 - specific bottlenecks
- ◆ Replace “ASIC” by “SOC” as key driver
- ◆ Expose new challenges:
 - embedded software
 - importance of analog/mixed signal/CMOS RF



New Figure 4 (Draft Rev. B, 3-12-99)

Red denotes most challenging activity

Required Advance in Design System Architecture



New Table 8

The Design Tool Environment

Design **productivity** requires *higher levels* of design:

- design re-use
- high-level synthesis
- system-level verification
- specialized tools operating at structured levels
- . . .

Product **functionality** and **performance** require *interacting* tools reaching from high to *circuit level*:

- synthesis/verification/PD together
- dynamic logic families
- critical timing behavior
- interconnect-aware design
- SoC with digital/analog/memory/software
- . . .



Design Complexity

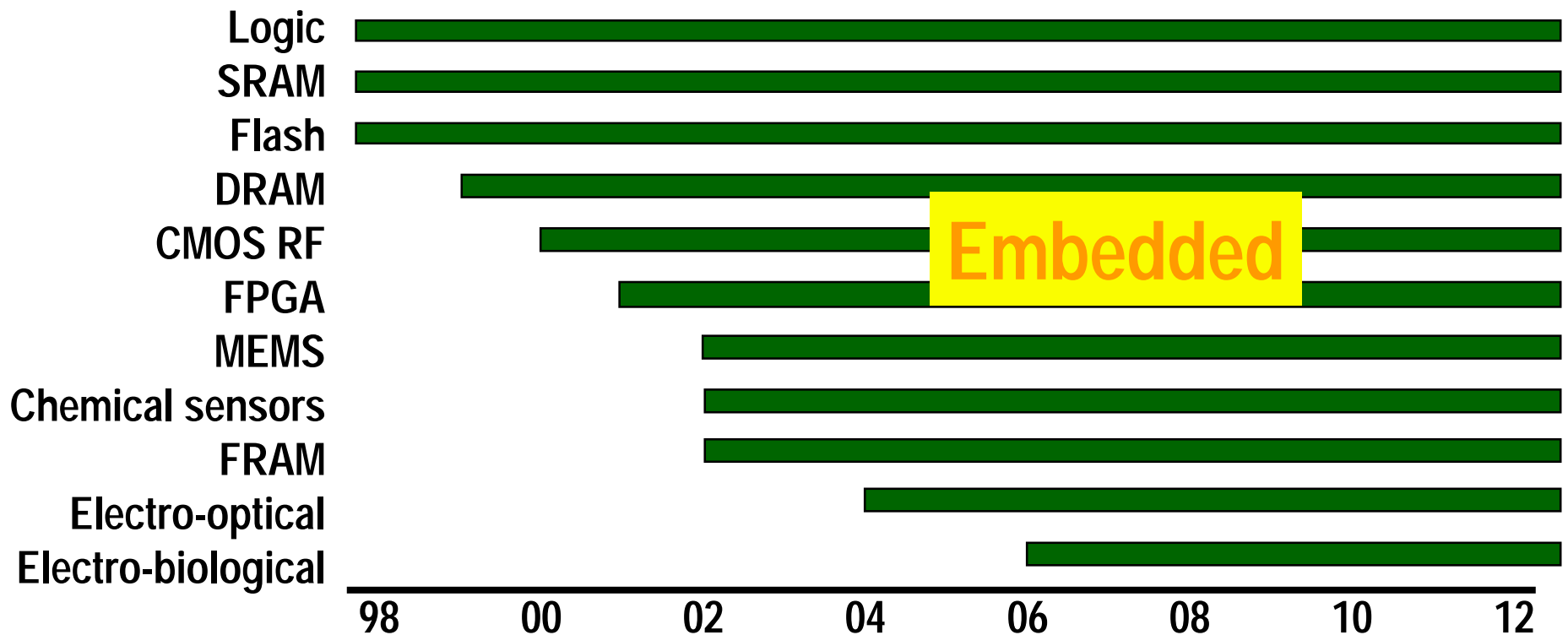
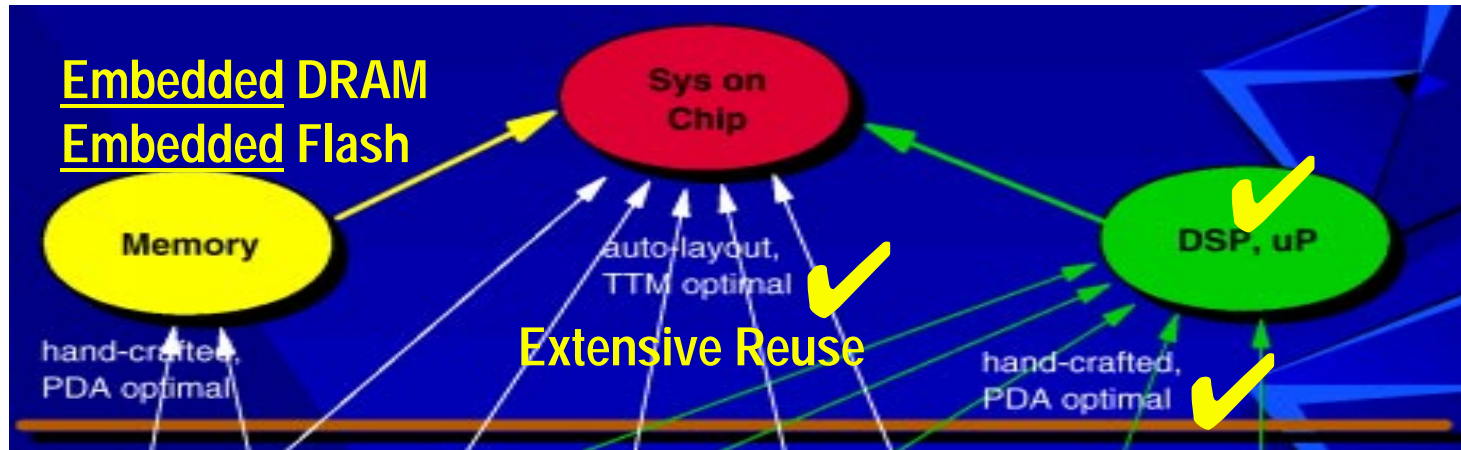
Superexponentially Increasing



Importance of System-on-a-Chip (called *System LSI* in Japan)

- ◆ *Could* be the most important category to the overall semiconductor industry in the years ahead
- ◆ Not always the largest chips. Driven by **application** in addition to **technological** factors
- ◆ Drives technology in the **mixed-technology** areas
 - Embedded DRAM, flash, FPGA, analog, CMOS RF, ...
- ◆ Drives packaging and test emphasis in significantly different directions
- ◆ Drives design technology
 - Design reuse, heterogeneous systems, embedded software
 - EDA- **Energy/Delay/Area** optimization

Importance of System-On-A-Chip



Approach to Analysis for SOC

Start Here ➔ \$\$ Categories: (e.g. \$1, \$3, \$10, \$30, \$100)

Packaging (40%?)

Test (30%?)

How many \$\$ left?

How complex a chip
can I afford?

What can I build?

Mixed technologies

Semiconductor
ITRS projections

Design reuse

System on Chip

- ◆ Capability introduction is application dependent
- ◆ Roadmap divergent rather than uniform

SoC Cost		2001	2006	2011
\$3	transistors			
	(applications)			
	capabilities			
\$25	features			
	transistors			
	(applications)			
\$100	capabilities			
	features			
	(applications)			
	transistors			

Capabilities: Logic, SRAM, Flash, DRAM, CMOS RF, FRAM, electro-optical

Features: passive devices, # layers, ...

SOC Design Productivity Table

	1999	2002	2005	2011	
Design Rule(μm)	0.25	0.13	0.10	0.05	
Size in gate count (x 10000)	500	2,000	10,000	100,000	(*3)
Logic gate count ratio (%)	80%	50%	30%	10%	
Logic Gate count (x 10000)	400	1,000	3,000	10,000	
Total Transistor count (x 10000)	2,500	10,000	50,000	500,000	
Design duration (in case of "As Is")	10 years	25 years	75 years	250 years	
Re-use circuit ratio (%)	20%	50%	70%	90%	
Newly designed circuit (x10000 g)	320	500	900	1000	
Productivity improvement(%)	100%	70%	49%	25%	(*1)
Normalized #gates for Newly Designed Circuit(x 10000 g)	320	350	441	250	
Overhead in Re-use circuit(%)	50%	25%	12.5%	3.125%	(*2)
Normalized #gates for Re-use circuit(x 10000 g)	40	125	263	281	
Normalized #gates for entire design (x 10000)	360	475	704	531	
Target Design duration (MY)	10.0	13.2	19.5	14.8	

(*1) 30% off / 3 years improvement
 (*2) 50% off / 3 years improvement

(*3) die size is assumed as 10mm \square

SOC Low Power Table

	unit	1999	2002	2005	2011
gate size	Mgates	5	20	100	1000
---->		2	10	50	500
size factor		1	4	20	200
---->		1	2.5	10	75
process	um	0.25	0.13	0.1	0.05
process factor		1	0.52	0.4	0.2
---->		1	0.47	0.32	0.14
frequency	MHz	150	400	1000	5000
frequency factor		1	2.67	6.67	33.33
---->		1	2.25	3	2.5
voltage	V	1.5	1.2	0.9	0.6
---->		1.5	1	0.5	0.3
voltage factor		1	0.64	0.36	0.16
---->		1	0.44	0.11	0.04
power trend		1	3.55	19.2	213.33
---->		1	1.17	1.07	1.05
estimation	W	3	10.65	57.6	640
---->		0.5	0.59	0.53	0.53
target	W	0.5	0.5	0.5	0.5

Key Design Focus Items

- ◆ System-on-Chip
 - cost-driven
 - heterogeneous
- ◆ IP reuse
 - reuse cost
 - standardization
- ◆ Embedded software
 - required resources growing: 30%+
- ◆ Power
 - requires significant scaleback in size, frequency
- ◆ Interconnect
 - awareness “percolating” to higher design levels