

# Defect Reduction ITWG

München, Germany

April 12-13, 1999



# Participants

| Region | Representative   |
|--------|--|
| Europe | <b>None?</b>   |
| Japan  | <b>T. Osada - Fujitsu</b>                              |
| Korea  | <b>None</b>  |
| Taiwan | <b>None</b>  |
| US     | <b>Milt Godwin - AMAT</b><br><b>David Jensen - AMD</b> |

Acknowledge Interconnect discussion with:  
Hyug Jin Kwon, Hyundai-Korea

# Difficult Challenges

- **Systematic Limited Yield**
  - Major yield limiter in 1st year
  - Model is needed for prediction and control of major contributors node to node
  - Advanced process control (feedforward and feedback) is critical to control variability
  - Tools must incorporate control for self-monitoring and self-correcting

# Yield Model

- Need model for devices with redundancy such as DRAM, SRAM, SoC
- Yield “model” needs to make sense with respect to known baseline
  - e.g. metrology budget should be less than litho budget
  - e.g. wafer handling budget should be consistent with current levels
- Yield model must comprehend:
  - cluster variability (process maturity)
  - critical area variability layer to layer
  - layer to layer PID budget

# Defect Detection

- Fast detection of scratch depth to determine depth and reliability effect
- Non-visual defect analysis and characterization is extremely critical
- Tools must be rationalized on economical proof - such as CoO
- Need statistically accurate sampling algorithms to optimize use of tools due to slow throughput
- Faster SEM Review
- **Need defect standard wafer - PSL not relevant**

# Defect Prevention and Elimination

- Separation of operator from wafer is key for yield improvement **and** reduction of in-line “noise” sources
- Solutions for wafer storage need to be cost-effective
- Check sticking coefficients for metals/organics
- Add dopants and  $(\text{SiH}_3)_2\text{O}$  to gases
- Understanding contamination mechanism is key to suppression and reduction measures
- Cross-contamination and (electrical) effect studies are very important

# DRAM Defect Density Assumptions

**GOAL:** Provide reasonable defect targets for tool suppliers

- For  $Y_{elec} = Y_s * Y_r$
- Base on “Production” Chip Size of 150mm<sup>2</sup>
- Overall Sort Yield ( $Y_{elec} = 85%$ )
  - with redundancy
- Systematic Limited Yield ( $Y_s = 90%$ )
  - at the end of “production” phase
  - just prior to entering “ramp phase” with 50% shrink
- Random Defect Limited Yield
  - $Y_r = 94%$  with redundancy (15%)
  - $Y_r = 78%$  without redundancy

# MPU Defect Density Assumptions

GOAL: Provide reasonable defect targets for tool suppliers

- For  $Y_{elec} = Y_s * Y_r$
- Base on “Ramp” Chip Size of  $160\text{mm}^2$  (@ 1999 node)
- Overall Sort Yield ( $Y_{elec} = 75\%$ )
- Systematic Limited Yield ( $Y_s = 80\%$ )
  - at the end of “ramp” phase
  - just prior to entering “peak” phase with 50% shrink
- Random Defect Limited Yield
  - $Y_r = 94\%$

# Yield and D<sub>0</sub> Summary

Further Discussion Required

|   | 1999 | 2001 | 2004 | 2007 | 2010 | 2013 | 2016 | 2019 |
|---|------|------|------|------|------|------|------|------|
| <b>Technology Node (nm)</b>                           | 180  | 130  | 100  | 70   | 50   | 35   | 25   | 18   |
| <b>Critical Dimensions (nm)</b>                       |      |      |      |      |      |      |      |      |
| DRAM 1/2 Pitch  | 180  | 130  | 100  | 71   | 50   | 35   | 25   | 18   |
| Logic 1/2 Pitch                                       | 207  | 150  | 115  | 81   | 58   | 41   | 29   | 20   |
| Logic Isolated Line                                   | 140  | 100  | 59   | 35   | 21   | 13   | 7    | 4    |
| <b>DRAM Product Roadmap (Bits)</b>                    |      |      |      |      |      |      |      |      |
| Production  | 256M | 256M | 1G   | 4G   | 4G   | 16G  | 64G  | 64G  |
| <b>DRAM Die Size (mm<sup>2</sup>)</b>                 |      |      |      |      |      |      |      |      |
| Production  | 150  | 150  | 150  | 150  | 150  | 150  | 150  | 150  |
| Ramp  | 75   | 75   | 75   | 75   | 75   | 75   | 75   | 75   |
| <b>MPU Cost-Performance Die Size (mm<sup>2</sup>)</b> |      |      |      |      |      |      |      |      |
| Ramp +2 yrs   | 160  | 170  | 187  | 206  | 226  | 249  | 274  | 301  |
| Peak +4 yrs   | 75   | 80   | 88   | 97   | 106  | 117  | 128  | 141  |
| <b>DRAM Yield (@ production phase end)</b>            |      |      |      |      |      |      |      |      |
| Sort (w/ 15% redundancy)                              | 85%  | 85%  | 85%  | 85%  | 85%  | 85%  | 85%  | 85%  |
| Systematic  | 90%  | 90%  | 90%  | 90%  | 90%  | 90%  | 90%  | 90%  |
| Random (w/ redundancy)                                | 94%  | 94%  | 94%  | 94%  | 94%  | 94%  | 94%  | 94%  |
| Random (w/out redundancy)                             | 78%  | 78%  | 78%  | 78%  | 78%  | 78%  | 78%  | 78%  |
| Random Do (killer defects/m <sup>2</sup> )            | 1718 | 1718 | 1718 | 1718 | 1718 | 1718 | 1718 | 1718 |
| Do (@ 90nm)   | 1718 | 896  | 530  | 265  | 133  | 66   | 33   | 17   |
| <b>MPU Yield (@ ramp phase end)</b>                   |      |      |      |      |      |      |      |      |
| Sort  | 75%  | 75%  | 75%  | 75%  | 75%  | 75%  | 75%  | 75%  |
| Systematic  | 80%  | 80%  | 80%  | 80%  | 80%  | 80%  | 80%  | 80%  |
| Random  | 94%  | 94%  | 94%  | 94%  | 94%  | 94%  | 94%  | 94%  |
| Random Do (killer defects/m <sup>2</sup> )            | 407  | 382  | 347  | 316  | 287  | 261  | 237  | 216  |
| Do (@ 90nm)   | 407  | 199  | 107  | 49   | 22   | 10   | 5    | 2    |
| Do (@ 70nm)   | 407  | 195  | 63   | 20   | 6    | 2    | 0.7  | 0.2  |

**DRAFT**

# Yield Model Tool Set

|                                |  |                           |
|--------------------------------|--|---------------------------|
| <b>CMP Clean</b>               |  | <b>Litho Stepper</b>      |
| <b>CMP Insulator</b>           |  | <b>Measure CD</b>         |
| <b>CMP Metal</b>               |  | <b>Measure Film</b>       |
| <b>Coat/Develop/Bake</b>       |  | <b>Measure Overlay</b>    |
| <b>CVD Insulator</b>           |  | <b>Metal CVD</b>          |
| <b>CVD Oxide Mask</b>          |  | <b>Metal Electroplate</b> |
| <b>Dielectric Track</b>        |  | <b>Metal Etch</b>         |
| <b>Furnace CVD</b>             |  | <b>Metal PVD</b>          |
| <b>Furnace Fast Ramp</b>       |  | <b>Plasma Etch</b>        |
| <b>Furnace Oxide/Anneal</b>    |  | <b>Plasma Strip</b>       |
| <b>Implant High Current</b>    |  | <b>RTP CVD</b>            |
| <b>Implant Low/Med Current</b> |  | <b>RTP Oxide/Anneal</b>   |
| <b>Inspect PLY</b>             |  | <b>Test</b>               |
| <b>Inspect Visual</b>          |  | <b>Vapor Phase Clean</b>  |
| <b>Litho Cell</b>              |  | <b>Wafer Handling</b>     |
|                                |  | <b>Wet Bench</b>          |