INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

1999 EDITION

CONTENT GUIDELINES AND FORMAT STANDARDS/
INSTRUCTIONS FOR 1999 TWG CHAPTER
DRAFT WRITING
APRIL 26, 1999

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INTRODUCTION

This book of guidelines is divided into 3 main chapters:

- Content Guidelines
  - The content guidelines show what type of information and examples of tables and figures for each section.
- Format Guidelines
  - The format guidelines are a set of instructions and styles for the document. Included is a detailed listing of styles per table.
- 1999 Chapter Template
  - The template is a blank document set that can be copied and used as a starting point for writers.

Also included is supplementary material information, the 1999 publication schedule, and contact information for assistance.

The content and format guidelines here are based on our 1997/1998 process, with some modifications adopted by the International Roadmap Committee (IRC) at our ITRS meeting held April 12-13, 1999. These guidelines are being sent to the ITRS participants over email. This information is also contained on the ITRS web site (http://www.itrs.net). To keep up with the most current version for timing cycles for the 1999 Roadmap, refer to the web site or to your TWG chair.

The IRC will be sending further information on the ORTC tables as the IRC and TWGs continue to converge on all of the numbers. For your convenience, we are including the current status of the four Lithography-related rows that were discussed with the IRC at the April 12-13 meeting in Munich. One of these rows (DRAM ½ Pitch) still defines the "technology node years" highlighted in the Roadmap. Any of these four rows may be indicated as a "Driver" for any specific row in a TWG Technology Requirements table to help simplify timing adjustments if there are future time changes in that ORTC "DRIVER" row.

SHORT TERM YEARS

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*	*DRIVER*
DRAM ½ PITCH (nm)	*180*	*165*	*150*	*130*	*120*	*110*	*100*	*D ½*
MPU GATE LENGTH (nm)	*140*	*120*	*100*	*85*	*80*	*70*	*65*	*M GATE*
MPU / ASIC ½ PITCH (nm)	*230*	*210*	*180*	*160*	*145*	*130*	*115*	*M & A ½*
ASIC GATE LENGTH (nm)	*180*	*165*	*150*	*130*	*120*	*110*	*100*	*A GATE*

LONG TERM YEARS

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	*2008 70 nm*	*2011 50 nm*	*2014 35 nm*	*DRIVER*
DRAM ½ PITCH (nm)	*70*	*50*	*35*	*D ½*
MPU GATE LENGTH (nm)	*45*	*32*	*22*	*M GATE*
MPU / ASIC ½ PITCH (nm)	*80*	*55*	*40*	*M & A ½*
ASIC GATE LENGTH (nm)	*70*	*50*	*35*	*A GATE*

This "timing snapshot" could change later; for example, if the post-2000 nodes are subsequently pulled-in by one year to match the pull-in already accepted for MPU gate length. If this happens, we will assume that rows in TWG Technology Requirements tables would shift with their designated ORTC "DRIVER" row. If no driver is indicated, there would be no automatic shift; however, interpolation would be used, as

necessary to generate new numbers for those rows in columns corresponding to "new years." For example, interpolation would be used for the 2007, 2010, and 2013 columns resulting from node shifts from the current 2008, 2011, and 2014 columns. Of course, these are just the default changes, which could be over-ridden by specific new inputs from the TWGs.

1999 Roadmap Content Guidelines

Overall Content Outline

Each TWG chapter is divided into these main sections:

- Scope
- Difficult Challenges
- Technology Requirements
- Potential Solutions
- Crosscut Issues

These sections are described further below. The Technology Requirements and Potential Solutions sections can have sub-section material. For example, the Front End Processes chapter may have the main section of Technology Requirements contain sub-sections such as Starting Materials and Surface Prep; similarly, Interconnect might have Metals and Dielectrics. The corresponding Potential Solutions sections should follow a similar sub-section structure. For more examples, refer to the 1997 edition of the Roadmap.

Page Allocation

Each focus TWG is allowed 20 pages of information. Each crosscut TWG is allowed 15 pages.

Tables/Figures

Specific tables/figures are required in the Difficult Challenges, Technology Requirements, and Potential Solutions sections. The Potential Solutions figures must follow the template provided in PowerPoint. Additional figures are allowed within the page allocation limits for each chapter at the discretion of each TWG.

Conventions

- Define all acronyms at first occurrence, like so: system on chip (SOC).
- Do not abbreviate words.
- If you use references, include the complete citation. It must be a published work. If copyrighted, include permission for use.
- Be consistent with how you use scientific notation in tables ($n \times 10^{n}$).
- Use the metric system.
- Use a space between units of measure, like so: 100 nm or 10 µm.

SECTION WRITING DESCRIPTIONS

Scope

The Scope section summarizes the key points of a TWG chapter. It lists the primary responsibilities of a TWG, and the secondary responsibilities that crosscut a particular technology area. How a TWG responds to the NTRS Grand Challenges (for example, as presented in the 1997 edition) can also be summarized in this section. Several good examples of Scope sections can be found in the 1997 edition.

Difficult Challenges

DIFFICULT CHALLENGES TABLE

Difficult Challenges are defined as requirements which will potentially not be met by the time needed and, therefore, might delay the high-level progress outlined in the Overall Roadmap Technology Characteristics tables.

A TWG lists its most difficult challenges and cites issues for those challenges, giving five difficult challenges for ≥ 100 nm/through 2005 and five for < 100nm/ beyond 2005.

- Each TWG will construct one Difficult Challenges table.
- The maximum table size is one page.

EXPLANATION NARRATIVE

The Difficult Challenges section includes a narrative that discusses where breakthroughs are needed for those technology requirements that have no known solutions at this time and may need significant invention to continue the desired trends.

DIFFICULT CHALLENGES TABLE EXAMPLE

1999 Difficult Challenges Sample Table Example (from 1998 Interconnect)

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Chip reliability	New materials and architecture (copper, low k, damascene) create some chip reliability exposure. Detecting, testing, modeling and control of new failure mechanisms will be key.
Process integration	Integrating new materials such as copper, low κ, high κ, ferroelectrics, etc., into process flows with low cost, high yield, acceptable reliability and contamination control, will be challenging.
Barriers/seed/low κ dielectric materials	Barrier and seed materials that address the electrical, mechanical and thermal integration issues with copper/ low κ must be identified
Dimensional control	Three dimensional control of critical feature size and multi-layer film thicknesses is an increasingly important predictor for circuit performance and reliability. Improved metrology, *in situ* process control, CAD* techniques and modeling are needed.
BEOL process with low/no FEOL** impact	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Dimensional control and size effects	Improved metrology, *in situ* process control and CAD techniques are needed. Microstructural and electron transport effects become important for three dimensional control.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual-damascene metal structures are also expected to be difficult.
New materials	In order to take advantage of the low resistivity and dielectric constant targets, new materials or processes must be developed. New materials are also required for system-on-a-chip needs.
Solutions after copper and low κ	Copper and low κ materials will be used for many generations. Innovations which include design and packaging enhancements or the use of rf/optical interconnect are necessary to meet future performance requirements.
BEOL process with low/no FEOL** impact	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.

EXAMPLE of TABLE
DATA NOT VERIFIED FOR 1999

**   CAD - computer aided design*
***   FEOL - front end of line*
**** BEOL - back end of line*

Technology Requirements

This section contains the "core" table showing the detailed technology area requirements over the time-span of the Roadmap. Note that the "year of introduction" shown for each requirement is to be a "leading indicator." It represents our best consensus estimate of the year in which this requirement will first be fulfilled in manufacturing at the level of at least 10,000 integrated circuits fabricated with "production tools."

This table is to be constructed as a Word table, to ensure that file conversion problems do not occur. Quantify the requirements data in the table (ideally the requirements are numbers).

- You can have multiple requirements tables or you may choose to have only one for your technology working group. Refer to the 1997 report for examples.
- Color code the data to show the status of research or development for the requirement. Remember to use white font color in the red cells. Please use the correct font style.

State of Technology Legend

- Solutions exist: White background and black text
- Solutions are being pursued: Yellow background and black text
- No known solutions: Red background and white text

The source of projections is to be noted in each cell [based on "data" † (measured or modeled) or based on best estimate by consensus or simple extrapolation ‡)].

For the 1999 ITRS, TWGs will indicate short term requirements annually through 2005, and then focus on node years at a 3-year cycle beyond 2005. Node years are based on the DRAM ½ pitch, and are noted with the dimensions. The Short Term Technology Requirements tables will indicate these node years: 1999/180 nm, 2002/130 nm, and 2005/100 nm. A "DRIVER" column indicates whether DRAM ½ pitch, MPU gate length, MPU and ASIC ½ pitch, or ASIC gate length is the technology driver for the requirements in that row. *Note that this column may be left blank if none of these is a significant driver for this row.*

Based on the "ORTC mini-table" discussed in the Introduction for these guidelines, the header for the Short Term Technology Requirements is as follows:

YEAR OF INTRODUCTION *"TECHNOLOGY NODE"*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*

The TWG Long Term Technology Requirements Table focuses on the node years every three years and indicates our best estimate of requirements for the node years through 2014. The header for the Long Term Technology Requirements table is as follows:

YEAR OF INTRODUCTION *"TECHNOLOGY NODE"*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*DRIVER*

As discussed in the Introduction with respect to the post-Munich ORTC mini-tables, this "timing snapshot" could change later; for example, if the post-2000 nodes are subsequently pulled-in by one year to match the pull-in already accepted for MPU gate length. If this happens, we will assume that rows in TWG Technology Requirements tables would shift with their designated ORTC "DRIVER" row. If no driver is indicated, there would be no automatic shift; however, interpolation would be used, as necessary, to generate new numbers for those rows in columns corresponding to "new years." For example, interpolation would be used for the 2007, 2010, and 2013 columns resulting from node shifts from the current 2008, 2011, and 2014 columns. Of course, these are just the default changes, which could be over-ridden by specific new inputs from the TWGs.

TECHNOLOGY REQUIREMENTS TABLES EXAMPLES

Below is an example of a Short Term Technology Requirements table. Based on 1998 information, the content data is not verified for 1999 and is shown only as an example (some cells are blank for this reason). Also, note that all data for an actual 1999 table should be filled in for every year, every row.

1999 Short Term Technology Requirements Table Example (based on 1998 Interconnect)

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Number of metal levels—DRAM	3	3	3	3	3	3	3–4	D ½
Number of metal levels—logic	6–7	7	7	7	7	7	7–8	M ½
Maximum interconnect length—logic (meters/chip) - top 2 global levels excluded (*)	1,700			3,300			5,000	M
Reliability—logic (FITs/meter) x 10^{-3}	1.5			0.8			0.5	M
Planarity requirements within litho field for minimum interconnect CD (nm) - defined as one third the depth of focus	250			200			175	
Minimum contacted/non-contacted pitch—DRAM (nm)	400/360			280/260			220/200	D ½
Minimum contacted/noncontacted interconnect pitch—logic (nm)	460/420			340/300			260/240	M ½
Minimum metal CD (nm) ***	180			130			100	D ½
Minimum contact/via CD (nm)	200/260			140/180			110/140	D ½
Metal height/width aspect ratio—logic (microprocessor) †	1.8			2.1			2.4	M ½
Via aspect ratio—logic †	2.2			2.5			2.7	M ½
Contact aspect ratio—DRAM using tungsten metal	6.3			7.5			9	D ½
Minimum metal effective resistivity (μΩ-cm) ‡	2.2	2.2	2.2	2.2	2.2	2.2	2.2	
Barrier/cladding thickness (nm)	23			16			11	
Minimum interlevel metal insulator—effective dielectric constant (k) §	2.5 - 4.1			2.0 - 2.5			1.5 - 2.0	

EXAMPLE of TABLE
DATA NOT VERIFIED FOR 1999

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

* *Computed at 30% metal coverage for the sum of M1 - Mn at minimum pitch for each level*

** *FIT—failure in time*

*** *Minimum CD for isolated lines (no contacts or vias)*

† Metal and via aspect ratios are additive for dual-damascene process flow

‡ Metal effective resistivity computed for the metal 2 wiring level (pitch not specified) assuming a conformal barrier

§ Dielectric constant roadmap is under critical review. The 1999 version of the roadmap will address this area in more detail.

1999 Long Term Technology Requirements Table Example (based on 1998 Interconnect)

YEAR OF INTRODUCTION	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Maximum interconnect length—logic (meters/chip) - top 2 global levels excluded (*)	9,200	17,000		M
Reliability—logic (FITs/meter) x 10^{-3}	0.3	0.1		M
Planarity requirements within litho field for minimum interconnect CD (nm) - defined as one third the depth of focus	175	175		
Minimum contacted/non-contacted pitch—DRAM (nm)	160/140	110/100		D ½
Minimum contacted/noncontacted interconnect pitch—logic (nm)	190/170	140/130		M
Minimum metal CD (nm) ***	70	50		D ½
Minimum contact/via CD (nm)	80/100	60/70		D ½
Metal height/width aspect ratio—logic (microprocessor) †	2.7	3		M
Via aspect ratio—logic †	2.9	3.2		M
Contact aspect ratio—DRAM using tungsten metal	10.5	12		D ½
Minimum metal effective resistivity (μΩ-cm) ‡	< 1.8	< 1.8		
Barrier/cladding thickness (nm)	3	1		
Minimum interlevel metal insulator—effective dielectric constant (k) §	≤ 1.5	≤ 1.5		

EXAMPLE of TABLE
DATA NOT VERIFIED FOR 1999

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

EXPLANATION NARRATIVE

This section also includes a narrative explaining key points associated with the tables.

Potential Solutions

The Potential Solutions section describes how the technology needs for each TWG might be achieved over the span of the Roadmap. All "reasonable" options for solutions should be indicated, including solutions depending on innovative research and development. Of course, additional solutions not currently known or projected may appear on future Roadmap updates. Narrowing of options is shown only as industry can no longer support multiple solutions at the next stage of development.

*POTENTIAL SOLUTIONS FIGURES (*UPDATE THESE FIGURES IN POWERPOINT; REFER TO FORMAT INSTRUCTIONS IN THE POWERPOINT FILE PROVIDED WITH THESE GUIDELINES*).*

To provide consistency, the Potential Solutions Figures in the TWG chapter reports are limited to the standard bar graphs represented by the PowerPoint template.

- Do not modify the figure grid, it is an annual timeline and provides consistency throughout the manuscript.
- Do not add new color bars to the chart and do not modify the legend.

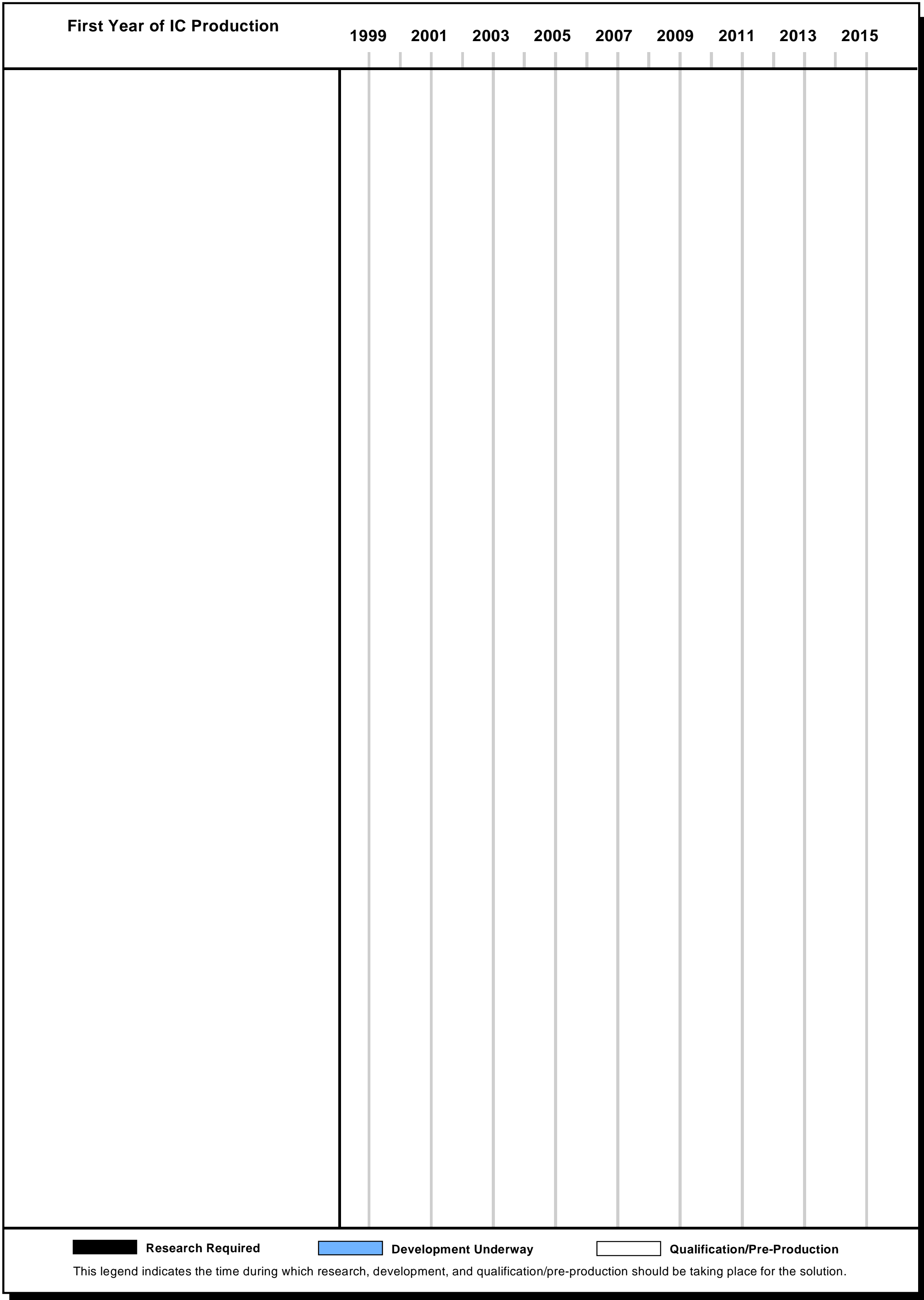
Potential Solutions Roadmap Legend

- Solution status is Research Required: Black background/white text
- Solution status is Development Underway: Light blue background/black text
- Solution status is Qualification/Pre-production: White background/black text

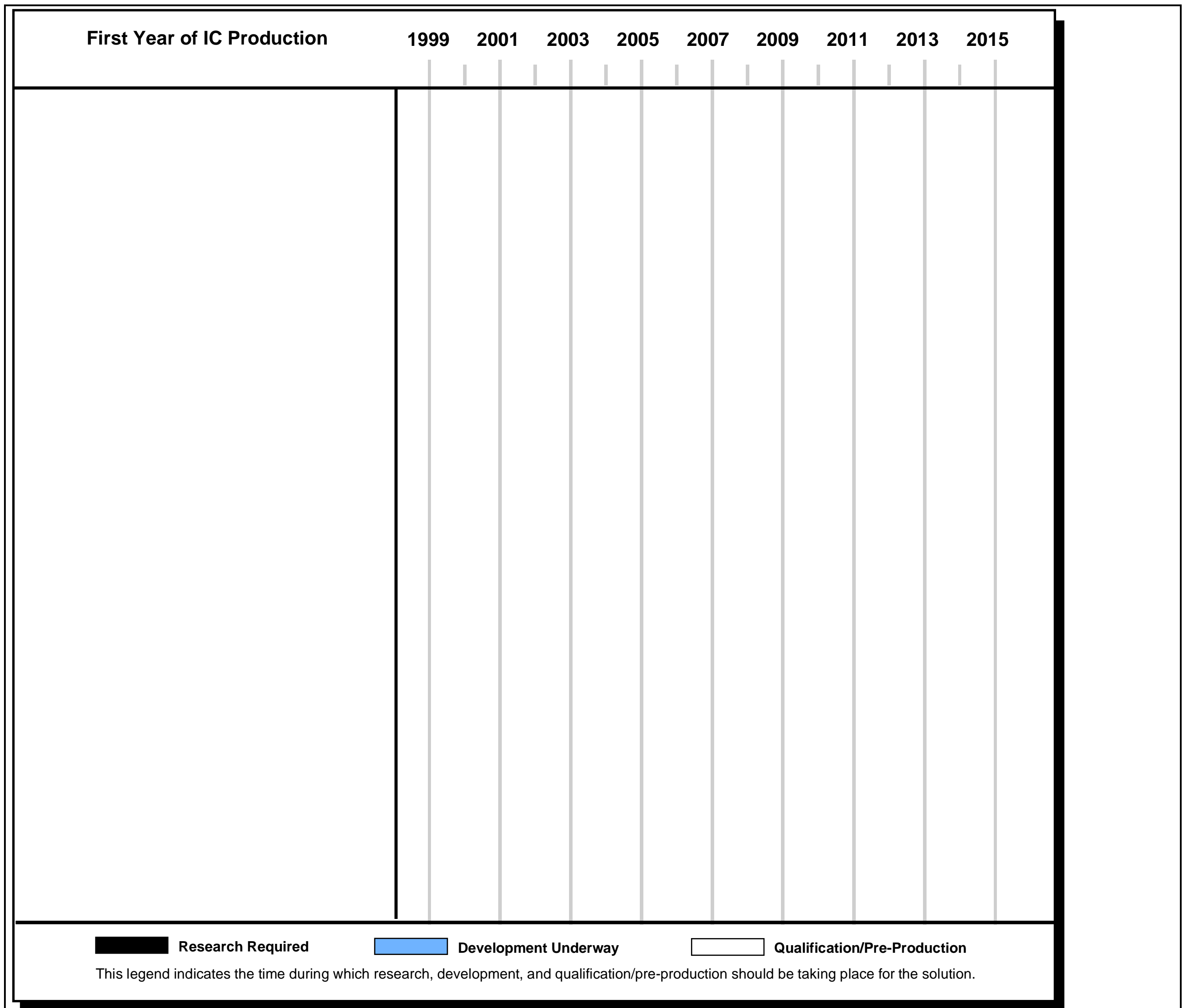
This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

EXPLANATION NARRATIVE

The Potential Solutions section includes a narrative explaining key points and considerations regarding the figures and may discuss areas of opportunities for research.



1999 Potential Solutions Template Example (this is a PowerPoint file copied as a picture)



TWG Potential Solutions ½ page

Crosscut Issues

Crosscut TWGs will have a chapter devoted to their TWG that contains Difficult Challenges, Technology Requirements, and Potential Solutions sections. For information unique to a particular Focus TWG, such as "Modeling and Simulation needs for Lithography" or "Metrology needs for Interconnect," Crosscut TWGs will contribute information to the appropriate Focus TWG in the form of one Crosscut table in each case.

The following is an example of a Crosscut Needs Table:

1999 Crosscut Needs Table Example (Modeling and Simulation Issues for Lithography)

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*
Resist Modeling	Predictive quantitative models, polymer surface interactions, coating and baking processes, silylation, edge roughness, E-beam, X-ray, and EUV resists	Establish mechanism-based models from basic studies on model materials Extend models to emerging materials Develop methodology for calibrating models on production tooling Validate models on 2-D and 3-D profiles
130 nm and Beyond	Image quality, overlay, throughput, and patterning/transfer in advance lithography systems based on EUV, X-ray, E-beam and maskless approaches, pattern dependence, stress and edge roughness in dissolution	Full system simulation of lithography tools with emphasis on balancing trade-offs in performance limiters such as resolution throughput, nonidealities in masks and mechanical and electrical components, materials inhomogeneities and transport effects in resists Simulation-based assessment of out-of-the-box approaches to maskless lithography
TCAD and Metrology	Implications of processing physics at the IC system design level, knowledge of manufacturing tolerance in simulating process design, technologist friendly tools, accurate interpretation of optical monitors, scanning probes and SEMs	Integration of TCAD with IC CAD‡ Integration of TCAD simulation with parameter extraction and statistical metrology of CIM§ Standard engineering workbench-based simulation environments Modeling of optical monitoring and SEM measurements

EXAMPLE of TABLE
DATA NOT VERIFIED FOR 1999

** OPC—optical proximity correction*
*** PPC—process proximity correction*
**** TCAD—technology computer aided design*
† SEM—scanning electron microscope
‡ CAD—computer aided design
§ CIM—computer integrated manufacturing

EXPLANATION NARRATIVE

Each Crosscut Needs Table may be accompanied by a paragraph of general explanatory text.

1999 ROADMAP FORMAT GUIDELINES

The following instructions will help you get started using the 1999 Roadmap document format template that contains the document styles.

Assumptions are that authors have a basic understanding of the Microsoft Word, and PowerPoint applications, and their hardware/software system has these applications. The document template is in Word 6.0, Windows 95. PowerPoint files are PowerPoint 4.

THE ITRS ROADMAP WORKING AREA WEBSITE

The ITRS web site will contain the format files for downloading. During draft review, the manuscript will be available for online review.

It is password protected. The userID and passcode set is available from your TWG chair.

FILES PROVIDED

Instructions and Template file – 99newfmt.doc

Powerpoint file – 99figs2.ppt

FILE / APPLICATION REQUIREMENTS

- Word 6.0
  - The 1999 document will be transferred between reviewers as a Word file. We have simplified the template and limited the document elements (Text and Tables) to Word only.
- Powerpoint 4
  - Build your figures in PowerPoint and then copy into Word inside the frame by using **Edit**, select **Paste Special** and paste **AS Picture**. This must be done inside the frame you are pasting into.

LOADING THE DOCUMENT TEMPLATE

Before you begin...	It is recommended that you create a separate directory for all the files associated with the Roadmap chapter for efficient managing and file navigation.

UPDATING TO THE ROADMAP STYLE NAMES

Please use only the styles in the document and do not modify them. This template was designed to use to help show true page allocation as well as to provide consistency with all writers.

1. At the menu bar, select the drop-down **View**, select **Normal**.

Notice that the far left of the screen now has style listings for every element (a line, paragraph, heading, or figure). You will see Style Names assigned to the Roadmap template, such as PARA1, HEAD.1, or Bullet.2.

2. Highlight the text that needs style changing. At the toolbar, press the drop-down arrow for style selection.
3. Scroll through the style names to find the correct style name.
4. Highlight the style name. The selection style will be changed. The left margin will now show the updated style name for the selection.

1999 ROADMAP STYLE SHEET

(This copy of the most used styles and their definitions is provided for authors to pull out and have readily available while writing.)

Text Type	*Style Name*	*Looks Like*
Heading for TWG chapter (Table of Contents, level 1)	HEAD.1	HEAD.1
Heading for section (e.g., Scope, Difficult Challenges, …) (Table of Contents, level 3)	HEAD.3	HEAD.3
Heading for subsection (e.g., Breakthroughs Needed) (Table of Contents, level 4)	HEAD.4	*HEAD.4*
Paragraph (or Body)	PARA1	PARA1
Bulleted list	BULLET.stac	• BULLET.stac
Numbered list	NUM.stac	1. NUM.stac
Figure title (List of Figures)	fig_title	*Figure Title*
Figure frame	FRAME.roadmap	FRAME.roadmap
Table title (List of Tables)	Table:Title	*Table:Title*
Technology Requirements Table Row Item Titles	Table:lev2	*Table:lev2*
Technology Requirements Table Row Descriptions	Table:lev3	Table:lev3
Technology Requirements Table data text - Solutions Exist	Table:txt8B	Table:txt8B
Technology Requirements Table data text - Solutions Being Pursued	Table:txt8Y	Table:txt8Y
Technology Requirements Table data text - No Known Solutions	Table:txt8W	Table:txt8W
Crosscut Tables Table text lists	Table:List	Table:List
Table notes (located at the bottom of a table)	Table:note_8i	*Table:note_8i*

STYLES FOR TEXT

HEAD.1 – TWG CHAPTER TITLE

HEAD.3 (12 PT) - SCOPE

PARA1 (10 pt) – Paragraph text

HEAD.3 (12 PT) - DIFFICULT CHALLENGES

PARA1 – (10 pt) Paragraph text

HEAD.3 (12PT) – TECHNOLOGY REQUIREMENTS

PARA1 (10 pt) – Paragraph text

HEAD.4 (11 PT) –SUB SECTION

PARA1 (10 pt) – Paragraph text

*ParaTitle (10 pt) – Title leading paragraph—*PARA1 (10 pt) – Paragraph text

(Example from 1997 Front End Processes chapter follows)

*Epitaxial Wafer—*The improved GOI in epitaxial material is due to the improved structural perfection of epitaxial material as compared to residual polishing micro-damage and grown-in micro-defects in polished wafers. Surface microroughness excursions may become more significant in degrading device performance as the gate dielectric thickness approaches a few unit cells.

HEAD.3 (12PT) – POTENTIAL SOLUTIONS

PARA1 (10 pt) – Paragraph text

HEAD.4 (11 PT) –SUB SECTION

PARA1 (10 pt) – Paragraph text

- Use PowerPoint files to create all figures. Build your figures in PowerPoint and then copy into Word inside the frame by using **Edit**, select **Paste Special** and paste **AS Picture**.

HEAD.3 (12PT) – CROSSCUT ISSUES

PARA1 (10 pt) – Paragraph text

HEAD.4 (11 PT) –SUB SECTION

PARA1 (10 pt) – Paragraph text

STYLES FOR TABLES

DIFFICULT CHALLENGES TABLE STYLES

Table:Title (11 pt) - Table # TWG Difficult Challenges

TABLE:LEV1C -8 PT FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	TABLE:LEV1C -8 PT SUMMARY OF ISSUES
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
TABLE:LEV1C -8 PT FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt
Table:List – 8pt	Table:List – 8pt

THE TECHNOLOGY REQUIREMENTS TABLE STYLES

Table:Title (11 pt) - Table # TWG Short Term Technology Requirements Title

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Table:lev2 (8 pt) Title of Item / Characteristics								
Table:lev3 (8 pt) subItem (unit)	Table:txt 8B	Table:txt 8B	Table:txt 8B	Table:txt 8B	Table:txt 8B	Table:txt 8B	Table:txt 8Y	
Table:lev3 (8 pt) subItem (unit)	Table:txt 8B	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	
Table:lev3 (8 pt) subItem (unit)	Table:txt 8B	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	Table:txt 8Y	Table:txt 8W	
Table:lev3 (8 pt) subItem (unit)	Table:txt 8B	Table:txt 8W	Table:txt 8W	Table:txt 8W	Table:txt 8W	Table:txt 8W	Table:txt 8W	
Table:lev3 (8 pt) subItem (unit)	Table:txt 8B	Table:txt 8W	Table:txt 8W	Table:txt 8W	Table:txt 8W	Table:txt 8W	Table:txt 8W	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table:Title (11 pt) - Table # TWG Long Term Technology Requirements Title

YEAR OF INTRODUCTION	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Table:lev2 (8 pt) Title of Item / Characteristics				
Table:lev3 (8 pt) subItem (unit)	Table:txt8B	Table:txt8B	Table:txt8B	
Table:lev3 (8 pt) subItem (unit)	Table:txt8B	Table:txt8Y	Table:txt8Y	
Table:lev3 (8 pt) subItem (unit)	Table:txt8B	Table:txt8Y	Table:txt8Y	
Table:lev3 (8 pt) subItem (unit)	Table:txt8B	Table:txt8W	Table:txt8W	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

CROSSCUT TABLE STYLES

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*
Table:List	Table:List	Table:List
Table:List	Table:List	Table:List
Table:List	Table:List	Table:List

UPDATING TABLE OF CONTENTS AND LISTS OF TABLES AND FIGURES

The Roadmap template provides a pre-defined Table of Contents and Lists for Tables and Figures. Since these are fields, these text areas have a gray background.

Note: Your document headings, figure titles, and table titles must be defined in the correct style for this feature to work. Please refer to the style name descriptions and the sample style page in this document appendix, "Updating to Roadmap Styles."

1. To update, place your cursor in the text area of the table or list to be updated.
2. Press the F9 key.
3. Select **Update Entire Table**. Click **OK**. The data fields will update to reflect the latest headings, figure and table titles.

Repeat these steps for each list.

CHARACTER MAPS FOR SPECIAL CHARACTERS

(Print these sheets for convenience.)

To insert a special character:
Use either the key for that character or the combination keystroke:
ALT key with ANSI code number

For example,
To insert a symbol for delta Δ, press the "D" key,
then change that character from New Century to Symbol font

To insert the less than or equal to ≤,
hold the ALT key down and type 0163,
then change that character to the Symbol font

To change a character from New Century to Symbol,
highlight the character in the edit line at the top of the screen

At the top menu bar, pull down Format,
select Cells. At the font selection, change the font to Symbol. Click OK.

The key or ANSI code is shaded beneath each character.

Symbol Font

!	∀	#	∃	%	&	(	)	*	+
!	"	#	$	%	&	(	)	*	+
,	−	.	0	1	2	3	4	5	6
,	-	.	0	1	2	3	4	5	6
7	8	9	:	;	<	=	>	?	≅
7	8	9	:	;	<	=	>	?	@
Α	Β	Χ	Δ	Ε	Φ	Γ	Η	Ι	ϑ
A	B	C	D	E	F	G	H	I	J
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1999 Chapter Template

The following is a template that a writer can use to copy and use for writing the TWG chapter. Styles are already in place.

TWG Chapter Title

Scope

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Difficult Challenges

Paragraph text

Table:Title (11 pt) - Table #   TWG Difficult Challenges

TECHNOLOGY REQUIREMENTS

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SUB SECTION

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Table:Title (11 pt) - Table # TWG Short Term Technology Requirements Title

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes:

Table:Title (11 pt) - Table # TWG Long Term Technology Requirements Title

YEAR OF INTRODUCTION	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

POTENTIAL SOLUTIONS

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SUB SECTION

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Use PowerPoint files to create all figures. Copy figures into the Word document as **Edit, Paste Special, Picture.**

Paste Picture from Powerpoint Here

Figure # Potential Solutions

CROSSCUT ISSUES

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SUB SECTION

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Table #   TWG Crosscut Issues

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*

SUPPLEMENTARY MATERIAL

The 1999 Roadmap publication will be primarily electronic, and will have the ability to have electronic links to other chapters and sections and to supplementary files.

All TWGs are encouraged to have materials (additional text, figures, tables, formulas) that support or add detail to their TWG chapter. This information will be part of the 1999 roadmap as an interactive material. These materials are separate supplemental files.

The format for this supplementary materials is at the discretion of the TWG chairs. For consistency for a reader, it is encouraged that the Roadmap format be followed as much as possible.

The software must be the same as required for the Roadmap. Please supply supplementary materials in Word or PowerPoint.

PUBLICATION SCHEDULE

•Feb - April	– TWGs write chapters
•April 12-13	– ITRS meeting Munich
•Apr 19 - June 11	– ITWGs write chapters - Create rough draft
•June 2-3	– US Roadmap Workshop
•June 11	– TWGs send updated material to Linda Wilson
•June 11 - July 26	– First Draft compiled
	– Edit sessions June 24 - 29
•June 30	– Pre-reading summaries for Conference due
	– 1st Draft posted
•July 7	– ITRS meeting
•July 8-9	– Roadmap Conference
•July 26	– ITWGs send updates to Linda Wilson
•July 26-Aug 12	– 2nd Draft compiled - changes from this point on are minor
	– Edit sessions Aug 6 - 11
	– Supplementary material links are identified
•Aug 15	– 2nd Draft posted
•Aug 20 - Aug 26	– Final changes are due
•Aug 27	– Sent to advisory boards for review/corrections/approval
•Aug 27 - Sept 9	– Corrections and final changes made, based on feedback
•Sept 17	– Content is frozen
•Sep 28-Oct 1	– Proof copy is approved by ITWGs
•Oct 15	– To CD producer and offset printer
•November 15	– Distribution

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