ITRS RCG

Interconnect TWG

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8 January 1999 DFW

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15 minutes

- **Membership**
- **Difficult Challenges (Table 31)**
- **Technology Requirements (Table 32)**
- **Architecture Solutions (Table 33)**
- **Plan through 6/99**

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1998/9 Membership

Lucent Technologies
Bell Labs Innovations

Christopher Case, chair

Bob Havemann, co-chair

SEMATECH
Marilyn Jones

Bob Geffken, ITWG rep

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Applied Materials
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Stanford
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SRC
Jim Hutchby

Sandia
Bruce Draper

Dennis Hartman

RPI
Shyam Murarka

U of New Mexico
Joe Cecchi

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Interconnect Scope

- 1994 NTRS introduced need for Cu and low k materials
- 1997 NTRS describes the adoption of these materials

Interconnect Theme

- Rapid changes in materials - to Cu, new barriers and the many low k solutions is without precedent
- Materials solutions for full-chip performance beyond 100 nm technology node are unknown
- Interconnect limitations will be circumvented by design and architecture solutions

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Difficult challenges Table 31

- **Issue: How to incorporate DRAM specific challenges**
- **Resolution: Incorporate into supporting text for Table 31**
- **Issue: wording of process integration challenge**
- **Resolution: modified text**
- **Other:**
  - **Added new challenge - Materials to meet k and resistivity targets**
  - **Added new description for BEOL processes with low or no FEOL impact**

Table 31 Difficult Challenges > 100 nm, rev. 1/99

Five Difficult Challenges ∨>100 nm / Before 2005	**Summary of Issues**
Chip Reliability	New materials and architecture (copper, low κ, damascene) create some chip reliability exposure. Detecting, testing, modeling and control of new failure mechanisms will be key.
Process Integration	Integrating new materials such as copper, low k, high k, ferroelectrics, etc., into process flows with low cost, high yield, acceptable reliability and contamination control,will be challenging.
Barriers/seed/low κ dielectric materials	Barrier and seedmaterials that address the electrical, mechanical and thermal issues with copper/ low κ.
Dimensional control	Three dimensional control of critical feature size and multi-layer film thicknesses is an increasingly important predictor for circuit performance and reliability. Improved metrology, *in situ* process control, CAD techniques and modeling are needed.
BEOL process with low/no FEOL** impact	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.

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Table 31 Difficult Challenges . 100 nm, rev. 1/99

Five Difficult Challenges < 100 nm / Beyond 2005	**Summary of Issues**
Dimensional control and size effects	Improved metrology, *in situ* process control and CAD techniques are needed. Microstructural and electron transport effects become important for 3D control.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual damascene metal structures are also expected to be difficult.
New materials	In order to take advantage of the low resistivity and dielectric constant targets, new materials or processes must be developed. New materials are also required fro system-on-a-chip needs.
Solutions after copper and low κ	Copper and low k materials will be used for many generations. Innovations which include design and packaging enhancements or the use of rf/optical interconnect are necessary to meet future performance requirements.
BEOL process with low/no FEOL** impact	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.

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Interconnect Tech Requirements Issues

- **Does not adequately distinguish MPU and DRAM requirements**
- **Metal level and pitch need to be directly linked and clarified**
- **Contact metal for DRAM should be specified**
- **Planarity requirements not explained**
- **Excluded Cu/SiO2 @ 180 nm as potential solution**
- **Calculation of effective resistivity not described**
- **Maximum interconnect length should be explained**

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Table 32 1/15/99 plan

- **For 1/15/99 1998 update:**
  - **Add W metal for Contact A/R DRAM spec**
  - **Modify ILD effective k @ 180 nm to read 3.0 to 4.1**
  - **Add planarity definition as 1/3 litho DOF**
  - **Explain effective resistivity calculated from M2 pitch with conformal barrier**
  - **Define maximum wiring length computed for die size at 30% coverage**
  - **Include further explanations of computed requirements into supporting text**

Table 32 1999 plan

- **For 1999 edition:**
  - **Entire rewrite begun**
  - **Separate MPU/DRAM technology specific requirements**
  - **Add separate requirements for Cu and Al wiring, where appropriate (ILD and k)**
  - **Add additional detail for M0, M1 - n, and power/ground levels design rules and CDs**

Technology Requirements, 1/99

		1999 *180 nm*	*2001* *150 nm*	*2002* *130 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*
Number of metal levels - DRAM		**3**	**3**	**3**	**3 - 4**	**4**	**4**
Number of metal levels - Logic		**6 - 7**	**6 - 7**	**7**	**7 - 8**	**8 - 9**	**9**
Maximum interconnect length - Logic (meters/chip)		**1,480**	**2,160**	**2,840**	**5,140**	**10,000**	**24,000**
Reliability - Logic (FITS/meter) X10 $^{-3}$		**1.7**	**1.3**	**0.9**	**0.5**	**0.2**	**0.1**
Planarity requirements within litho field for minimum interconnect CD (nm) - 1/3 DOF		**250**	**230**	**200**	**175**	**175**	**175**
Minimum contacted/non-contacted interconnect pitch - DRAM (nm)		**400/360**	**330/300**	**280/260**	**220/200**	**160/140**	**110/100**
Minimum contacted/non-contacted interconnect pitch - LOGIC (nm)		**460/420**	**390/360**	**340/300**	**260/240**	**190/170**	**140/130**
Minimum metal CD (nm)**		**180**	**150**	**130**	**100**	**70**	**50**
Minimum contact/via CD (nm)		**200/260**	**170/210**	**140/180**	**110/140**	**80/100**	**60/70**
Metal height/width aspect ratio - LOGIC (μP)		**1.8****	**2.0****	**2.1****	**2.4****	**2.7****	**3.0****
Via aspect ratio - LOGIC		**2.2****	**2.4****	**2.5****	**2.7****	**2.9****	**3.2****
Contact aspect ratio - DRAM - tungsten metal		**6.3**	**7**	**7.5**	**9.0**	**10.5**	**’12**
Metal effective resistivity ($\mu\Omega$–cm)		**2.2**	**2.2**	**2.2**	**2.2**	**< 1.8**	**< 1.8**
Barrier/cladding thickness (nm)		**23**	**20**	**16**	**11**	**3**	**1**
Interlevel metal insulator; effective dielectric constant (k)		**2.5 - 4.1**	**2.5 - 3.2**	**2.0 - 2.5**	**1.5 - 2.0**	**< 1.5**	**< 1.5**

**Minimum CD for isolated lines (no contacts or vias)

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Technology Requirements, 1/99 contd.

		1999 180 nm	2001 150 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm
Metal height/width aspect ratio - LOGIC (µP)		1.8**	2.0**	2.1**	2.4**	2.7**	3.0**
Via aspect ratio - LOGIC		2.2**	2.4**	2.5**	2.7**	2.9**	3.2**
Contact aspect ratio - DRAM		6.3	7	7.5	9.0	10.5	'12
Metal effective resistivity (µΩ–cm)		2.2	2.2	2.2	2.2	< 1.8	< 1.8
Barrier/cladding thickness (nm)		23	20	16	11	3	1
Interlevel metal insulator; effective dielectric constant (k)		2.5 - 4.1	2.0 - 2.5.2	1.5 - 2.05	1.5 - 2.0	< 1.5	< 1.5

- * FIT - failure in time
- ** Minimum CD for isolated lines (no contacts orvias)
- *** Metal and via A/R additive for dual damascene process flows
- **** Metal effective resistivity computed for the metal 2 (pitch not specified) wiring level assuming a conformal barrier

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Table 33 Architecture Potential Solutions, rev. 1/99

Architecture/Device	Signal	Connectivty	Packaging
3D	Low temperature operation	Self construction	MCM
	Optical/rf	Fault tolerant	Area array
		Neural wiring	Functional partiioning

- **New architectural approaches needed**
  - **3D, 3D devices and self assembled**
- **Low temperature operation boosts performance**
- **Optical**
- **Improvements primarily through design**

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1999 issues not in 1998 update

- **Low k gap-fill dielectric deposition for subtractive Cu/Al patterning**
- **Need Jmax specs that are material/level and application specific**
- **Need substantial increase in reliability text including method to evaluate**
- **More emphasis on cleans**
- **Barrier free process for Cu technology - may be treatment of low k**
- **How to incorporate metrics that address the very broad base of system on chip solutions**

Plan through 6/99

- **Complete 1/15/99 table revisions**
- **Create interconnect specific working area on ITRS web site akin to that used by interconnect DTWG -**
- **1/13/99 Wednesday 11-12 (EST) telecon to discuss RCG meeting and format**
- **2/10/99 Wednesday 9-3pm (Austin) Face-to-face**
- **3/16-18 Tues-Thurs. Video telecon for sub-teams**
- **4/9/99 Friday 10-6pm Week of MRS (draft) San Francisco**
- **5/13-14/99 Full Roadmap**
- **Face-to-face at IITC conference 5/27/99 to revise Rev 1 to Rev 2 draft and incorporate Japan inputs**

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Where do we go from here?

- **Must build physically based predictive models for interconnect.**
- **Determine physical and electrical characteristics of conductors and metals at <100 nm dimensions and multi- GHz frequencies.**
- **Constrain net size and introduce clock repeaters and pipelined communications.**
- **Evaluate optical interconnect -** ***inter*** **and** ***intra*** **chip.**
- **Develop new high Tc (353 K) superconductors which meet density and current requirements - also introduce low temperature chip operation.**
- **Optimize the partitioning between the chip interconnect and the package interconnect.**
- **Below 100 nm, there are no known materials which meet performance requirements for full-size chips.**

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